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(gate adj oxide) and ((evaporat$ or vapor) same zirconium) same (electron adj beam)	12

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DATE: Tuesday, May 28, 2002 Printable Copy Create Case

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	DB=DWPI; PLUR=YES; OP=ADJ		
L1	(gate adj oxide) and ((evaporat$ or vapor) same zirconium)	0	L1
	DB=USPT; PLUR=YES; OP=ADJ		
L2	(gate adj oxide) and ((evaporat$ or vapor) same zirconium)	56	L2
	DB=PGPB; PLUR=YES; OP=ADJ		
L3	(gate adj oxide) and ((evaporat$ or vapor) same zirconium)	9	L3
	DB=JPAB; PLUR=YES; OP=ADJ		
L4	(gate adj oxide) and ((evaporat$ or vapor) same zirconium)	0	L4
	DB=EPAB; PLUR=YES; OP=ADJ		
L5	(gate adj oxide) and ((evaporat$ or vapor) same zirconium)	0	L5
	DB=USPT; PLUR=YES; OP=ADJ		
L6	L2 and oxidiz$	39	L6
L7	(gate adj oxide) and ((evaporat$ or vapor) same metal) same (electron adj beam)	117	L7
L8	(gate adj oxide) and ((evaporat$ or vapor) same zirconium) same (electron adj beam)	12	L8

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Search Results - Record(s) 1 through 20 of 39 returned.

☐ 1. Document ID: US 6396092 B1

L6: Entry 1 of 39 File: USPT May 28, 2002

US-PAT-NO: 6396092
DOCUMENT-IDENTIFIER: US 6396092 B1

TITLE: Semiconductor device and method for manufacturing the same

DATE-ISSUED: May 28, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Takatani; Shinichiro	Koganei			JPX
Miki; Hiroshi	Shinjuku-ku			JPX
Kushida; Keiko	Kodaira			JPX
Fujisaki; Yoshihisa	Hachioji			JPX
Torii; Kazuyoshi	Hachioji			JPX

US-CL-CURRENT: 257/295; 257/303, 257/306, 257/309, 257/310, 257/741, 365/145, 365/65, 365/87, 438/239, 438/240, 438/244 , 438/253, 438/3, 438/387, 438/396

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

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☐ 2. Document ID: US 6387712 B1

L6: Entry 2 of 39 File: USPT May 14, 2002

US-PAT-NO: 6387712
DOCUMENT-IDENTIFIER: US 6387712 B1

TITLE: Process for preparing ferroelectric thin films

DATE-ISSUED: May 14, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yano; Yoshihiko	Kanagawa			JPX
Noguchi; Takao	Chiba			JPX

US-CL-CURRENT: 438/3; 438/763, 438/792, 438/909

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

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☐ 3. Document ID: US 6380579 B1

L6: Entry 3 of 39 File: USPT Apr 30, 2002

US-PAT-NO: 6380579
DOCUMENT-IDENTIFIER: US 6380579 B1

TITLE: Capacitor of semiconductor device

DATE-ISSUED: April 30, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nam; Sang-don	Yongin			KRX
Kim; Jin-won	Seoul			KRX

US-CL-CURRENT: 257/306; 257/295, 257/296, 257/297, 257/303, 257/307, 257/308, 257/309, 257/310, 257/757, 257/767, 361/15 , 438/244, 438/250, 438/253, 438/393, 438/394, 438/395, 438/396

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 4. Document ID: US 6352892 B1

L6: Entry 4 of 39 File: USPT Mar 5, 2002

US-PAT-NO: 6352892
DOCUMENT-IDENTIFIER: US 6352892 B1

TITLE: Method of making DRAM trench capacitor

DATE-ISSUED: March 5, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Jammy; Rajarao	Wappingers Falls	NY		
Mandelman; Jack A.	Stormville	NY		
Radens; Carl J.	La Guageville	NY		

US-CL-CURRENT: 438/244; 438/240, 438/249

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 5. Document ID: US 6316801 B1

L6: Entry 5 of 39 File: USPT Nov 13, 2001

US-PAT-NO: 6316801
DOCUMENT-IDENTIFIER: US 6316801 B1

TITLE: Semiconductor device having capacitive element structure and multilevel interconnection structure and method of fabricating the same

DATE-ISSUED: November 13, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Amanuma; Kazushi	Tokyo			JPX

US-CL-CURRENT: 257/306; 257/311, 257/758, 257/774

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 6. Document ID: US 6297086 B1

L6: Entry 6 of 39 File: USPT Oct 2, 2001

US-PAT-NO: 6297086
DOCUMENT-IDENTIFIER: US 6297086 B1

TITLE: Application of excimer laser anneal to DRAM processing

DATE-ISSUED: October 2, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hegde; Suryanarayan G.	Hollowville	NY		
Lee; Kam Leung	Putnam Valley	NY		
Mandelman; Jack A.	Stormville	NY		
Radens; Carl J.	LaGrangeville	NY		

US-CL-CURRENT: 438/243; 438/248, 438/249, 438/386, 438/391, 438/392

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 7. Document ID: US 6222218 B1

L6: Entry 7 of 39 File: USPT Apr 24, 2001

US-PAT-NO: 6222218
DOCUMENT-IDENTIFIER: US 6222218 B1

TITLE: DRAM trench

DATE-ISSUED: April 24, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Jammy; Rajarao	Wappingers Falls	NY		
Mandelman; Jack A.	Stormville	NY		
Radens; Carl J.	Lagrangeville	NY		

US-CL-CURRENT: 257/301; 257/296, 257/300

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 8. Document ID: US 6143655 A

L6: Entry 8 of 39 File: USPT Nov 7, 2000

US-PAT-NO: 6143655
DOCUMENT-IDENTIFIER: US 6143655 A

TITLE: Methods and structures for silver interconnections in integrated circuits

DATE-ISSUED: November 7, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Forbes; Leonard	Corvallis	OR		
Farrar; Paul A.	So. Burlington	VT		
Ahn; Kie Y.	Chappaqua	NY		

US-CL-CURRENT: 438/686; 257/742, 257/743, 257/762, 438/46, 438/602, 438/660, 438/752, 438/770, 438/85

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 9. Document ID: US 6140672 A

L6: Entry 9 of 39 File: USPT Oct 31, 2000

US-PAT-NO: 6140672
DOCUMENT-IDENTIFIER: US 6140672 A

TITLE: Ferroelectric field effect transistor having a gate electrode being electrically connected to the bottom electrode of a ferroelectric capacitor

DATE-ISSUED: October 31, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Arita; Koji	Colorado Springs	CO		
Paz de Araujo; Carlos A.	Colorado Springs	CO		

US-CL-CURRENT: 257/295; 257/296, 257/300, 438/3

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 10. Document ID: US 6121647 A

L6: Entry 10 of 39 File: USPT Sep 19, 2000

US-PAT-NO: 6121647

DOCUMENT-IDENTIFIER: US 6121647 A

TITLE: Film structure, electronic device, recording medium, and process of preparing ferroelectric thin films

DATE-ISSUED: September 19, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yano; Yoshihiko	Kanagawa			JPX
Noguchi; Takao	Chiba			JPX

US-CL-CURRENT: 257/295; 257/310

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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11. Document ID: US 6121126 A

L6: Entry 11 of 39 File: USPT Sep 19, 2000

US-PAT-NO: 6121126
DOCUMENT-IDENTIFIER: US 6121126 A

TITLE: Methods and structures for metal interconnections in integrated circuits

DATE-ISSUED: September 19, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ahn; Kie Y.	Chappaqua	NY		
Forbes; Leonard	Corvallis	OR		
Farrar; Paul A.	S. Burlington	VT		

US-CL-CURRENT: 438/602; 438/46, 438/619, 438/688, 438/752, 438/770, 438/779

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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12. Document ID: US 6100176 A

L6: Entry 12 of 39 File: USPT Aug 8, 2000

US-PAT-NO: 6100176
DOCUMENT-IDENTIFIER: US 6100176 A

TITLE: Methods and structures for gold interconnections in integrated circuits

DATE-ISSUED: August 8, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Forbes; Leonard	Corvallis	OR		
Farrar; Paul A.	So. Burlington	VT		
Ahn; Kie Y.	Chappaqua	NY		

US-CL-CURRENT: 438/619; 257/742, 257/743, 438/622, 438/624

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 13. Document ID: US 6084260 A

L6: Entry 13 of 39 File: USPT Jul 4, 2000

US-PAT-NO: 6084260
DOCUMENT-IDENTIFIER: US 6084260 A

TITLE: Semiconductor storage device and method for manufacturing the same

DATE-ISSUED: July 4, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hirai; Tadahiko	Fuji			JPX
Tarui; Yasuo	Higashikurume-shi, Tokyo 203			JPX

US-CL-CURRENT: 257/295; 257/324, 257/411

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 14. Document ID: US 6027961 A

L6: Entry 14 of 39 File: USPT Feb 22, 2000

US-PAT-NO: 6027961
DOCUMENT-IDENTIFIER: US 6027961 A

TITLE: CMOS semiconductor devices and method of formation

DATE-ISSUED: February 22, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Maiti; Bikas	Austin	TX		
Tobin; Philip J.	Austin	TX		
Mogab; C. Joseph	Austin	TX		
Hobbs; Christopher	Austin	TX		
Frisa; Larry E.	Radebeul bei Dresden			DEX

US-CL-CURRENT: 438/199; 438/584, 438/592

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 15. Document ID: US 6020024 A

L6: Entry 15 of 39 File: USPT Feb 1, 2000

US-PAT-NO: 6020024
DOCUMENT-IDENTIFIER: US 6020024 A

TITLE: Method for forming high dielectric constant metal oxides

DATE-ISSUED: February 1, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Maiti; Bikas	Austin	TX		
Tobin; Philip J.	Austin	TX		
Hegde; Rama I.	Austin	TX		
Cuellar; Jesus	LaGrange	TX		

US-CL-CURRENT: 427/248.1; 427/255.7, 427/309, 427/527, 427/99, 438/287

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 16. Document ID: US 6013160 A

L6: Entry 16 of 39 File: USPT Jan 11, 2000

US-PAT-NO: 6013160
DOCUMENT-IDENTIFIER: US 6013160 A

TITLE: Method of making a printhead having reduced surface roughness

DATE-ISSUED: January 11, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Raisanen; Alan D.	Sodus	NY		
Burke; Cathie J.	Rochester	NY		

US-CL-CURRENT: 204/192.15; 204/192.21

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 17. Document ID: US 5955755 A

L6: Entry 17 of 39 File: USPT Sep 21, 1999

US-PAT-NO: 5955755
DOCUMENT-IDENTIFIER: US 5955755 A

TITLE: Semiconductor storage device and method for manufacturing the same

DATE-ISSUED: September 21, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hirai; Tadahiko	Fuji			JPX
Tarui; Yasuo	Tokyo 203			JPX

US-CL-CURRENT: 257/295; 257/324, 257/406, 438/287

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 18. Document ID: US 5955213 A

L6: Entry 18 of 39 File: USPT Sep 21, 1999

US-PAT-NO: 5955213
DOCUMENT-IDENTIFIER: US 5955213 A

TITLE: Ferroelectric thin film, electric device, and method for preparing ferroelectric thin film

DATE-ISSUED: September 21, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yano; Yoshihiko	Kanagawa			JPX
Noguchi; Takao	Chiba			JPX

US-CL-CURRENT: 428/700; 428/450, 428/469, 428/472, 428/701

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 19. Document ID: US 5920775 A

L6: Entry 19 of 39 File: USPT Jul 6, 1999

US-PAT-NO: 5920775
DOCUMENT-IDENTIFIER: US 5920775 A

TITLE: Method for forming a storage capacitor within an integrated circuit

DATE-ISSUED: July 6, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Koh; Chao-Ming	Hsinchu			TWX

US-CL-CURRENT: 438/241; 438/210, 438/253, 438/396

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 20. Document ID: US 5920121 A

L6: Entry 20 of 39 File: USPT Jul 6, 1999

US-PAT-NO: 5920121
DOCUMENT-IDENTIFIER: US 5920121 A

TITLE: Methods and structures for gold interconnections in integrated circuits

DATE-ISSUED: July 6, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Forbes; Leonard	Corvallis	OR		
Farrar; Paul A.	So. Burlington	VT		
Ahn; Kie Y.	Chappaqua	NY		

US-CL-CURRENT: 257/742; 257/522, 257/743

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 21. Document ID: US 5919515 A

L6: Entry 21 of 39 File: USPT Jul 6, 1999

US-PAT-NO: 5919515
DOCUMENT-IDENTIFIER: US 5919515 A

TITLE: Ferroelectric thin film, electric device and method for preparing ferroelectric thin film

DATE-ISSUED: July 6, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yano; Yoshihiko	Kanagawa			JPX
Noguchi; Takao	Chiba			JPX

US-CL-CURRENT: 427/126.3; 117/109, 427/126.1

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 22. Document ID: US 5916378 A

L6: Entry 22 of 39 File: USPT Jun 29, 1999

US-PAT-NO: 5916378
DOCUMENT-IDENTIFIER: US 5916378 A

TITLE: Method of reducing metal contamination during semiconductor processing in a reactor having metal components

DATE-ISSUED: June 29, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Bailey; Robert Jeffrey	Santa Cruz	CA		
Brady; Patrick J.	Livermore	CA		

US-CL-CURRENT: 148/243; 148/275, 148/276, 148/280, 148/285, 428/472.2, 438/379, 438/680, 438/681, 438/909

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 23. Document ID: US 5907789 A

L6: Entry 23 of 39 File: USPT May 25, 1999

US-PAT-NO: 5907789
DOCUMENT-IDENTIFIER: US 5907789 A

TITLE: Method of forming a contact-hole of a semiconductor element

DATE-ISSUED: May 25, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Komatsu; Hiroshi	Kanagawa			JPX

US-CL-CURRENT: 438/649; 438/592, 438/648, 438/655, 438/656, 438/683, 438/685

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments KWIC
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☐ 24. Document ID: US 5851841 A

L6: Entry 24 of 39 File: USPT Dec 22, 1998

US-PAT-NO: 5851841
DOCUMENT-IDENTIFIER: US 5851841 A

TITLE: Method for producing ferroelectric film element, and ferroelectric film element and ferroelectric memory element produced by the method

DATE-ISSUED: December 22, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ushikubo; Maho	Kashiwa			JPX
Ito; Yasuyuki	Kashiwa			JPX
Yokoyama; Seiichi	Kashiwa			JPX
Matsunaga; Hironori	Noda			JPX
Koba; Masayoshi	Nara			JPX

US-CL-CURRENT: 438/240; 438/781

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments KWIC
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☐ 25. Document ID: US 5828080 A

L6: Entry 25 of 39 File: USPT Oct 27, 1998

US-PAT-NO: 5828080
DOCUMENT-IDENTIFIER: US 5828080 A

TITLE: Oxide thin film, electronic device substrate and electronic device

DATE-ISSUED: October 27, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yano; Yoshihiko	Kanagawa			JPX
Noguchi; Takao	Chiba			JPX

US-CL-CURRENT: 257/43; 257/310, 257/314, 257/410, 257/411

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 26. Document ID: US 5810923 A

L6: Entry 26 of 39 File: USPT Sep 22, 1998

US-PAT-NO: 5810923
DOCUMENT-IDENTIFIER: US 5810923 A

TITLE: Method for forming oxide thin film and the treatment of silicon substrate

DATE-ISSUED: September 22, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yano; Yoshihiko	Kanagawa			JPX
Noguchi; Takao	Chiba			JPX
Nagano; Katsuto	Kanagawa			JPX

US-CL-CURRENT: 117/84; 117/89, 117/94, 427/248.1, 427/250

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 27. Document ID: US 5801105 A

L6: Entry 27 of 39 File: USPT Sep 1, 1998

US-PAT-NO: 5801105
DOCUMENT-IDENTIFIER: US 5801105 A

TITLE: Multilayer thin film, substrate for electronic device, electronic device, and preparation of multilayer oxide thin film

DATE-ISSUED: September 1, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yano; Yoshihiko	Kanagawa			JPX
Noguchi; Takao	Chiba			JPX

US-CL-CURRENT: 438/785; 438/2, 438/3, 438/648

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

28. Document ID: US 5753934 A

L6: Entry 28 of 39 File: USPT May 19, 1998

US-PAT-NO: 5753934
DOCUMENT-IDENTIFIER: US 5753934 A

TITLE: Multilayer thin film, substrate for electronic device, electronic device, and preparation of multilayer oxide thin film

DATE-ISSUED: May 19, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yano; Yoshihiko	Kanagawa			JPX
Noguchi; Takao	Chiba			JPX

US-CL-CURRENT: 257/30; 257/31, 257/635, 257/636, 257/637

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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29. Document ID: US 5719083 A

L6: Entry 29 of 39 File: USPT Feb 17, 1998

US-PAT-NO: 5719083
DOCUMENT-IDENTIFIER: US 5719083 A

TITLE: Method of forming a complex film over a substrate having a specifically selected work function

DATE-ISSUED: February 17, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Komatsu; Hiroshi	Kanagawa			JPX

US-CL-CURRENT: 438/652; 438/197, 438/647, 438/655

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

30. Document ID: US 5700722 A

L6: Entry 30 of 39 File: USPT Dec 23, 1997

US-PAT-NO: 5700722
DOCUMENT-IDENTIFIER: US 5700722 A

TITLE: Process for forming silicide plugs in semiconductor devices

DATE-ISSUED: December 23, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Sumi; Hirofumi	Kanagawa			JPX

US-CL-CURRENT: 438/649; 438/651, 438/660, 438/672

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 31. Document ID: US 5686151 A

L6: Entry 31 of 39 File: USPT Nov 11, 1997

US-PAT-NO: 5686151
DOCUMENT-IDENTIFIER: US 5686151 A

TITLE: Method of forming a metal oxide film

DATE-ISSUED: November 11, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Imai; Keitaro	Kawasaki			JPX
Kiyotoshi; Masahiro	Matsudo			JPX
Okano; Haruo	Tokyo			JPX

US-CL-CURRENT: 427/576; 427/126.3, 427/62, 505/447, 505/477, 505/734

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 32. Document ID: US 5619057 A

L6: Entry 32 of 39 File: USPT Apr 8, 1997

US-PAT-NO: 5619057
DOCUMENT-IDENTIFIER: US 5619057 A

TITLE: Complex film overlying a substrate with defined work function

DATE-ISSUED: April 8, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Komatsu; Hiroshi	Kanagawa			JPX

US-CL-CURRENT: 257/382; 257/384, 257/407, 257/412, 257/413

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 33. Document ID: US 5572052 A

L6: Entry 33 of 39 File: USPT Nov 5, 1996

US-PAT-NO: 5572052
DOCUMENT-IDENTIFIER: US 5572052 A

TITLE: Electronic device using zirconate titanate and barium titanate ferroelectrics in insulating layer

DATE-ISSUED: November 5, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kashihara; Keiichiro	Hyogo			JPX
Okudaira; Tomonori	Hyogo			JPX
Itoh; Hiromi	Hyogo			JPX

US-CL-CURRENT: 257/295; 361/312, 361/313, 361/322, 365/145, 365/149

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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☐ 34. Document ID: US 5397735 A

L6: Entry 34 of 39 File: USPT Mar 14, 1995

US-PAT-NO: 5397735
DOCUMENT-IDENTIFIER: US 5397735 A

TITLE: Process for hardening active electronic components against ionizing radiations, and hardened components of large dimensions

DATE-ISSUED: March 14, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mercandalli; Louis	Montgeron			FRX
Pribat; Didier	Sevres			FRX
Dessertenne; Bernard	Bures Sur Yvette			FRX
Karapiperis; Leonidas	Bourg la Reine			FRX
Dieumegard; Dominique	Mareil-Marly			FRX

US-CL-CURRENT: 438/459; 117/45, 117/931, 117/934, 438/479, 438/489, 438/953, 438/967

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 35. Document ID: US 5055260 A

L6: Entry 35 of 39 File: USPT Oct 8, 1991

US-PAT-NO: 5055260
DOCUMENT-IDENTIFIER: US 5055260 A

TITLE: Reactor analysis system

DATE-ISSUED: October 8, 1991

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Roberge; Raymond P.	Chappaqua	NY		
Francis, Jr.; Arthur W.	Monroe	NY		
Wolfe; Thomas G.	Westport	CT		

US-CL-CURRENT: 422/62; 422/103, 422/70, 422/78, 422/80, 422/81, 422/83, 422/90, 436/115, 436/124, 436/158, 436/55

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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36. Document ID: US 4983543 A

L6: Entry 36 of 39 File: USPT Jan 8, 1991

US-PAT-NO: 4983543
DOCUMENT-IDENTIFIER: US 4983543 A

TITLE: Method of manufacturing a semiconductor integrated circuit having an interconnection wire embedded in a protective layer covering the semiconductor integrated circuit

DATE-ISSUED: January 8, 1991

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Sato; Yasuhisa	Isehara			JPX
Motoyama; Takushi	Kawasaki			JPX

US-CL-CURRENT: 438/630; 438/641, 438/649, 438/672, 438/675

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

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37. Document ID: US 4891186 A

L6: Entry 37 of 39 File: USPT Jan 2, 1990

US-PAT-NO: 4891186
DOCUMENT-IDENTIFIER: US 4891186 A

TITLE: Reactor analysis system

DATE-ISSUED: January 2, 1990

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Roberge; Raymond P.	Chappaqua	NY		
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Wolfe; Thomas G.	Cos Cob	CT		

US-CL-CURRENT: 422/83; 422/62, 436/115, 436/124, 436/158, 436/55

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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38. Document ID: US 4392150 A

L6: Entry 38 of 39 File: USPT Jul 5, 1983

US-PAT-NO: 4392150
DOCUMENT-IDENTIFIER: US 4392150 A

TITLE: MOS Integrated circuit having refractory metal or metal silicide interconnect layer

DATE-ISSUED: July 5, 1983

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Courreges; Francis G.	Sandy	UT		

US-CL-CURRENT: 257/304; 257/383, 257/757, 438/586, 438/647, 438/655

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

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39. Document ID: US 3849216 A

L6: Entry 39 of 39 File: USPT Nov 19, 1974

US-PAT-NO: 3849216
DOCUMENT-IDENTIFIER: US 3849216 A

TITLE: METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE MANUFACTURED BY USING THE METHOD

DATE-ISSUED: November 19, 1974

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Salters; Roelof Herman Willem	Emmasingel, Eindhoven			NL

US-CL-CURRENT: 438/225; 257/365, 257/396, 438/229, 438/297, 438/301, 438/453

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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Welcome !

Thank you for your interest in *the International Technology Roadmap for Semiconductors: 1999 edition.*

We have worked diligently as teams of Technology Working Groups from around the world to assess technology requirements for the semiconductor industry over the next 15 years. The working groups include the technologies of Design; Test and Test Equipment; Process Integration, Devices, and Structures; Front-end Processes; Lithography; Interconnect; Factory Integration; Assembly and Packaging; Environment, Safety, and Health; Defect Reduction; Metrology; and Modeling and Simulation.

For this edition, our focus has been on near term needs for the next six years, and then assessing the longer term issues in the years beyond 2005. We see technical opportunities as well as challenges for all areas as the industry approaches the 100 nm feature size realm and beyond.

As we continue to assess where we are and where we are going, we are once again humbled at the scope of this exercise of "roadmapping" our industry's needs in the areas of research and development. This is an ongoing process as new innovations surface throughout the world, requiring constant review and routine revisions of this information.

This effort is sponsored by the Semiconductor Industry Association (SIA), and with participation from members of the European Electronic Component Association (EECA), the Electronic Industries Association of Japan (EIAJ), the Korea Semiconductor Industry Association (KSIA), and the Taiwan Semiconductor Industry Association (TSIA).

About the *International Technology Roadmap for Semiconductors*

The semiconductor industry consists of a global community of suppliers, researchers, and chip manufacturers. The Semiconductor Industry Association's (SIA) 1994 and 1997 editions of the *National Technology Roadmap for Semiconductors* were very valuable to this world wide industry. The community has responded to the recommendations of the Roadmap for continuing success. It is understood, however, the industry needs for research and development are constantly changing, requiring frequent reviews and new assessments. It is recognized that these assessments that include the entire community leverages our understanding of key challenges we all face as an industry.

As such, the Technology Roadmap for Semiconductors is always in active review. The year 1999 is a formal revision year for the Roadmap. The Technology Working Groups (TWGs) assess the data for technology needs and areas where innovation is encouraged. By consensus these teams update the information. ITRS conferences provide a forum for review by the entire semiconductor community for feedback and input.

Once this feedback is gathered, each TWG issues a formal report. These reports make up the Roadmap. The Roadmap is then reviewed and approved by technical advisory boards from all over the world, prepared for distribution, and made available to the public.

We invite you to participate in this dynamic process by coming to the ITRS Conferences to promote continued success of the industry!

Special thanks to members of the European Electronic Component Association (EECA), the Electronic Industries Association of Japan (EIAJ), the Korea Semiconductor Industry Association (KSIA), and the Taiwan Semiconductor Industry Association (TSIA) for their valued input.

About this CD ...

The International Technology Roadmap for Semiconductors is contained on this CD as an interactive electronic document, with navigation links throughout each chapter.

Table of Contents Previous Next Last

The Table of Contents for each chapter is also interactive.

Additionally, as a new feature of Roadmap information, several chapters have links to additional information that further explain data. These are highlighted as blue, underlined text.
(try it here by selecting with your mouse.)

What is on this CD?

- ITRS document as individual chapter files—Adobe 3.0 pdf. format
- Supplemental information—Microsoft Word 97, Excel 7.0, or PowerPoint 7.0 file format.
- Contact information for the IRC and each ITWG.
- A link to the ITRS public web site for continual updated information— http://public.itrs.net

The information is available for printing on postscript printers, and is downloadable.

(Tip: You can also access the individual files by using your file manager and viewing the directory of the CD.)

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Please contact us at SEMATECH at 1+(512)356-6877. We will happy to help you.

Thank you,

The ITRS production team

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International Technology Roadmap for Semiconductors
1999 Edition

Introduction

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FOREWORD

The semiconductor industry has continued to prosper and also to foster the growth of multiple industries since the early 70s. At the center of this sustained growth, resides the unique factor that has made the semiconductor industry successful: "Decreases in device feature size have provided improved functionality at a reduced cost." Device linear features have indeed decreased at the rate of about 70% every three years for most of the industry's history. Acceleration to a 2-year cycle has been experienced in the most recent years. Cost per function has simultaneously decreased at an average rate of about 25–30%/year/function.

Since 1992, the Semiconductor Industry Association (SIA) has coordinated the efforts of producing what was originally the *National Technology Roadmap for Semiconductors* (NTRS). This document of requirements and possible solutions was generated three times: in 1992, 1994, and 1997. The NTRS has provided a 15-year outlook on the major trends of the semiconductor industry. As such, it has been a good reference document for all semiconductor manufacturers. Most of all, it has provided useful guidance for suppliers of equipment, materials and software. It has also provided clear targets for researchers in the outer years.

The semiconductor industry has become a global industry in the '90s, as many semiconductor suppliers have established manufacturing or assembly facilities in multiple regions of the world. Similarly, the suppliers to the semiconductor industry have established world-wide operations. Furthermore, alliances, joint ventures, and many forms of cooperation have been established among semiconductor manufactures as well as among equipment, materials, and software suppliers.

The above considerations have led to the realization that a document that provides guidance for the whole industry would benefit from inputs from all regions of the world that have leadership activities in the field of semiconductors. This realization has led to the creation of the *International Technology Roadmap for Semiconductors* (ITRS). The invitation to cooperation on the ITRS was extended by the SIA at the World Semiconductor Council in April of 1998. The offer was enthusiastically accepted by the trade organizations of Europe (EECA), Korea (KSIA), Japan (EIAJ), and Taiwan (TSIA). The initial collaboration of these five organizations produced the ITRS 1998 Update, which consisted of a comprehensive revision of the 1997 NTRS tables. This year, the five regions have jointly produced a new edition of the semiconductor industry roadmap document—*The International Technology Roadmap for Semiconductors: 1999.*

As the reader will realize by studying this newly created document, the number and the difficulty of the technical challenges continue to increase as technology moves forward. The red areas signifying: "No solutions yet" are in most cases shown within a 5-year reach. Traditional scaling, which has been at the basis of the semiconductor industry for the last 30 years, is indeed beginning to show the fundamental limits of the materials constituting the building blocks of the planar CMOS process. However, new materials can be introduced in the basic CMOS structure to replace and/or augment the existing ones to further extend the device scaling approach. Since the assimilation of these new materials into the modified CMOS process gives the device physicist and the circuit designer improved electrical performance similar to the historical trends, this new regime has been often identified as "Equivalent Scaling." It is expected that these new materials will provide a viable solution to extending the limit of the planar CMOS process for the next 5–10 years.

Despite the use of these new materials, it will be challenging to maintain a rate of improvement in electrical performance of about 2× every two years in the high-performance components by relying exclusively on improvements in technology. Innovation in the techniques used in circuit and system design will be essential to maintain the historical trends in performance improvement. To achieve this result it is expected that the integration of multiple silicon technologies on the same chip and a closer integration of package and silicon technology will be necessary. This emerging product category is identified as Performance System-on-a-Chip (P-SoC).

On the other hand, cost-effective solutions will require an assessment of the silicon technology complexity that can be afforded for a given cost. Specifically, given a system cost target, what technology complexity can be afforded? This product category is identified as Cost-effective System-on-a-Chip (C-SoC).

Finally, as the ITRS looks at 10–15 years in the future, it becomes evident that most of the known technological capabilities will be approaching or have reached their limits. In order to provide the Computer, Communication, Consumer, and other electronics industries with continuously more efficient building blocks, it becomes necessary to investigate new devices that may provide a more cost-effective alternative to planar CMOS in this timeframe. Adequate preparation for this potential transition must include starting to identify the possible candidates as early as possible and, then, systematically testing their feasibility.

In conclusion, note that the planar CMOS silicon gate technology ultimately resulted from technical investigations initiated in the 1940s. These early studies did not lead to the start of the semiconductor industry, as we know it today, until the late 60s. It would be difficult for any single company to support the progressively increasing R&D investments necessary to evolve the technology from Traditional Scaling to Equivalent Scaling, and, finally, to investigate and develop a set of new devices usable beyond the limits of CMOS. The contributors to the ITRS agree that much of the R&D needs to be in the shared "pre-competitive domain."

It is the purpose of this 1999 ITRS to provide a reference document of requirements, potential solutions, and their timing for the semiconductor industry. This result has been accomplished by providing a forum for international discussion, cooperation, and agreement among the leading semiconductor manufacturers and the leading suppliers of equipment, materials, and software, as well as researchers from university and government labs. It is hoped that, in the future, starting with this document as a common reference and through cooperative efforts among the various ITRS participants, the challenge of R&D investments will be cooperatively and more uniformly shared by the whole industry.

ACKNOWLEDGMENTS

Producing this inaugural *International Technology Roadmap for Semiconductors* has been a significant undertaking. The ITRS is produced by a global community of researchers, manufacturers, and suppliers who *volunteer* to travel; meet; build teams; examine material (on a greater scale than what is represented in this Roadmap edition); discuss, write, and reach consensus on key industry needs; and identify opportunities for new devices, materials, and technologies to help foster continued industry success.

The Semiconductor Industry Association wishes to formally and sincerely express its appreciation for the many hours of tremendous personal effort involved to deliver this collection of information. The devotion and attention given by each individual contributor of the Roadmap represents perhaps the greatest enabling energy within our industry.

The SIA thanks the

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INTRODUCTION

OVERVIEW

The 1999 edition of *The International Technology Roadmap for Semiconductors (ITRS)* is the result of a worldwide consensus building process. The participation of semiconductor experts from Europe, Japan, Korea, and Taiwan, as well as the U.S.A., ensures that the 1999 ITRS is an even more valid source of guidance for the industry as we strive to extend the historical advancement of semiconductor technology and the worldwide integrated circuit (IC) market. During the past year, those of us involved in the ITRS process have been invigorated by the enthusiasm of our new international partners in this endeavor. Their diverse expertise and dedicated efforts have brought the "Roadmap" to a new level of agreement about future technology requirements for the semiconductor industry. This is a very significant advance toward further fulfilling the goal of the Roadmap to present an industry-wide consensus on the "best current estimate" of our future research and development needs out to a 15-year horizon. As such, it should provide a guide to the efforts of research organizations, and research sponsors within industry, government, and universities.

For four decades, the semiconductor industry has distinguished itself by the rapid pace of improvement in its products. The principal categories of improvement trends are shown in Table A with examples of each. Most of these trends have been exponential, resulting principally from the industry's ability to exponentially decrease the minimum feature sizes used to fabricate integrated circuits. Of course, the most frequently cited trend is in integration level, which is usually expressed as Moore's Law ("the number of components per chip doubles every 18 months"). The most significant trend for society is in decreasing cost-per-function, which has led to an enormous growth in the market for integrated circuits over the past forty years.

Table A Improvement Trends for ICs Enabled by Feature Scaling

TREND	*EXAMPLE*
Functionality	nonvolatile memory, smart power
Integration Level	components/chip—Moore's Law
Compactness	components/cm^2
Speed	microprocessor clock MHz
Power	laptop or cell phone battery life
Cost	cost-per-function—historically decreasing at >25% / year

All of these improvement trends have been enabled by significant R&D investments and by industry-wide learning. Within the last two decades, the growing size of the required investments has changed the industry perception of collaboration and "the competitive/pre-competitive boundary." This has spawned many R&D partnerships, consortia, and other cooperative ventures.

TECHNOLOGY REQUIREMENTS PERSPECTIVE

Since its inception in 1992, a basic premise of the Roadmap has been that continued scaling of microelectronics would further reduce the cost per function (historically, ~25%/year) and promote market growth for integrated circuits (averaging ~15%/year). Thus, the Roadmap has been put together in the spirit of a challenge—essentially, "What technical capabilities need to be developed for us to stay on Moore's Law and the other trends?" During the 1980s and '90s, this challenge has become so formidable that more and more of the development effort has been shared in a precompetitive environment including consortia and collaboration with suppliers. In this process, the ITRS serves as a guide to the principal technology needs. It does this in two ways: (1) showing the relatively near-term "targets" that need to be met by "technology solutions" currently under development, and (2) indicating where there are no "known solutions" (of reasonable confidence) to continued scaling in some aspect of the semiconductor technology. This latter situation is highlighted as "red" on the Roadmap. The "red" is officially "on" the Roadmap to clearly warn where progress might end if some real breakthroughs aren't achieved in the future. Such breakthroughs would result in the "red" turning to "yellow" and, ultimately, "white" in future editions and could easily be

responsible for new concepts appearing "on" the Roadmap. In fact, the rate of migration of useful new concepts onto the Roadmap could be used as a measure of its success in fostering technology progress.

For some Roadmap readers, the "red" designation may not have adequately served its purpose of highlighting significant and exciting challenges. There can be a tendency to view any number in the Roadmap as "on the road to sure implementation" regardless of its color. An analysis of "red" usage might classify the "red" parameters into two categories:

(1) where the consensus is that the particular value will ultimately be achieved (perhaps late), but for which we don't have much confidence in any currently proposed solution(s), or

(2) where the consensus is that the value will never be achieved (for example, some "work-around" will render it irrelevant or progress will indeed end).

A conservative interpretation might view "red" parameters of the "second kind" as effectively "beyond" or "off" the Roadmap. In future editions of the ITRS, we may try to distinguish these cases ("shades of red") or use other means to clarify the often-used but poorly defined terminology "on/off the Roadmap."

Another sense in which items may be "on/off the Roadmap" is in terms of the breadth of technology addressed. The scope of the 1999 ITRS specifically includes detailed technology requirements for all "Complementary Metal-Oxide-Silicon" (CMOS) integrated circuits, including mixed-signal products. This group constitutes over 75% of the world's semiconductor consumption. Of course, many of the same technologies used to design and manufacture CMOS ICs are also used for other products such as compound-semiconductor, discrete, and micro-electromechanical systems (MEMS) devices. Thus, to a large extent, the Roadmap covers many common technology requirements for most "thin-film-process-based micro/nanotechnology."

The ITRS time horizon (15 years) provides another boundary to what may be considered "on/off the Roadmap." To date, each edition of the ITRS has been built around a view toward continued scaling of CMOS technology. However, with the 1999 edition, we are reaching the point where the horizon of the Roadmap approximately coincides with the most optimistic projections for continued scaling of CMOS (for example, MOSFET channel lengths of roughly 20 nm). It is also difficult for most people in the semiconductor industry to imagine how we could continue to afford the historic trends of increase in process equipment and factory costs for another 15 years! Thus, future editions of the ITRS may begin pointing toward more radical approaches to perpetuate our ability to further reduce the cost-per-function and increase the performance of integrated circuits. It is probable that such approaches will involve new devices as well as new manufacturing paradigms. It is a strong intent of this edition of the Roadmap to help us prepare for the future by enhancing communication and stimulating creative solutions to the many critical issues and research needs identified herein.

POTENTIAL SOLUTIONS PERSPECTIVE

The ITRS attempts to avoid prematurely identifying definite solutions to the future technology challenges. This is difficult, since guidance on the needs is intended and "one person's need is sometimes another person's solution" (for example, via the customer-supplier relationship or some other type of connection within the "technology hierarchy"). Despite this need to provide guidance, the Roadmap participants are continually pursuing new ways to prevent the Roadmap itself from being interpreted as limiting the range of creative approaches to further advance microelectronics technology. One of the resulting compromises has been to only present illustrative examples of potential solutions to selected challenges in the ITRS. In all cases, it should be noted that these are not to be construed even as complete lists of all solutions suggested to date, much less limits on what should be explored in the near future. A few of the potential technical solutions are listed, where known, just to convey current thinking and efforts. Furthermore, the listing of a particular potential solution does not constitute an endorsement by the Roadmap process. It is *not* the intent of this document to convey or to be interpreted as portraying the most likely solutions to be adopted, nor to focus attention on those potential solutions currently known at the expense of other innovative concepts. In fact, it is eagerly hoped that this Roadmap will inspire additional innovative concepts. The semiconductor industry's future success continues to depend on new ideas.

OVERALL ROADMAP PROCESS AND STRUCTURE

Each technology-area chapter of the ITRS is written by a corresponding International Technology Working Group (ITWG) consisting of experts in that field from industry (chip-makers as well as their equipment and materials suppliers), government, and universities. In addition, each edition of the ITRS incorporates feedback gathered from an even larger community through "sub-TWG meetings" and public "Roadmap Workshops." For this edition, an ITRS Workshop was held on July 8–9, 1999 in Santa Clara, California. The Roadmap resulting from this broad input is, hopefully, a "best-attempt" at building the widest possible consensus on the future technology needs of the semiconductor industry.

The ITWGs are of two types: "Focus" TWGs and "Crosscut" TWGs. The Focus TWGs correspond to typical sub-activities that sequentially span the "Design/Process/Test/Package product flow" for integrated circuits. The Crosscut TWGs represent important supporting activities that tend to individually overlap with the "product flow" at many critical points. For the 1999 ITRS, the Focus TWGs are the following:

- Design
- Test
- Process Integration, Devices, & Structures
- Front-End Processes
- Lithography
- Interconnect
- Factory Integration
- Assembly & Packaging

Similarly, the 1999 Crosscut TWGs are the following:

- Environment, Safety, & Health
- Defect Reduction
- Metrology
- Modeling & Simulation

Each ITWG has two representatives from each of the five geographical regions (Europe, Korea, Japan, Taiwan, and the U.S.A.). These representatives are typically elected from "domestic" TWGs in each of their regions. Overall coordination of the ITRS process is the responsibility of the International Roadmap Committee (IRC), which also has two members from each region (for example, representing a regional coordinating committee such as the SIA Roadmap Coordinating Group [RCG] for the U.S.A.).

The principal IRC functions include:

- providing guidance/coordination for the ITWGs,
- hosting the ITRS Workshops, and
- editing the ITRS.

A central part of the IRC guidance/coordination is provided through the up-front creation (as well as continued updating) of a set of Overall Roadmap Technology Characteristics (ORTC) Tables. These tables summarize key high-level technology requirements, which define the future "Technology Nodes" and, generally, establish some common reference points for establishing consistency between the chapters written by individual ITWGs. The high-level targets expressed in the ORTC Tables are based, in part, on the compelling economic strategy to maintain the current high rate of advancement in integrated circuit technologies. Thus, the ORTC provide a "top-down business incentive" to balance the tendency for the ITWGs to become conservative in expressing their individual, detailed future requirements.

The "principal tables" in each chapter are individual Technology Requirements tables, patterned after the ORTC Tables. For the 1999 ITRS, the ORTC and Technology Requirements tables have been separated into "Near-Term Years" (1999 through 2005, annually) and "Long-term Years" (2008, 2011, and 2014). This new format is illustrated in Table B, which contains a few key "lithography-related" ORTC lines.

Table B ITRS Table Structure—
Key Lithography-Related Characteristics by Product Type

NEAR-TERM YEARS

YEAR *TECHNOLOGY NODE*	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*	*DRIVER*
DRAM ½ PITCH (nm)	*180*	*165*	*150*	*130*	*120*	*110*	*100*	*D ½*
MPU GATE LENGTH (nm)	*140*	*120*	*100*	*85-90*	*80*	*70*	*65*	*M GATE*
MPU / ASIC ½ PITCH (nm)	*230*	*210*	*180*	*160*	*145*	*130*	*115*	*M & A ½*
ASIC GATE LENGTH (nm)	*180*	*165*	*150*	*130*	*120*	*110*	*100*	*A GATE*

LONG-TERM YEARS

YEAR *TECHNOLOGY NODE*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*	*DRIVER*
DRAM ½ PITCH (nm)	*70*	*50*	*35*	*D ½*
MPU GATE LENGTH (nm)	*45*	*30-32*	*20-22*	*M GATE*
MPU / ASIC ½ PITCH (nm)	*80*	*55*	*40*	*M & A ½*
ASIC GATE LENGTH (nm)	*70*	*50*	*35*	*A GATE*

The ORTC and Technology Requirements tables are intended to indicate current best estimates of introduction timing for specific technology requirements. Ideally, the Roadmap might show multiple timing points along the "research-development-prototyping-manufacturing" cycle for each requirement. However, in the interests of simplicity, usually only one point in time is currently estimated. The "default" point is called "Year of Introduction" in the ITRS, which may be characterized as "at the leading-edge of ramp to volume manufacturing." Note, however, that some rows in the ORTC and Technology Requirements tables refer to other timing points, which are defined for each case (e.g., "at sample"). Of course, for the "Long-term Years," it's possible for the "best-estimate year of introduction" to fall in between the selected 3-year table intervals for some technology requirements. However, this will generally not be the case, since the concept of "Technology Nodes" attempts to synchronize technology development around a "synergistic cycle" that has historically been linked to the introduction of new Dynamic Random Access Memory (DRAM) Generations with a 4× increase in bits/chip. For as long as this cycle strictly followed Moore's Law (3-year cycle for 4×), the Technology Nodes and DRAM generations were essentially synonymous. However, in recent years, the "technology-development cycle" has been closer to two years. In addition, a greater diversity of products serving as technology drivers, faster-paced introduction/optimization of product-specific technology, and the general increase in business and technology complexity are all tending to "de-couple the parameters" that have traditionally characterized "advance to the next technology node." For example, it is obvious that the scaling of transistor gate length and copper metal linewidth are relatively independent of the scaling of DRAM cell area. They are all still fundamentally limited by lithography capability, but, today, there are many other very influential factors. In fact, even the choice of basic lithography technology has tended to become more "product specific" (such as "pushing the wavelength as fast as possible" versus "using phase-shift masks"). Thus, for future editions of the ITRS, we will need to revisit the utility of continuing to list "Technology Nodes." However, for 1999, the ITRS shows six nodes of future semiconductor technology, through the "35-nm Generation" (which includes 20–22-nm transistor gate lengths). Thus, note that the "Node Designation" ("35-nm" at the horizon of the 1999 ITRS) is defined by DRAM ½ Pitch (one of the rows in Table B), not by the transistor gate length or minimum feature size characteristic of that Node.

Additional (and, in some cases, more precise) definitions related to the ITRS tables may be found in Appendix B.

TECHNOLOGY DRIVERS

The particular lithography-related rows selected for Table B from the ORTC tables are special in that any one of them may be designated by an ITWG as a "Driver" for any specific row in one of their Technology Requirements Tables. The designation of Drivers for Technology Requirements assists in the process of convergence on the final ITRS tables and also provides an indication of assumed timing dependencies in the final document. Thus, as the Roadmap is updated in subsequent editions, this information will be used for constructing a first-pass strawman version of the new tables. For example, if the requirements in any of these Driver Rows of the ORTC Tables were subsequently pulled-in by one year, it would be assumed that rows in the ITWG Technology Requirements tables would shift by default along with their designated ORTC Driver row. If no Driver is indicated for a particular requirement, there would be no automatic shift; however, interpolation would be used, as necessary to generate new numbers for those rows in columns corresponding to years that were not listed in the previous edition.

TECHNOLOGY NODE CHALLENGES

INTRODUCTION

System-on-a-chip (SoC) devices, for promising use in consumer and industrial electronics applications such as digital communications equipment, have been added to the scope of the *International Technology Roadmap for Semiconductors: 1999.* In addition, DRAM half pitches of 180, 130, 100, 70, 50 and 35 nm have been defined as technology nodes that are general indices of technology development. Each node represents a reduction to approximately 70 percent of the preceding node. Each step represents the creation of significant technology progress.

In addition, specific years have been targeted for the commencement of ramp to mass production (typically, monthly shipments of at least 10,000 units) in each of the various technology nodes. These technology nodes, which are common to all of the Technology Working Groups (TWGs), will facilitate understanding of the Roadmap for the path ahead.

This chapter presents a brief, easy-to-understand summary of the consensus of the Working Groups for each of the technology nodes.

YEAR	*1999*	*2002*	*2005*	*2008*	*2011*	*2014*
TECHNOLOGY NODE (nm)	*180*	*130*	*100*	*70*	*50*	*35*

SYSTEM-ON-A-CHIP

Historically, the Roadmap has emphasized the technological limits of silicon production, leading to the specification of the most complex chips that can be developed in the categories of memory, microprocessor MPU), and ASIC at a particular technology node. With the growing importance of high-volume consumer markets and the ability to integrate almost all aspects of a system design on a single chip, the Roadmap has included an additional vehicle to capture the requirements of this important, emerging area. We refer to this vehicle as a *System-On-a-Chip* (SoC). There are a number of characteristics that distinguish a mainstream SoC, but the main consideration is that it is primarily defined by its performance and cost rather than by technological limits. As a *system*-on-a-chip, these chips are often mixed-technology designs, including such diverse combinations as embedded DRAM, high-performance or low-power logic, analog, RF, and even more esoteric technologies like Micro-ElectroMechanical Systems (MEMS) and optical input/output. In all categories of the Roadmap, design productivity is a key requirement. This is particularly true for the SoC category, where time-to-market for a particular application-specific capability is a key requirement of the

designs. For primarily cost and time-to-market reasons, we expect that product families will be developed around specific SoC architectures and that many of these SoC designs will be customized for their target markets by programming the part (using software, FPGA, Flash, and others). This category of SoC is referred to as a *programmable platform.* The design tools and technologies needed to assemble, verify, and program such embedded SoC's will present a major challenge over the next decade.

DESIGN WORKING GROUP

The advances that enable manufacturing at the aggressive technology nodes of this Roadmap give rise to great challenges in design, verification, and test. Design complexity is increasing superexponentially because of the compounding effects of increased density and number of transistors, increased heterogeneity of design types on a singe chip (such as in SoC designs), and the increasing number of factors that design tools and methods must consider with smaller feature sizes and higher levels of integration. The demands for faster time to market; higher performance digital MPUs and ASICs; mixed-signal and mixed technology designs incorporating analog, RF, MEMS, and others; and parts composed from separately designed IP all produce challenges on various complexity scales. *Silicon complexity* is increased with the much larger numbers of interacting devices and interconnects and the impact of new technologies, new logic families to meet performance goals, and the effects of power and current requirements. *System complexity* is growing not only because of increased system size, but due to SoC designs with a diversity of design styles, integrated passive components, and the increased need to incorporate embedded software. *Design procedure complexity* is also increasing with the growing interaction among design levels, the difficulties of convergence and predictability of the design process, and the growing size and dispersion of design teams—all required for quality, productivity, and time-to-market. *Verification complexity* rises with the need to validate core-based and mixed-technology designs, timing and function together, and behavior at the system level. And the *test complexity* grows greatly at higher speeds, higher levels of integration, and greater design heterogeneity, making external test-through-pins less viable.

TEST WORKING GROUP

The basic requirements are high test reliability (corresponding to low field failure rates) and low test costs. The ability to test for failure modes, such as those associated with the cross-talk caused by high density interconnect, is already essential in nodes above 100 nm. Research in this area must be facilitated. Moreover, testing of embedded mixed analog/digital circuits, and the use of Design-for-Test (DFT) for testing high-speed devices using both low-cost and low-speed testers, present major challenges above 100 nm. Built-In-Self-Test (BIST), which can generate a test pattern and store results within a chip, is a potential solution to both of these problems.

Testing of SoC for nodes below 100 nm is another major issue, and there is a need for the development of a higher-order DFT. Below 100 nm, the potential for the salvage of otherwise unusable chips, using the Built-In-Self-Repair function of memories and logic devices (incorporated in testing processes), will also be explored.

PROCESS INTEGRATION, DEVICES, & STRUCTURES WORKING GROUP

Past trends in DRAM chip size indicate that chip size increased by 1.4× for every four times increase of bit capacity. This progression, if continued further, would make chip sizes too large and lead to problems with the size of lithographic exposure areas and packaging. Accordingly, a model has been proposed in which chip size will now be increased 1.2× for every four times increase of bit capacity. This new model corresponds well with the current trend for a doubling of memory capacity every two years. The deviation from the previous trends in the expansion of memory size, as exemplified by this new model, will necessitate the development of new cell structures, such as open-bit-line cell or cross-point-cell structures, among others, which are characterized by smaller cell sizes relative to the design rules.

For further scaling of MOSFETs, it is necessary to achieve device design for higher performance and minimum variation in product specifications, while effectively addressing the issues associated with gate dielectrics and pn junctions as described in the *Front End Processes* chapter. The introductions of halo doping, as a channel formation technology, and of a high-mobility silicon-germanium epitaxial layer may be

considered potential solutions down to 100 nm. At nodes below 50 nm, the use of novel switching devices, such as quantum-dot or single-electron transistors, may be needed in regions where the statistical variance in the measurements of number and position of impurities becomes significant. New storage devices, such as ferroelectric RAMs (FeRAMs) and MRAMs, which are nonvolatile RAMs, may prove to be viable solutions for memory. For analog and mixed-signal devices, noise problems must be effectively dealt with as the operating voltage becomes lower (2.0–1.5 Volts). At the same time, maintaining capacitor capacity and minimizing parasitic capacitance will be technical challenges upon further scaling of devices. The former problem will be dealt with through adoption of high κ material, while the latter will be effectively resolved by use of low κ dielectrics, copper multi-layer interconnect, SOI substrates, and three-dimensional structures.

In SoC devices with embedded memory, logic, and analog circuits, noise due to interference between different circuit blocks such as digital and analog circuits must be suppressed. In addition, highly integrated processes with excellent cost-performance are required in order to control ever-increasing processing steps and growing chip sizes.

FRONT END PROCESS WORKING GROUP

Technology breakthroughs, in terms of materials and processes, are needed for further scaling because existing materials and technologies are approaching their physical limits. Significant issues include: the use of physically thicker (than silicon dioxide) gate materials to minimize direct tunnel current through the MOSFET gate while maintaining high-capacitance (higher κ); the use of metal gate electrodes to compensate for slower processing speeds caused by depletion in poly-silicon electrodes and boron penetration of the silicon substrate (from the poly-silicon); and methods for forming ultra-thin and low-sheet-resistance pn junctions for higher performance transistors. Moreover, the new materials to be used for gates and dielectrics tend to make the gate etching process more difficult. In addition to CD uniformity and selectivity, etch profiles and line edge roughness must be controlled properly to maintain optimal transistor performance.

Down to the 100 nm node (65 nm gate length), Si_3N_4, unary metal oxides and silicates, with equivalent oxide thickness down to about 1 nm, may be used in MOSFET gate stacks. Raised source/drain, plasma doping and laser annealing methods are candidates for ultra-thin junctions. Additionally, BST may be used as a high κ dielectric for DRAM storage cell scaling, and Ru or RuO_2 may be used for electrodes.

MOSFETs from 65 nm down to 20 nm gate length may require very high κ (>20) gate dielectrics and/or "dual-gate" SOI structures. Vertical MOS may also be used. Open-bit-line cells, cross-point cells and multi-state circuits present good prospects for use as DRAM cell architectures.

Another important breakthrough area is the substrate used in device manufacture. Despite aggressive actions taken to limit chip size, it is generally recognized that at some point in time substrates beyond 300 mm (such as 450 mm) in diameter will need to be introduced in order to manage the manufacturing costs of large chip size devices. The achievement of acceptable cost/performance characteristics of these large substrates constitutes another area where breakthroughs will be needed.

LITHOGRAPHY WORKING GROUP

Scaling must be achieved at reasonable cost and in accordance with the timing technology mentioned above. A 70% reduction from the previous node has typically been achieved within two-three years through shortening of the wavelength of light sources, increased numerical aperture (NA) for optical systems, utilization of half-tone phase-shift masks and other resolution enhancement technologies (RET) such as annular illumination, and the development of high-performance resists. Optical lithography may be extended in the near future through the development of 157 nm technology, which uses F_2 laser light, as well as alternating phase-shift masks and other high-resolution techniques. (Beyond 157 nm, solutions using extreme ultraviolet (EUV), electron projection lithography (EPL), electron-beam direct-write (EBDW), proximity X-ray lithography (PXL) and other "next-generation lithography" (NGL) technologies will have to be developed.) 157 nm light tends to be absorbed by oxygen and organic materials, so there will be a need for oxygen-free exposure equipment, as well as for new resist materials and processes. NGLs generally

employ principles beyond those currently used in "refractive" optical lithography, and innovations will be required in light sources, "optical" systems, masks, resists and almost all other aspects of the technology. Potential solutions at each node are listed below as follows:

NODE	*POTENTIAL SOLUTIONS*
180 nm	KrF
130 nm	KrF+RET, ArF
100 nm	ArF+ RET, F2, EPL, PXL, IPL
70 nm	F2+RET, EPL, EUV, IPL, CBDW
50 nm	EUV, EPL, IPL, CBDW
35 nm	EUV, IPL, EPL, CBDW, Innovative Technology

Mask-making capability and cost escalation have become the major limiter to lithography progress. With the roadmap acceleration over the past three years, the mask industry has fallen behind the requirements of the chipmakers. Mask equipment and process capabilities for complex OPC and PSM are just becoming available for the 180 nm node production requirements. These capabilities are being pushed beyond their limits for 130 nm to 100 nm development. Mask processes for advanced technologies (157 nm, XRL, EUV, EPL, and IPL) are in research and development.

The difficult challenges common to all nodes include controlling critical dimensions, overlays, and defect density. These challenges are not only caused by "relative scaling" but are increasingly related to "absolute sizes," especially at nodes under 100 nm. For example, as actual processing dimensions are getting close to the sizes of photoresist molecules and other physical distances associated with exposure and development, existing techniques for measuring sizes, positions, and defects are becoming difficult to use (as described in detail in the *Metrology* and *Defect Reduction* chapters). In addition, the displacement of the equipment's structural parts due to heat and vibration is no longer negligible.

INTERCONNECT WORKING GROUP

The function of an interconnect or wiring system is to distribute clock and other signals and to provide power/ground to and among the various circuits/systems functions on a chip. The fundamental development requirement for interconnect is to meet the high-speed transmission needs of chips despite further scaling of feature sizes. As supply voltage is scaled or reduced, cross-talk has become an issue for all clock and signal wiring levels; the near term solution adopted by the industry is the use of thinner copper metallization to lower line-to-line capacitance. Although copper-containing chips were introduced in 1998, copper must be combined with new insulator materials. The introduction of new low κ dielectrics, CVD metal/barrier/seed layers, and additional elements for SoC, provide significant process and process integration challenges. Interfaces, contamination, adhesion, leakage, and thermal budget, confounded by the number of wiring levels for interconnect, ground planes and other passive elements, create a difficult to manage complexity. Further, although the technical product driver for the smallest feature size remains the dynamic memory chip, an emerging classification of chips, the system-on-a-chip, or SoC, will challenge microprocessors for increased complexity and decreased design rules. Managing this rapid rate of materials introduction and the concomitant complexity represents the overall near term challenge. For the long term, material innovation with traditional scaling will no longer satisfy performance requirements. New design or technology solutions (such as coplanar waveguides, free space RF, optical interconnect) will be needed to overcome the performance limitations of traditional interconnect.

FACTORY INTEGRATION WORKING GROUP

Factory Integration's basic needs include improved factory productivity through cost reduction; adaptability in the face of change; improved reliability and availability; and shorter production cycle time. In the near term, a focus has been placed on the wafer processing aspect of semiconductor fabrication and on comparisons and contrasts between high-volume/high-mix and high-volume/low-mix production lines. The "management of complexity" is considered to be a fundamental issue that must be further examined. The broad concept of complexity represents the introduction of a wide variety of new products and technologies;

the diversification of processes; the use of large-diameter wafers; and increased reliance on factory automation and systematization. Two subordinate issues, "factory optimization" to reduce costs and shorten production cycle time, and the "flexibility/extendibility" required to accommodate multiple generations of products and larger-scale factory operations, have also been addressed. Factory operations is the umbrella under which the requirements for production cycle time and the operating rates for production lines, among other things, can be examined. Assuming a high-volume/high-mix production line, the required production cycle time, by mask layer, for each of the technology nodes is determined as follows:

TECHNOLOGY NODE (nm)	180	130	100	70	50	35
Non Hot Lot Production Period per Mask Layer (days)	1.8	1.6	1.4	1.3	1.2	1.1
Hot Lot Production Period per Mask Layer (days)	0.9	0.85	0.8	0.75	0.7	0.65

Direct and single-wafer transport with realtime dispatching is needed by the 100 nm node. In addition, for manufacturing equipment, a reduction of non-production (dummy, conditioning, and test) wafers is needed.

ASSEMBLY & PACKAGING WORKING GROUP

The reduction in package size and the effective dissipation of heat are basic needs. In logic chips with 800 pins or higher, the conventional package design (in which terminals are present only on the periphery of the chip) is inappropriate, since the chip area must be increased for installation of the terminals alone. Instead, the area array configuration must be adopted because the package has terminals arranged in grid form on the entire surface of the chip. In order to achieve further reduction in size of packages and high density boards at low cost, flip-chip connection in ball grid arrays (BGAs) is expected to produce good results. Conventional ceramic substrates will have to be replaced with low-cost organic materials for most applications. Required performance characteristics include lower hygroscopy, higher CTE matching to chips, and higher glass transition temperatures, as necessitated by the use of lead-free solder for environmental reasons. Metal lines on the substrate must accommodate much finer-pitch terminals and fan-out wiring. Moreover, improved adhesion and moisture resistance for increased mechanical strength of connections, as well as improved hygroscopy for increased reliability, will be needed for the underfill materials for flip chips. There is also a need for the establishment of superior thermal design and simulation procedures for packages and devices with more effective heat dissipation characteristics and for the development of test methods which provide an assurance of quality and reliability for high-density substrates and semiconductor packages without relying on probes. The development of technologies for the integration of area array/flip chip connections with fine-pitch ball grid arrays (FBGA) / chip-size packages (CSP) is a prerequisite for further reduction, and the use of ultra- fine fan-out wiring will be essential.

ENVIRONMENT, SAFETY, & HEALTH WORKING GROUP

Chemical materials and equipment management includes provision for the dissemination of information concerning the environment, safety, and health to engineers prior to the use of new chemical compounds and materials to prevent problems in these areas following the release of new technologies and products. Efforts to reduce energy consumption in semiconductor production factories and facilities help to eliminate a major cause of global warming and mitigate the factors contributing to climatic change. Worker protection programs are designed to improve existing factories, facilities, safety equipment, training, and education to safeguard the safety and health of workers. Resource conservation programs serve to conserve water, energy, chemical compounds, and materials and other raw materials, and to promote the development of substitutes for toxic materials and the recycling of industrial wastes. Design and management methods will focus on the identification of materials and processes that minimize environmental pressures and the risks to health and safety.

For the nodes of 70 nm or below, the use of new chemical substances in semiconductor fabrication processes is highly likely. There is a need, therefore, for the development of methodologies for the prompt provision of information on environmental effects from a comprehensive examination of any new chemicals. Given the fact that there is increasing societal demand for resource conservation and for effective measures to counter

climatic change, the development of substitute materials with reduced environmental effects and efficient recycling technologies will be essential.

DEFECT REDUCTION WORKING GROUP

The product yield is one of the basic indicators of the completeness of a semiconductor technology. To maintain a high yield, defect reduction is a continuing challenge that is common to all nodes. With progress between nodes, devices will become ever more complex. In reality, the amount of data that must be processed for correct trouble-shooting performance is 80 times higher at the 50 nm node than it is at the 180 nm node. The requirements for defect analysis systems, including defect detection equipment, have become increasingly stringent. This has made defect reduction a far more difficult proposition.

The accuracy of defect inspection equipment for patterned wafers based on conventional technology (ultraviolet light) has already proved inadequate in meeting the requirements for mass production at the 130 nm node. There is no inspection equipment capable of detecting and analyzing defects in high-aspect-ratio circuit patterns. Moreover, the classification speed for defects; the number of defects that can be handled; and the speed of chemical element analysis will also be inadequate; thereby, making it extremely difficult to identify the causes of defects. Accordingly, new defect detection equipment must be developed to satisfy the requirements for lower defect rates.

METROLOGY WORKING GROUP

Even at the 180 nm node, current metrology capability does not meet precision and accuracy requirements for many measurements done during device manufacturing. Aggressive scaling is accelerating the gaps found at the 130 nm node and beyond. The roadmap expresses a strong concern about the gap in capability for sub 100 nm wafer and mask level critical dimension and other inline microscopy measurements. Mask metrology needs are more difficult to meet due to optical proximity correction and phase shift mask structures, and thus they receive an expanded coverage. Future challenges come from the high aspect ratio structures, ultra thin layers, ultra-shallow junctions combined with the use of new materials for transistor, capacitor, and on-chip interconnect. Interfaces between materials require some form of process control. The move toward greater use of measurement data for automated process control and the use of clustered or *in situ* metrology has come to be known as "Integrated Metrology". There is a need to develop measurement technology for Integrated Metrology. Characterization and metrology for contamination control for the 70 nm node and beyond will be a significant concern.

MODELING & SIMULATION WORKING GROUP

The focus of modeling and simulation is on improvements in the efficiency of development as well as of production. Optimal processes, electrical characteristics, heat damage, and the reliability of devices will be forecast based on theoretical models in order to optimize process/device/circuit designs. In so doing, cost reductions of 25% and 35% may be achieved, respectively, at the 130 nm and 100 nm nodes. In addition to the improvement of existing models, new models for processes in lithography, etching, CVD, and other technologies will have to be developed as scaling progresses down to the 100 nm node. Greater understanding of plasmas, wafer surface reactions, exposure/development of photoresists, and other complex reactions will also be necessary. In addition, improvements in grid (mesh) generation and numerical calculation algorithms will be required to improve calculation speed and accuracy. Below 100 nm, better simulation techniques for newly introduced gate materials, including models of the dielectric constant, the tunneling phenomena and the reliability, must be addressed. In contrast, nanometer devices will have pronounced quantum effects in addition to the obvious effects of discrete atoms in impurities. Thus, precise modeling of the various phenomena observed in processes at the electron level must be established. In contrast to conventional models, which assume the physical continuity of materials, alternative solutions at nodes below 100 nm may include the adoption of discrete modeling procedures: for example, the Monte Carlo methods, in which atoms and electrons are treated as particles, or the quantum dynamic calculation methods, which are based on solving Schroedinger's equation.

DIFFICULT CHALLENGES TABLES

DESIGN

Table C Design Difficult Challenges

Five Difficult Challenges ≥ 100 nm / Through 2005	*Summary of Issues*
Silicon complexity	Large numbers of interacting devices and interconnects
	Impact of signal integrity, noise, reliability, manufacturability
	Power and current management; voltage scaling
	Need for new logic families to meet performance challenges
	Atomic-scale effects
	Alternative technologies (such as copper, low κ dielectric, SOI)
System complexity	Embedded software as a key design problem
	System-on-a-chip design with a diversity of design styles (including analog, mixed-signal, RF, MEMS, electro-optical)
	Increased system and function size
	Use of open systems and incorporation into global networks
	Integrated passive components
Design procedure complexity	Convergence and predictability of design procedure
	Core-based, IP-reused designs and standards for integration
	Large, collaborative, multi-skilled, geographically distributed teams
	Interacting design levels with multiple, complex design constraints
	Specification and estimation needed at all levels
	Technology remapping or migration to maintain productivity
Verification and analysis complexity	Formal methods for system-level verification
	System-on-a-Chip specification
	Early high-level timing verification
	Core-based design verification (including analog/mixed-signal)
	Verification of heterogeneous systems (including mixed-signal, MEMS)
Test/testability complexity	Quality and yield impact due to test equipment limits
	Test of core-based designs from multiple sources (including analog, RF)
	Difficulty of at-speed test with increased clock frequencies
	Signal integrity testability
Five Additional Difficult Challenges < 100 nm / Beyond 2005	
Silicon complexity	Uncertainty due to manufacturing variability
	Uncertainty in fundamental chip parameters (such as signal skew)
	Design with novel devices (multi-threshold, 3D layout, SOI)
	Soft errors
System complexity	Total system integration including new integrated technologies (such as MEMS, electro-optical, electro-chemical, electro-biological)
	Design techniques for fault tolerance
	Embedded software and on-chip operating system issues
Design procedure complexity	True one-pass design process supporting incremental and partial design specification
	Integration of design process with manufacturing to address reliability and yield
Verification and analysis complexity	Physical verification for novel interconnects (optical, RF, 3D) at high frequency
	Verification for novel devices (nanotube, molecular, chemical)
Test/testability complexity	Dependence on self-test solutions for SoC (RF, analog)
	System test (including MEMS and electro-optical components)

κ—dielectric constant *SOI—silicon on insulator* *IP—intellectual property*

TEST & TEST EQUIPMENT

Table D Test and Test Equipment Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥ 100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
BIST and DFT	Test equipment costs will rise toward $20M and wafer yields may suffer without DFT and BIST. DFT required for at-speed test with a low-speed tester. Tools required for inserting DFT and BIST and estimating cost. Analog BIST needed. Access to SoC cores needed when using DFT and BIST.
DUT to ATE interface	A major roadblock will be the need for high-frequency, high pin-count probes and test sockets; research and development is urgently required to lower inductance and cost. Increasing pincounts lead to larger test heads and longer I/O round-trip delays (RTD). This problem can be avoided using two transmission lines, but I/O pins must then drive 25 ohms. Power and thermal management problems Nonuniform wafer temperatures and the requirement for active DUT temperature control Simulation needed for the path from the device through the package to the ATE pin electronics Interface circuits must not degrade ATE accuracy or introduce noise. Especially for high-frequency differential DUT I/O Faster, multi-socket, automatic package handlers are required.
Mixed-signal instruments	IC manufactures must partner with the ATE suppliers to ensure ATE capability will match the mixed-signal requirements These will require more bandwidth, higher sample rates, and lower noise. Testing chips containing RF and audio circuits will be a major challenge if they also contain large numbers of noisy digital circuits.
Failure analysis	3D CAD and FA systems for isolation of defects in multi-layer metal processes New fault models, such as for crosstalk. Automatic test generators for fault diagnosis. CAD software for fault diagnosis using new fault models to support DFT and BIST requirements.
Test development.	Automatic test program generators to reduce test development time Test standards, such as STIL , IEEE P1500 Reuse of core tests for SoC to reduce test development time Simulation of the ATE, interface, and DUT to avoid test development on expensive ATE. (virtual testing) Data management needs to be integrated into test program development
FIVE DIFFICULT CHALLENGES <100 nm / BEYOND 2005	
DUT to ATE interface	Optical probing techniques Full wafer test Power and thermal management problems, especially with 300 mm wafers and increasing parallel test sites Contactless probing using BIST (see DFT/BIST section)
SoC test methods	New DFT techniques (SCAN and BIST have been the mainstay for over 20 years). New test methods for control and observation are needed. Tests will need to be developed utilizing the design hierarchy. Analog BIST Logic BIST for new fault models and failure analysis Deterministic self-test instead of pseudo random test patterns EDA tools for DFT selection considering cost/performance issues
MEMS, sensors, and new IC technologies	Develop new test methods.
New burn-in techniques.	Research is required. Test during burn-in using burn-in DFT/BIST capability; low-cost, massive parallel test during burn-in
Failure analysis.	Realtime analysis of defects in multi-layer metal processes New fault models, such as noise New CAD tools for diagnosis Failure analysis for analog devices

FA—failure analysis
SCAN—A test method in which test patterns are scanned in and out of the DUT.
STIL—IEEE Standard Test Interface Language

PROCESS INTEGRATION, DEVICES, & STRUCTURES

Table E Process Integration, Devices, and Structures Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
Meeting device performance targets with available gate stack materials	Production worthy high κ dielectrics and compatible gate materials will not be available.
Function integration at low V_{dd}	Crosstalk, substrate noise, and device performance difficult to optimize simultaneously at high clock rates and low V_{dd}.
Managing power, ground, signal, and clock on multilevel coupled interconnect	Despite the use of low κ dielectrics, interconnect scaling is increasing coupling capacitance, crosstalk and signal integrity issues. Power, clock, and ground distribution will consume an increasing fraction of available interconnect.
Management of increasing reliability risks with the rapid introduction of new technologies.	Inadequate identification and modeling of failure modes in new materials, new operating regions (such as tunneling) and new SoC technologies (such as MEMS)
Integration of precision passive elements	Maintaining high Q, low noise, and tolerances of discrete components.
FIVE DIFFICULT CHALLENGES <100 nm / BEYOND 2005	
Overcoming fundamental scaling limits for current device structures	Switching drive, noise margin, material properties, and reliability will limit performance improvements from scaling
Integration choices for system-on-a-chip	Cost-effective process integration of many functions on a single chip.
Atomic level fluctuations and statistical process variations	Possible reduction of yield and performance below desired levels due to unacceptable statistical variations.
Design for manufacturability, reliability, and performance.	Inadequate smart design tools that incorporate integration challenges in process control, proximity effects, reliability, performance, and others
Low-power, low-voltage, high-performance, and reliable nonvolatile memory element	NVM program and erase require voltages that are incompatible with highly scaled low-voltage devices

FRONT END PROCESSES

Table F Front End Process Difficult Challenges

DIFFICULT CHALLENGES THROUGH 2005, LOGIC GATE LENGTH > 65 nm	*SUMMARY OF ISSUES*
Nitride Derivatives and High κ Gate Stacks	Effective oxide thickness ~/>1.2 nm for nitride derivatives, ~/< 1.2 nm for high κ Achieve optimal channel mobility >95% of SiO_2 Minimize gate leakage mechanisms to achieve ~/<1A/cm^2 for high-performance logic and ~/<0.001 A/cm^2 for system LSI Control Boron penetration. Minimize gate electrode depletion, e.g., polysilicon depletion Chemical compatibility of dual metal with appropriate work functions
DRAM Storage Cells (Stack and Trench Capacitors)	Implementation of Ta_2O_5, BST, etc., with associated compatible electrode materials Capacitor structures that meet (DRAM ½ Pitch)^2 scaling Trench and stack capacitor scaling to <100 nm
Ultra-Shallow Junctions (USJ) with Standard Processing	Achievement of lateral and depth abruptness Achievement of low series resistance, <10% of channel R_s Annealing technology to achieve ~/<300Ω/□ at ~/<30 nm X_j
L_{eff} Control	Etch CD control and selectivity Sidewall etch control Microloading effects of dense/isolated lines Halo/pocket implant optimization Overall thermal cycle control
Metrology	Physical, electrical and chemical measurement and characterization of gate dielectric, electrodes, USJ, etc.
DIFFICULT CHALLENGES BEYOND 2005 AND AFTER, LOGIC GATE LENGTH ≤ 65 nm	
Ultra High κ Gate Stack	Effective oxide thickness <0.9 nm Chemical compatibility of dual metal with appropriate work functions Acceptable channel mobility Thermal budget and dielectric stability CD Control Gate Leakage ~/<1A/cm^2 for high performance logic, ~/<0.001 A/cm^2 for system LSI Cost-effective CMOS integration
Memory Storage Cell	Will an alternate storage cell supplant conventional memory? Ultra high κ capacitor dielectric (Epi BST) Are trench and stack capacitor structures viable at or below 70 nm while meeting (DRAM ½ Pitch)^2 scaling?
Alternate and Ultra-scaled Transistor Structures	CMOS structure: raised S/D, replacement gate process flow, CD control, CMOS integration, and others New device structures beyond planar CMOS: pillar, wraparound gate, and others.
Integration of Silicon Compatible Materials	CoO of large wafers (>300 mm): epi, SOI, Si:Ge Development of compatible high κ dielectric materials Development of compatible dual metal electrodes Development of material compatible cleaning processes
Metrology	Physical, chemical and electrical measurement and characterization of new dielectric, electrodes, and ultra-shallow, ultra-abrupt, dopant distributions

LITHOGRAPHY

Table G Lithography Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥ 100 nm THROUGH 2005	*SUMMARY OF ISSUES*
Optical mask fabrication with resolution enhancement techniques for ≤ 130 nm and post-optical mask fabrication	Development of commercial mask manufacturing processes to meet requirements of Roadmap options (such as 157 nm substrates and films; defect free multi-layer substrate or membranes) Development of equipment infrastructure (writers, inspection, repair) for relatively small market
Lithography technology consensus (193 nm + RET, 157 nm, NGL)	Narrowing of Roadmap options for 100–50 nm nodes. Achieving global consensus among technology developers and chip manufacturers
Cost control and return on investment (ROI)	Achieving constant/improved throughput with larger wafers Development of cost-effective resolution enhanced optical masks and post-optical masks including an affordable ASIC solution, such as low costs masks. Achieving ROI for industry (chipmakers, equipment and material suppliers, and infrastructure) on large investments necessary for Roadmap acceleration, especially single node solutions at 100 nm and below.
Gate CD control improvements	Development of processes to control minimum feature size to less than 7 nm, 3 sigma
Overlay improvements	Development of new and improved alignment and overlay control methods independent of technology option
FIVE DIFFICULT CHALLENGES < 100 nm BEYOND 2005	
Mask fabrication and process control	Development of commercial mask manufacturing processes to meet requirements of Roadmap options (such as 157 nm substrates and films; defect free multi-layer substrate or membranes) Development of equipment infrastructure (writers, inspection, repair) for relatively small market Development of mask process control methods to achieve critical dimension, image placement, and defect density control below 100 nm nodes
Metrology and defect inspection	R&D for critical dimension and overlay metrology, and patterned wafer defect inspection for defects < 40 nm
Cost control and return on investment (ROI)	Development of innovative technologies, tools, and materials to maintain historic productivity improvements Achieving constant/improved throughput with post-optical technologies Achieving ROI for industry (chipmakers, equipment and material suppliers, and infrastructure) on large investments necessary for Roadmap acceleration, especially single node solutions at 100 nm and below.
Gate CD control improvements	Development of processes to control minimum feature size to less than 5 nm, 3 sigma, and reducing line edge roughness
Overlay improvements and measurements	Development of new and improved alignment and overlay control methods independent of technology option

INTERCONNECT

Table H Interconnect Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥ 100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
New materials	Rapid introduction of materials/processes are necessary to meet resistivity and low/high κ targets and address SoC needs.
Reliability	New materials create new chip reliability (electrical, thermal and mechanical) exposure. Detecting, testing, modeling and control of failure mechanisms will be key.
Process integration	Combinations of materials (Cu, Al, low κ, high κ, ferroelectrics, new barriers/nucleation layers) along with multiple technologies used in SoC applications open new integration challenges.
Dimensional control	Multi-dimensional control of interconnect features is necessary for circuit performance and reliability. Multiple levels, new materials, reduced feature size and pattern dependent processes create this challenge.
Interconnect process with low/no device impact	As feature sizes shrink, interconnect processes must be compatible with device roadmaps. Low plasma damage, contamination and thermal budgets are key concerns.
FIVE DIFFICULT CHALLENGES <100 nm / BEYOND 2005	
Dimensional control and metrology	Multi-dimensional control and metrology of interconnect features is necessary for circuit performance and reliability.
Aspect ratios for fill and etch	As features shrink, etching and filling high aspect ratio structures will be challenging, especially for DRAM. Dual damascene metal structures are also expected to be difficult.
New materials and size effects	Continued introductions of materials/processes are expected. Microstructural and quantum effects become important.
Solutions beyond copper and low κ	Material innovation with traditional scaling will no longer satisfy performance requirements. Accelerated design, packaging and unconventional interconnect innovation will be needed.
Process integration	Combinations of materials along with multiple technologies used in SoC applications are a continued challenge. Plasma damage, contamination and thermal budgets are key concerns.

FACTORY INTEGRATION

Table I Factory Integration Difficult Challenges

DIFFICULT CHALLENGES	SUMMARY OF ISSUES
Complexity Management	Rapidly changing business needs and globalization trends • Increasing rate of new product and technology introductions • Globally disparate factories run as single "virtual factory" • Need to meet regulations in different geographical areas Increasing process and product complexity • Explosive growth of data collection/analysis requirements • Increasing number of processing steps • Multiple lots in a carrier Larger wafers and carriers driving ergonomic solutions • Increasing expectations for material handling automation systems Increased reliance on factory systems • Multiple system interdependencies • Co-existence of new factory systems with existing (legacy) systems
Factory Optimization	Meet customer ontime delivery • Balanced throughput and cycle time • Reduce time to ramp factories, products, and processes Improve Overall Factory Effectiveness (OFE) • Improve all Factory Integration thrust areas Improve factory yield • Control production equipment and factory processes to reduce parametric variation Reduce product and operation cost • Minimize waste and scrap and reduce the number of nonproduct wafers Satisfy all local, state and federal regulations.
Extendibility, Flexibility, and Scalability	Reuse of building, production and support equipment, and factory systems • Across multiple technology nodes • Across a wafer size conversion Factory designs that support rapid process and technology changes and retrofits • Understand up-front costs to incorporate EFS • Determine which EFS features to include and not to include • Minimize downtime to on-going operations Increase tighter ESH/Code requirements Increase purity requirements for process and materials

ASSEMBLY & PACKAGING

Table J Assembly & Packaging Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥ 100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
Improved organic substrates for high I/O area array flip chip	T_g compatible with Pb free solder processing ε_r approaching 2.0 Improved area array escape wireability at low cost Lower CTE approaching 6.0 ppm/°C Low moisture absorption High density substrate test
Improved underfills for high I/O area array flip chip Reliability limits of flip chip on organic substrates	Improved manufacturability (fast dispense/cure), better interface adhesion, lower moisture absorption, flow for dense bump pitch Reliability up to 170°C for automotive Comprehensive parametric knowledge of packaging components (chip size, underfill, substrate, heat sink, UBM/bump)
Coordinated design tools and simulators to address chip, package, and substrate complexity	Physical design Thermal/thermo-mechanical Electrical (power disturbs, EMI, signal integrity associated w/higher frequency/current, lower voltage, mixed-signal co-design) Commercial EDA supplier support
System reliability impact of Cu/low κ on packaging	Bump and underfill technology to assure low κ dielectric integrity Mechanical strength of dielectrics Interfacial adhesion
Cost effective cooling for cost-performance and high-performance sectors	Meeting 40°C above ambient temperature Localized on-chip power density
DIFFICULT CHALLENGES < 100 nm / BEYOND 2005	
Close the gap between the substrate technology and the chip	Low-loss, low ε_r materials Cost/unit area constant (cost/layer decreasing) Interconnect density scaled to silicon System level solution that optimizes reliability and cost
"System level" view of integrated chip, package, and substrate needs	Commercial EDA supplier support
Ultra high frequency design for high density digital and mixed-signal packaging	Efficient design and simulation tools Integrated analog to digital design tools
Manufacturability and reliability of large body packages	Substrate flatness Co-planarity of chip-to-package and package-to-board

CTE—coefficient of thermal expansion
EMI—electromagnetic interference
UBM—under bump metallurgy
EDA—electronic design automation

ENVIRONMENT, SAFETY, AND HEALTH

Table K Environment, Safety, and Health Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥ 100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
Chemicals, Materials and Equipment Management	*Chemical Data Collection* Need to document and make available environment, safety, and health characteristics of chemicals. *New Chemical Assessment* Need for quality rapid assessment methodologies to ensure that new chemicals can be utilized in manufacturing, while protecting human health, safety, and the environment without delaying process implementation. *Environment Management* Need to develop effective management systems to address issues related to disposal of equipment, and hazardous and non-hazardous residue from the manufacturing process.
Climate Change Mitigation	*Reduce Energy Use Of Process Equipment* Need to design energy efficient larger wafer size processing equipment. *Reduce Energy Use Of The Manufacturing Facility* Need to design energy efficient facilities to offset the increasing energy requirements of higher class clean rooms. *Reduce High Global Warming Potential (GWP) Chemicals Emission* Need ongoing improvement in methods that will result in emissions reduction from GWP chemicals.
Workplace Protection	*Equipment Safety* Need to design ergonomically correct and safe equipment. *Chemical Exposure Protection* Increase knowledge base on health and safety characteristics of chemicals and materials used in the manufacturing and maintenance processes, and of the process byproducts; and implement safeguards to protect the users of the equipment and facility.
Resource Conservation	*Reduce Water, Chemicals And Materials Use* Requirements for large amounts of water, chemicals, and materials limit sustainable growth. *Waste Recycle* Increase in resource use as the result of increasing process complexity will require that efficient waste recycling methods be developed.
ESH Design and Measurement Methods	*Evaluate and Quantify ESH Impact* Need integrated way to evaluate and quantify ESH impact of process, chemicals, and process equipment, and to make ESH a design parameter in development procedures for new equipment and processes.
FIVE DIFFICULT CHALLENGES < 100 nm / BEYOND 2005	
Chemicals, Materials and Equipment Management	*Chemical Use Information* Rapid introduction of chemicals and materials into new process requires the understanding of process fundamentals in order to reduce ESH impacts.
Climate Change Mitigation	*Reduce Energy Use* The importance of reducing energy use for climate change will grow. *Reduce High GWP Chemicals Emissions* No known alternatives and international regulatory pressure to reduce emissions of GWP chemicals.
Workplace Protection	*Equipment Safety* Need ergonomic principles integrated into the processing and wafer moving equipment for both operation and maintenance aspects, and into the overall manufacturing facility.
Resource Conservation	*Reduce Water, Energy, Chemicals And Materials Use* Need resource efficient processing and facility support equipment and improved water reclaim and recycling methods. Emphasis on resource sustainability will grow.
ESH Design and Measurement Methods	*Evaluate and Quantify ESH Impact* Need integrated ESH design in development of new equipment and processes.

DEFECT REDUCTION

Table L Defect Reduction Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥ 100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
Yield Models—Random, systematic, parametric, and memory redundancy models must be developed and validated to correlate process induced defects, equipment generated particles and product/process measurements to yield	Correlated process-induced defects (PID), particles per wafer per pass (PWP), product inspections, and *in situ* measurements Sampling and statistical issues with ultra-small populations Impact of within-wafer variations on yield predictions Development of parametric yield loss models
High Aspect Ratio Inspection—High-speed, cost-effective tools must be developed that rapidly detect defects associated with high-aspect ratio contacts/ vias/trenches, and especially defects near/at the bottom of these features.	Poor transmission of energy into bottom of via and back out to detection system Large number of contacts and vias per wafer
Trace Impurity Specifications—Test structures and advanced modeling are needed to determine the effect of trace impurities on device performance, reliability and yield.	The need to better understand the impact of trace impurities is expected to become more important as new materials and processes are introduced.
Defect Sourcing—Automated, intelligent analysis and reduction algorithms that correlate facility, design, process, test and WIP data must be developed to enable rapid root cause analysis of yield limiting conditions.	Circuit complexity grows exponentially and the ability to rapidly isolate failures on non-arrayed chips is needed. Automated data reduction algorithms must be developed to source defects from multiple data sources (facility, design, process and test.)
Nonvisual Defects—Failure analysis tools and techniques are needed to enable localization of defects where no visual defect is detected.	Many defects that cause electrical faults are not detectable inline.
FIVE DIFFICULT CHALLENGES < 100 nm / BEYOND 2005	
Yield Models—Defect "budgeting" must comprehend greater parametric sensitivities, complex integration issues, greater transistor packing, ultra-thin film integrity, etc.	Development of test structures for new technology nodes Modeling complex integration issues Ultra-thin film integrity modeling Better methods of scaling front end process complexity that considers increased transistor packing density
Defect Detection—Detection and simultaneous differentiation of multiple killer defect types is necessary at high capture rates and throughputs	Existing techniques tradeoff throughput for sensitivity, but at predicted defect levels, both throughput and sensitivity are necessary for statistical validity. Ability to detect particles at critical size do may not exist
Escalating Inspection Costs—Equipment must effectively utilize realtime process and contamination control through integrated *in situ* process and product metrology	Equipment must effectively utilize real time process and contamination control through *in situ* sensors. Inspection must occur during yield ramp and by exception only in a production environment.
Defect Characterization—Defect data must include size, shape, composition, location all independent of "background," for accelerated yield learning	Defect characteristic data will be necessary to enable continued yield learning. Inline defect detection data must include size, shape, composition, and so on., all independent of location and topology. Test structures will have to be developed that emulate design to process and process integration issues.
Defect Free Intelligent Equipment—Advanced modeling (chemistry/contamination), materials technology, software and sensors are required to provide robust, defect-free process tools that predict failures/faults and automatically initiate corrective actions prior to defect formation.	Advanced modeling (chemistry/contamination), materials technology, software and sensors are required to provide robust, defect-free process tools that predict failures/faults and automatically initiate corrective actions prior to defect formation Development of advanced low defect surface preparation techniques

METROLOGY

Table M Metrology Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥ 100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
Factory level and company wide metrology integration for *in situ* and inline metrology tools; continued development of robust sensors and process controllers; and data management that allows integration of add-on sensors	Standards for process controllers and data management must be agreed upon. Conversion of massive quantities of raw data to information useful for enhancing the yield of a semiconductor manufacturing process. Better sensors must be developed for trench etch end point, ion species/energy/dosage (current), and wafer temperature during RTA.
Impurity detection (particles, oxygen, and metallics) at levels of interest for starting materials and reduced edge exclusion for metrology tools	Existing capabilities will not meet Roadmap specifications. Very small particles must be detected and properly sized. Detectivity of trace metals in bulk silicon or in the top silicon layer of SOI (silicon on insulator) must be enhanced.
Measurement of the frequency-dependent dielectric constant of low κ interconnect materials at 5xto 10x base frequency.	Equipment, procedures, and test structures need to be reduced to practice and applied to low κ interconnect materials that account for clock harmonics, skin effects, cross-talk, and anisotropy of materials.
Control of high-aspect ratio technologies such as damascene challenges all metrology methods.	New process control needs are not yet established. For example, 3-dimensional (CD and depth) measurements will be required for trench structures in new, low κ dielectrics.
Measurement of complex material stacks	Reference materials and standard measurement methodology for new, high κ gate and capacitor dielectrics with interface layers, thin films such as interconnect barrier and low κ dielectric layers, and other process needs. Optical measurement of gate and capacitor dielectric averages over too large an area and needs to characterize interfacial layers. The same is true for measurement of barrier layers.
ADDITIONAL DIFFICULT CHALLENGES < 100 nm / BEYOND 2005	
Nondestructive, production worthy wafer and mask level microscopy for critical dimension measurement, overlay, defect detection, and analysis	Surface charging and contamination interfere with electron beam imaging. CD measurements must account for side wall shape. CD for damascene process may require measurement of trench structures.
Standard electrical test methods for reliability of new materials, such as ultra-thin gate and capacitor dielectric materials, are not available.	The wearout mechanism for new, high κ gate and capacitor dielectric materials is unknown.
Statistical limits of sub-70 nm process control	Controlling processes where the natural stochastic variation limits metrology will be difficult. Examples are low-dose implant, thin gate dielectrics, and edge roughness of very small structures.
3D dopant profiling	The dimensions of the active area approach the spacing between dopant atoms, complicating both process simulation and metrology. Elemental measurement of the dopant concentration at the requested spatial resolution is not possible.
Production worthy, physical inline metrology for transistor processes that provides SPC required to achieve consistent electrical properties	Presently, the combined physical metrology for gate dielectric, CD, and dopant dose and profile is not adequate for sub-70 nm design rules.

SPC—statistical process control

MODELING & SIMULATION

Table N Modeling and Simulation Difficult Challenges

DIFFICULT CHALLENGES ≥100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
High frequency circuit modeling (>1GHz)	Efficient simulation of full-chip interconnect delay High frequency circuit models including non-quasi-static, gate RLC, substrate noise, QM effects Accurate 3D interconnect model; inductance effects
Modeling of ultra-shallow junctions	Diffusion parameters (such as from first principles calculations) for As, B, P, Sb, In, Ge Interface effects on point defects and dopants Activation models (In, As, B); metastable states Implant damage, amorphization, re-crystallization
Unified package/die-level models	Unified package/chip-level circuit models Integrated treatment of thermal, mechanical, electrical effects
Model thin film and etch variation across chip/wafer (Equipment/topography)	Reaction paths and rate constants; reduced models for complex chemistry Plasma models; linked equipment/feature models CMP (full wafer and chip level) Pattern dependent effects
Model alternative lithography technologies	Resolution enhancement; mask synthesis (OPC, PSM) Predictive resist models 248 versus 193 versus 157 evaluation and tradeoffs Next-generation lithography system models
Reliability models for circuit design and technology development	Circuit and device level transistor reliability: oxide TDDB, hot carrier, electromigration, NVM reliability, SER, ESD, latch-up
Model new interconnect materials and interfaces	Electromigration (physical), grain structure, diffusion barriers, metallurgy, low κ dielectric materials
DIFFICULT CHALLENGES <100 nm / BEYOND 2005	
Gate stack models for ultra-thin dielectrics	Electrical and processing models for alternate gate dielectrics, and alternate gate materials (such as metal) Model epsilon, surface states, reliability, breakdown and tunneling from process conditions
Nano-scale device modeling	New device concepts (using quantum effect) beyond traditional MOS; single electron transistors, effect of single dopants, etc.
Atomistic process modeling	Accurate atomic scale models for process integration

International Technology Roadmap for Semiconductors
1999 Edition

Overall Roadmap Technology Characteristics
&
Glossary

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OVERALL ROADMAP TECHNOLOGY CHARACTERISTICS

OVERVIEW

The Overall Roadmap Technology Characteristics (ORTC) tables provide a consolidated summary of the key technology metrics. As described in the Introduction, the year header on the tables may refer to different points in the development/life cycle of integrated circuits (ICs) characterized by this technology, depending on the individual line item metric. However, unless otherwise specified for a line, the default year header still refers (as in previous Roadmaps) to the year when product shipment first exceeds 10,000 units of ICs from a manufacturing site using "production tooling."

The ORTC tables are created early in the Roadmap process and are used as the basis for initiating the activities of the Technology Working Groups in producing their detailed chapters. The ORTC tables were also used throughout the renewal effort of the Roadmap as a means of providing synchronization among the TWGs by highlighting inconsistencies between the specific tables. As a result, the ORTC tables went through several iterations until the Roadmap document was completed. The metric values of the ORTC tables can be found throughout the Roadmap in greater detail in each Technology Working Group chapter. Additionally, an ORTC glossary is provided as an appendix.

The new tables include an unprecedented level of cross-TWG and international coordination and consensus building to develop underlying models of trends and to reach agreement on target metrics. The ORTC tables have also expanded in line items compared to the 1997 NTRS. The expansion is due to the addition of several line items, which clarify the underlying models and communicate additional details of the interrelationships between technology areas.

ROADMAP TIMELINE

The timing at which future technology nodes are introduced has not changed since the ITRS 1998 Update. However, it has changed since the 1997 NTRS, which was the last edition with "explanatory text." Thus, we will next describe the node timing changes between the 1997 NTRS and the 1998/1999 ITRS. By international consensus, the "150-nm node" was eliminated, and the subsequent technology nodes, beginning with the 130-nm node, were pulled in by one year. Note that products built with the 180-nm technology node are shipping in 1999, fulfilling the forecast of a 2-year technology-node cycle from the 250-nm node in 1997. In addition, the introduction into the market place of the 130-nm technology node, which, in 1997, was predicted to occur in the year 2003, is now forecast to occur in the year 2002, representing a continuation of the 3-year cycle for DRAM metal half-pitch nodes. By agreement and driven by performance demand, the MPU gate length is forecast to continue scaling by about 70% per 2-year cycle through the 100-nm MPU gate-length in 2001, but is expected to return to a 3-year cycle thereafter. There is some optimism that DRAM half-pitch nodes could undergo an additional 1-year pull-in. This possibility will be re-evaluated during the year 2000 ITRS update. To reflect the variety of cycles and to allow for closer monitoring of future roadmap shifts, it was agreed to publish annual technology requirements from 1999 through 2005, called the "Near-Term Years," and at three-year (node) intervals thereafter, called the "Long-Term Years" (2008, 2011, 2014).

It should be observed that the ORTC metrics, which guide the Roadmap, are often used by semiconductor companies as a set of targets that need to be achieved ahead of schedule to achieve industry leadership. Thus, the highly competitive environment of the semiconductor industry tends to quickly make obsolete many portions of the ORTC metrics and, consequently, the Roadmap. Hopefully, our annual update process will provide sufficiently close tracking of the evolving international consensus on technology directions to maintain the usefulness of the ITRS to the industry.

BACKGROUND

PRODUCT GENERATIONS AND CHIP-SIZE MODEL

In this section, we will discuss "product generations" and their relationship to the technology nodes. In the past, these terms have often been used interchangeably, but the historically simple picture of a new DRAM product generation every three years, at 4× the previous density and based on an essentially new set of technology features, has become obsolete as a way to define technology nodes. In this edition of the ITRS, "technology node" is still linked to an anticipated DRAM feature size (minimum metal half-pitch), but the implications of this connection are diminishing as the product evolution/shrink path becomes more complex. Thus, "technology node" is now not much more than a simple label for still somewhat convenient "tick-marks" along this path.

Historically, DRAM products have been recognized as the technology drivers for the whole semiconductor industry. Prior to the early 1990s, logic (as exemplified by MPU) technology was developed at a slower pace than DRAM technology. During the last few years, the development rate of new technologies used to manufacture microprocessors has accelerated. As anticipated, microprocessor products have now not only closed the technology gap with DRAM, but are now actually driving the most leading-edge lithography tools. It is now recognized that DRAM and microprocessor products share the technology leadership role.

Several fundamental differences exist between the two families of products. Due to strong commodity market economic pressure to reduce cost and increase fab output productivity, DRAM product emphasizes the minimization of the chip size. Therefore development of DRAM technology focuses mainly on minimization of the area occupied by the memory cell. However, this pressure to minimize cell size is in conflict with the requirement to maximize the capacitance of the cell for charge storage performance, which puts pressure on memory cell designers to find creative ways through design and materials to meet minimum capacitance requirements while reducing cell size. In addition, to closely pack the highest number of DRAM cells in the smallest area requires minimization of cell pitch. Microprocessors have also come under strong market pressure to reduce costs while still maximizing performance, which is dominated by the length of the transistor gate and by the number of interconnect layers. As a result, teams of both regional and international technical and business analysts worked to develop and reach consensus on models of the required functionality, chip size, cell area, and density. Additional line items were added to communicate the model consensus, and the underlying model assumptions are included in notations. It was agreed that the key ITRS technology node identifier would continue to be the DRAM half-pitch. Table 1 also includes the aggressive MPU gate-length performance-driven feature size and, for completeness, also tracks the MPU/ASIC product metal half-pitch that will trail slightly behind or equal to the DRAM half-pitch.

For each product generation, both the leading-edge ("at introduction") and the high-volume ("at production") DRAM products are indicated. As anticipated during the 1997 NTRS renewal, the recent availability of 193-nm wavelength exposure tools, working with complementary mask and photoresist technologies, should enable the 130 nm half-pitch node by 2002. The 150 nm half-pitch capability (now an annualized shrink target, rather than a formal node target) is still expected to become available by 2001, and possibly sooner. It is still anticipated that "non-optical" exposure techniques may become viable contenders to optical lithography with the advent of the 100 nm technology node, presently targeted in 2005 for DRAM metal half-pitch. Printed gate-length of 100 nm for MPU is targeted in 2001.

In comparing the 1999 edition of the ITRS with the 1997 Roadmap, it should be noted that the long-term average annualized reduction rate in feature size is projected to continue at approximately 11%/year (~30% reduction/three years), even though this rate accelerated to approximately 16%/year (~30% reduction/two years) in the time interval 1995–1999. The overall schedule for introduction of a new product generation has once again been accelerated by one additional year, and a best-case opportunity exists for the industry to repeat the performance at the year 2001 Roadmap renewal.

Table 1a Product Generations and Chip Size Model—Near Term Years

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
DRAM ½ Pitch (nm)	180	165	150	130	120	110	100	*D ½*
MPU Gate Length (nm) ††	140	120	100	85-90	80	70	65	*M GATE*
MPU/ASIC ½ Pitch (nm)	230	210	180	160	145	130	115	*M AND A ½*
ASIC Gate Length (nm)	180	165	150	130	120	110	100	*A GATE*
Memory								
Generation at introduction §	1G	—	2G	—	4G	—	8G	—
Functions per chip (Gbits)	1.07	—	2.15	—	4.29	—	8.59	*Market — Moore's Law*
Cell area factor	8.0	7.3	6.6	6.0	5.4	4.9	4.4	*Market — Cost/Timing*
Cell area (μm^2)	0.26	0.20	0.15	0.10	0.08	0.059	0.044	*Market — Cost/Timing*
Chip size at introduction (mm^2) §	400	—	438	—	480	—	526	*Market — Cost/Timing*
Cell array area at introduction (% of chip size) §	70%	—	72%	—	70%	—	72%	*Market — Cost/Timing*
Gbits/cm^2 at introduction §	0.27	—	0.49	—	0.89	—	1.63	*Market — Cost/Timing*
Generation at production §	256M	—	(512)	—	1G	—	2G	*Market — Cost/Timing*
Chip size at production (mm^2) §	132	—	145	—	159	—	174	*Market — Cost/Timing*
Cell array area at production (% of chip size) §	53%	—	55%	—	53%	—	54%	*Market — Cost/Timing*
Gbits/cm^2 at production §	0.20	—	0.37	—	0.68	—	1.23	*Market — Cost/Timing*
Logic (High-volume Microprocessor) Cost-performance *								
Generation at introduction †	p99c	—	p01c	—	p03c	—	p05c	—
Functions per chip (million transistors [Mtransistors])	23.8	—	47.6	—	95.2	—	190	*Market — Moore's Law*
Process/design annual improvement factor ++	0.90	0.90	0.90	0.91	0.92	0.93	0.93	*Market — Cost/Timing*
Transistor density SRAM at introduction (Mtransistors/cm^2)	35	50	70	95	128	173	234	*Market — Cost/Timing*
Transistor density logic at introduction (Mtransistors/cm^2)	6.6	9.4	13	18	24	33	44	*Market — Cost/Timing*
*Chip size at introduction (mm^2) ****	340	—	340	—	372	—	408	*Market — Cost/Timing*

++ The MPU Process/design improvement factor is an estimate of the additional annual functional area reduction required beyond the area reduction contributed by the MPU metal half-pitch reduction. Note that this additional area reduction for transistor density plays a role generally analogous to the "cell area factor" for DRAMs. It has been achieved historically through a combination of many factors, for example: use of additional interconnect levels, self-alignment techniques, and more efficient circuit layout.

Table 1a Product Generations and Chip Size Model—Near Term Years (continued)

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
DRAM ½ Pitch (nm)	180	165	150	130	120	110	100	D ½
MPU Gate Length (nm) ††	140	120	100	85-90	80	70	65	M GATE
MPU/ASIC ½ Pitch (nm)	230	210	180	160	145	130	115	M AND A ½
ASIC Gate Length (nm)	180	165	150	130	120	110	100	A GATE
Logic (High-volume Microprocessor) Cost-performance *(continued)								
Cost performance MPU (Mtransistors/cm^2 at introduction) (including on-chip SRAM) ***	7	—	14	—	26	—	47	M Gate and M and A ½
Generation at ramp †	p97c	—	p99c	—	p01c	—	P03c	—
Chip size at ramp (mm^2) ***	170	—	170	—	214	—	235	Market — Cost/Timing
Cost performance MPU (Mtransistors/cm^2 at ramp, including on-chip SRAM) ***	7	—	14	—	22	—	41	M Gate and M and A ½
Logic (Low-volume Microprocessor) High-performance **								
Generation at ramp ‡	p99h	—	p01h	—	p03h	—	p05h	—
Functions per chip (million transistors)	110	—	220	—	441	—	882	Market — Moore's Law
Chip size at ramp (mm^2) ***	450	—	450	—	567	—	622	Market — Cost/Timing
High-performance MPU Mtransistors/cm^2 at ramp (including on-chip SRAM) ***	24	—	49	—	78	—	142	M Gate and M and A ½
ASIC								
ASIC usable Mtransistors/cm^2 (auto layout)	20	28	40	54	73	99	133	M Gate and M and A ½
ASIC max chip size at ramp (mm^2) (maximum lithographic field size)	800	800	800	800	800	800	800	Lithographic Field Size
ASIC maximum functions per chip at ramp (Mtransistors/chip) (fit in maximum lithographic field size)	160	224	320	432	584	800	1064	Market — Performance/ Timing

†† *Range of node targets indicates the acknowledgment of the difficulty of projecting the impact of the return to the 3-year technology node cycle starting in 2001 and the uncertainty of the long term years of the Roadmap timeframe.*

§ *DRAM Model—Generations 4× bits/chip every four years with interim 2× bits/chip generations; InTER-generation chip size growth rate model is 1.2× every four years; InTRA-generation chip size shrink model is 0.5× every three years beginning 1999.*

† *p is processor, numerals reflect year of introduction, c is cost-performance product.*

‡ *p is processor, numerals reflect year at ramp, h is high-performance product.*

* *MPU Cost-performance Model—Cost-performance MPU includes small level 1 (L1) on-chip SRAM (32Kbyte/1999), but consists primarily of logic transistor functionality; both SRAM and Logic functionality doubles every two years.*

** *MPU High-performance Model—High-performance MPU includes large level 2 (L2) on-chip SRAM (2MByte/1999) added to ramp-level cost-performance core functionality shrunk from 2-year-prior generation (P99h = 11.9M transistor (Mtransistors) (shrunk P97 core) + 98Mtransistors (2048 bytes × 8 bits/byte × 6 transistors/bit) L2 SRAM = 110Mtransistors/1999); both SRAM and Logic functionality doubles every two years.*

*** *MPU Chip Size Model—Both the cost-performance and high-performance MPUs target for InTER-generation chip size growth rate model is flat through 2001, then 1.2× growth every four years after 2001; InTRA-generation chip size shrink model is 0.5× every two years through 2001, then 0.5× every three years after 2001.*

Table 1b Product Generations and Chip Size Model—Long Term Years

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
DRAM ½ Pitch (nm)	70	50	35
MPU Gate Length (nm) ††	45	30-32	20-22
MPU/ASIC ½ Pitch (nm)	80	55	40
ASIC Gate Length (nm)	70	50	35
Memory			
Generation at introduction §	—	64G	—
Functions per chip (billion bits (Gbits))	24.3	68.7	194
Cell area factor	3.5	3.0	2.5
Cell area (μm^2)	0.017	0.008	0.003
Chip size at introduction (mm^2) §	603	691	792
Cell area efficiency at introduction (% of chip size) §	69%	75%	75%
Gbits/cm^2 at introduction §	4.03	9.94	24.5
Generation at production §	—	16G	—
Chip Size at production (mm^2) §	199	229	262
Cell area efficiency at production (% of chip size) §	52%	56%	57%
Gbits/cm^2 at production §	3.05	7.51	18.5
Logic (High-volume Microprocessor) Cost-performance *			
Generation at introduction †	—	p11c	—
Functions per chip (million transistors (Mtransistors))	539	1,523	4,308
Process/design improvement factor	0.93	0.93	0.93
Transistor density SRAM at introduction (Mtransistors/cm^2)	577	1,423	3,510
Transistor density logic at introduction (Mtransistors/cm^2)	109	269	664
*Chip size at introduction (mm^2) ****	468	536	615

Table 1b Product Generations and Chip Size Model—Long Term Years (continued)

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
DRAM ½ Pitch (nm)	70	50	35
MPU Gate Length (nm)††	45	30–32	20–22
MPU/ASIC ½ Pitch (nm)	80	55	40
ASIC Gate Length (nm)	70	50	35
Logic (High-volume Microprocessor) Cost-performance * (continued)			
Cost-performance MPU Mtransistors/cm² at introduction (including on-chip SRAM) ***	115	284	701
Generation at ramp †	—	p09c	—
Chip size at ramp (mm²) ***	269	308	354
Cost performance MPU Mtransistors/cm² at ramp (including on-chip SRAM) ***	100	247	609
Logic (Low-volume Microprocessor) High-performance **			
Generation at ramp ‡	—	p11h	—
Functions per chip (million transistors)	2,494	7,053	19,949
Chip size at ramp (mm²) ***	713	817	937
High-performance MPU Mtransistors/cm² at ramp (including on-chip SRAM) ***	350	863	2,130
ASIC			
ASIC usable Mtransistors/cm² (auto layout)	328	811	2,000
ASIC maximum chip size at ramp (mm²) (maximum lithographic field size)	800	800	800
ASIC maximum functions per chip at ramp (Mtransistors/chip) (fit in maximum lithographic field size)	2,624	6,488	16,000

Since only the 2011 odd-year product generation data column is available in the Long Term table format, interpolated numbers were calculated and included in the 2008 and 2014 node columns. The extended market-need-based product trends for the product generation two-year-cycle years (1999, 2001, 2003, 2005, 2007, 2009, 2011, 2013) are forecast to follow patterns established in Near Term Table 1a.

†† *Range of node targets indicates the acknowledgment of the difficulty of projecting the impact of the return to the 3-year technology node cycle starting in 2001 and the uncertainty of the long term years of the Roadmap timeframe.*

§ *DRAM Model—Generations 4× bits/chip every four years with interim 2× bits/chip generations; InTER-generation chip size growth rate model is 1.2× every four years; InTRA-generation chip size shrink model is 0.5× every three years beginning 1999.*

† *p is processor, numerals reflect year of introduction, c is cost-performance product.*

‡ *p is processor, numerals reflect year at ramp, h is high-performance product.*

* *MPU Cost-performance Model—Cost-performance MPU includes small level 1 (L1) on-chip SRAM (32Kbyte/1999), but consists primarily of logic transistor functionality; both SRAM and Logic functionality doubles every two years.*

** *MPU High-performance Model—High-performance MPU includes large level 2 (L2) on-chip SRAM (2Mbyte/1999) added to ramp-level cost-performance core functionality shrunk from 2-year-prior generation (P99h = 11.9M transistor (Mtransistors) (shrunk P97 core) + 98Mtransistors (2048 bytes × 8 bits/byte × 6 transistors/bit) L2 SRAM = 110Mtransistors/1999); both SRAM and Logic functionality doubles every two years.*

*** *MPU Chip Size Model—Both the cost-performance and high-performance MPUs target for InTER-generation chip size growth rate model is flat through 2001, then 1.2× growth every four years after 2001; InTRA-generation chip size shrink model is 0.5× every two years through 2001, then 0.5× every three years after 2001.*

CHIP-SIZE, LITHOGRAPHIC-FIELD, AND WAFER-SIZE TRENDS

Despite the continuous reduction in feature size of about 30% every three years, the size of first DRAM product demonstration in technical forums such as the IEEE International Solid State Circuits Conference (ISSCC) has continued to double every six years (an increase of about 12%/year). This increase in chip area has been necessary to accommodate 59% more bits/capacitors/transistors per year in accordance with Moore's Law (historically doubling functions per chip every 1.5 years). However, to maintain the historical trend of reducing cost/function by 25–30%/year, it is necessary to continuously enhance equipment productivity, increase manufacturing yields, use the largest wafer size available, and, most of all, increase the number of chips available on a wafer. The increase in the gross number of chips available on a wafer is primarily obtained by reducing the area of the chip by means of a combination of smaller feature size (shrink/scaling) and product/process redesign (compaction). For instance, using the latest consensus models, it is forecast that the introduction chip area of a cost-effective product generation [which doubles the inter-generation (generation-to-generation) functionality every two years] must grow no faster than 20% every four years. Furthermore, the area must be shrunk at an intra-generation (within a generation) annual reduction rate of 50% (the square of the .7× lithography reduction rate) during every technology node period. Due to an additional 2-year cycle through the year 2001, the MPU products will be able to target a flat die size. However, after 2001, the intra-generation chip size of MPUs will also grow at a 20%-per-four-years rate due to the return to a 3-year technology node cycle. Doubling the on-chip functionality (transistors) and growing only 20% every four years will require MPU chip and process designers to add to lithography improvements an additional design/process chip-size reduction of 7% annually after 2001.

DRAM products must meet the requirements of the limited intra-generation chip-size growth and also maintain a cell area ratio of less than 70% of total die area. Therefore, DRAM products require aggressive cell area factors (cell area in units of minimum-feature-size-squared). The Front-End Processes Technology Working Group has provided the cell area factors and detailed the challenges and needs for solutions to meet the aggressive cell area goals in the Front-End Processes chapter. Due to the importance of tracking/coordinating these new challenges, the DRAM cell area factor, the target cell sizes, and the cell array area percentage of total chip-size line items have been added to ORTC Table 1. To improve productivity, it is necessary to increase the output of good chips at each step in the fabrication process. The ability of printing multiple chips in a single exposure is determined by the field size of the lithographic tool and the size and aspect ratio of the chips being printed on the wafer. The roadmap for this useful parameter is included in Table 2.

In the present ITRS chip-size model for DRAMs, the introduction chip size is smaller than the existing 800-mm^2 capability of large step-and-scan fields. Even the large high-performance MPU chip sizes are not forecast to grow larger than 800 mm^2 until the 2011 generation. However, the models depend upon not only meeting the present lithography targets, but are also dependent on achieving the aggressive DRAM and MPU design and process improvement targets. If those targets slip, then pressure will increase to print chip sizes larger than the present roadmap.

Historically, another major productivity increase has resulted from the industry's conversion to wafer sizes of progressively larger diameter. It is projected that the number of available chips will increase by a factor of 2.4–2.5 on a 300-mm wafer compared to the number of chips available on a 200-mm wafer. However, it is presently forecast that conversion to high-volume production using 300-mm diameter wafers will not begin until 2001, even though a full-flow pilot line was demonstrated in 1998 and actually produced commercial 64-Mbit DRAMs. The delay of 300-mm ramp was due to a combination of: 1) overbuilt 200-mm fabs; 2) a significant slow-down in the Asian economies; and 3) the rapid deployment of accelerated-technology (primarily lithography) upgrade equipment into existing factories to meet the demand for increased unit shipments of leading-edge products in an environment of rapidly falling market prices.

The semiconductor industry shows signs of a recovery having begun 1999. So, the need for the 300-mm productivity boost should increase in urgency, especially for leading-edge manufacturers who have little or no over-capacity. The 1999 Wafer-Diameter Generation roadmap was adapted to be consistent with the delayed start of 300 mm. Therefore, the first pilot capability for the next 1.5× wafer size conversion to 450-

mm diameter is not anticipated to be required until 2009–10. Likewise, consistent with the 300-mm wafer generation experience, 450-mm wafer production will not begin volume ramp (20K wafer start per week capacity) until the 2012–2014 timeframe. However, should the other productivity-improvement drivers (lithography and design/process improvements) fail to stay on schedule, there would be a need to accelerate the use of increased wafer diameter as a productivity improvement.

Table 2a Chip-Size, Lithographic-Field and Wafer-Size Trends—Near Term Years

(Note: 1999 Lithographic field sizes represent current capability)

YEAR TECHNOLOGY NODE	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*
DRAM Chip Size							
Cell area factor	8.0	7.3	6.6	6.0	5.4	4.9	4.4
Cell area (μm^2)	0.26	0.20	0.15	0.10	0.08	0.059	0.044
Cell array area at introduction (% of chip size) §	70%	—	72%	—	70%	—	72%
DRAM generation at introduction §	1G	—	(2G)	—	4G	—	(8G)
Chip size at introduction (mm^2) §	400	—	438	—	480	—	526
Chip height at 2:1 aspect ratio (mm)	14.1	—	14.8	—	15.5	—	16.2
Chip length at 2:1 aspect ratio (mm)	28.3	—	29.6	—	31.0	—	32.4
Cell array area at sample (% of chip size) §	60%	—	63%	—	61%	—	62%
DRAM generation at sample §	(512M)	—	1G	—	(2G)	—	4G
Chip size at sample (mm^2) §	230	—	252	—	276	—	302
Chip height at 2:1 aspect ratio (mm)	10.7	—	11.22	—	11.8	—	12.3
Chip length at 2:1 aspect ratio (mm)	21.5	—	22.5	—	23.5	—	24.6
Cell array area at production (% of chip size) §	53%	—	55%	—	53%	—	54%
Generation at production §	256M	—	(512)	—	1G	—	2G
Chip size at production (mm^2) §	132	—	145	—	159	—	174
Chip height at 2:1 aspect ratio (mm)	8.1	—	8.5	—	8.9	—	9.33
Chip length at 2:1 aspect ratio (mm)	16.3	—	17.0	—	17.8	—	18.7
Cell array area at ramp (% of chip size) §	.48%	—	49%	—	45%	—	47%
Generation at ramp §	(128)	—	256M	—	(512)	—	1G
Chip size at ramp (mm^2) §	74	—	83	—	91	—	100
Chip height at 2:1 aspect ratio (mm)	4.2	—	6.4	—	8.9	—	9.3
Chip length at 2:1 aspect ratio (mm)	8.4	—	12.7	—	17.9	—	18.6
MPU Chip Size							
*High-performance MPU generation at ramp ** ‡*	p99h	—	p01h	—	p03h	—	P05h
*Chip size at ramp (mm^2) ****	450	—	450	—	567	—	622
Maximum lithographic field size — area (mm^2)	800	800	800	800	800	800	800
Maximum lithographic field size — length (mm)	32	32	32	32	32	32	32
Maximum lithographic field size — width (mm)	25	25	25	25	25	25	25
Minimum lithographic field size — area (mm^2)	484	506	529	552	576	600	625
Minimum lithographic field size — length (mm)	22	22.5	23	23.5	24	24.5	25
Minimum lithographic field size — width (mm)	22	22.5	23	23.5	24	24.5	25
Maximum Substrate Diameter (mm) — High-volume Production (>20K wafer starts per month)							
Bulk or epitaxial or SOI wafer	200	200	300	300	300	300	300

Table 2b Chip-Size, Lithographic-Field and Wafer Size Trends—Long Term Years

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
DRAM Chip Size			
Cell area factor	3.5	3.0	2.5
Cell area (μm^2)	0.017	.008	0.003
Cell array area at introduction (% of chip size) §	69%	75%	75%
DRAM generation at introduction §	—	64G	—
Chip size at introduction (mm^2) §	603	691	792
Chip height at 2:1 aspect ratio (mm)	17.4	18.6	19.9
Chip length at 2:1 aspect ratio (mm)	34.7	37.2	39.8
Cell array area at sample (% of chip size) §	60%	65%	65%
DRAM generation at sample §	—	(32G)	—
Chip size at sample (mm^2) §	347	398	456
Chip height at 2:1 aspect ratio (mm)	13.2	14.1	15.1
Chip length at 2:1 aspect ratio (mm)	26.3	28.2	30.2
Cell array area at production (% of chip size) §	52%	56%	57%
Generation at production §	—	16G	—
Chip size at production (mm^2) §	199	229	262
Chip height at 2:1 aspect ratio (mm)	10.0	10.7	11.4
Chip length at 2:1 aspect ratio (mm)	20.2	21.4	22.9
Cell array area at ramp (% of chip size) §	45%	49%	49%
Generation at ramp §	—	(8G)	—
Chip size at ramp (mm^2) §	115	131	151
Chip height at 2:1 aspect ratio (mm)	7.6	8.1	8.7
Chip length at 2:1 aspect ratio (mm)	15.2	16.2	17.4
MPU Chip Size			
*High-performance MPU generation at ramp ** ‡*	—	p11h	—
*Chip size at ramp (mm^2) ****	713	817	937
Maximum lithographic field size—area (mm^2)	800	800	800
Maximum lithographic field size—length (mm)	32	32	32
Maximum lithographic field size—width (mm)	25	25	25
Minimum lithographic field size—area (mm^2)	625	625	625
Minimum lithographic field size—length (mm)	25	25	25
Minimum lithographic field size—width (mm)	25	25	25
Maximum Substrate Diameter (mm)—High-volume Production (>20K wafer starts per month)			
Bulk or epitaxial or SOI wafer	300	300	450

SOI—Silicon on Insulator

§ *DRAM Model—Generations 4× bits/chip every four years with interim 2× bits/chip generations; InTER-generation chip size growth rate model is 1.2× every four years; InTRA-generation chip size shrink model is 0.5× every three years beginning 1999.*

‡ *p is processor, numerals reflect year at ramp, h is high-performance product.*

** *MPU High-performance Model—High-performance MPU includes large level 2 (L2) on-chip SRAM (2MByte/1999) added to ramp-level cost-performance core functionality shrunk from 2-year-prior generation (P99h = 11.9M transistor (Mtransistors) (shrunk P97 core) + 98Mtransistors (2048 bytes × 8 bits/byte × 6 transistors/bit) L2 SRAM = 110Mtransistors/1999); both SRAM and Logic functionality doubles every two years.*

*** *MPU Chip Size Model—Both the cost-performance and high-performance MPUs target for InTER-generation chip size growth rate model is flat through 2001, then 1.2× growth every four years after 2001; InTRA-generation chip size shrink model is 0.5× every two years through 2001, then 0.5× every three years after 2001.*

PERFORMANCE OF PACKAGED CHIPS

NUMBER OF PADS AND PINS / PAD PITCH, COST PER PIN, FREQUENCY

The demand for a higher number of functions on a single chip requires the integration of an increased number of transistors or bits (memory cells) for each product generation. Typically, the number of pads and pins necessary to allow Input/Output (I/O) signals to flow to and from an integrated circuit increases as the number of transistors on a chip increases. Refer to Table 3.

Additional power and ground connections to the chip are also necessary to optimize power management and to increase noise immunity. Based upon chip pad-count numbers supplied by the Test TWG, logic products (MPUs and high-performance ASICs) both approach a maximum of about 4K pads over the ITRS period. The MPU products are forecast to almost double the total number of pads through this period, whereas the ASICs nearly triple the maximum number of pads per chip. The two product types also differ significantly in the ratio of power/ground pads. The MPU product pad counts have a typical ratio of 1/3 signal I/O pads to 2/3 power and ground pads, or two power/ground pads for every signal I/O pad. Unlike MPUs, high-performance ASIC product pad counts typically include only one power/ground pad for each signal I/O pad.

Table 3a Performance of Packaged Chips: Number of Pads and Pins—Near Term Years

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
Number of Chip I/Os (Number of Total Chip Pads) — Maximum							
Total pads—MPU	2,304	2,560	3,042	3,042	3,042	3,042	3,042
Signal I/O—MPU (1/3 of total pads)	768	1,024	1,024	1,024	1,024	1,024	1,024
Power and ground pads—MPU (2/3 of total pads)	1,536	1,536	2,018	2,018	2,018	2,018	2,018
Total pads—ASIC high-performance	1,400	1,800	2,200	2,600	3,000	3,400	3,800
Signal I/O pads—ASIC high-performance (½ of total pads)	700	900	1,100	1,300	1,500	1,700	1,900
Power and ground pads—ASIC high-performance (½ of total pads)	700	900	1,100	1,300	1,500	1,700	1,900
Chip-to-package pads (Peripheral)	368	397	429	464	501	541	584
Number of Total Package Pins/Balls—Maximum							
Microprocessor/controller, cost-performance	740	821	912	1,012	1,123	1,247	1,384
ASIC (high-performance)	1,600	1,792	2,007	2,248	2,518	2,820	3,158

Table 3b Performance of Packaged Chips: Number of Pads and Pins—Long Term Years

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
Number of Chip I/Os (Number of Total Chip Pads)—Maximum			
Total pads—MPU	3,840	4,224	4,416
Signal I/O pads—MPU (1/3 of total pads)	1,280	1,408	1,472
Power and ground pads—MPU (2/3 of total pads)	2,560	2,816	2,944
Total pads—ASIC high-performance	4,600	5,400	6,000
Signal I/O pads—ASIC high-performance (½ of total pads)	2,300	2,700	3,000
Power and ground pads—ASIC high-performance (½ of total pads)	2,300	2,700	3,000
Chip-to-package pads (Peripheral)	736	927	1,167
Number of Total Package Pins/Balls—Maximum			
Microprocessor/controller, cost-performance	1,893	2,589	3,541
ASIC (high-performance)	4,437	6,234	8,758

Package pin-count (Table 3) and cost-per-pin (Table 4), provided by the Assembly and Package TWG, point out challenges to future manufacturing economics. Based upon the projected growth in the number of transistors/chip, it is forecast that the number of package pin/balls will continue to grow at an annual rate of approximately 11%, while the cost/pin decreases at 5%/year. These trends make it more challenging for suppliers of packaging technologies to deliver cost-effective solutions, because the overall average cost of packaging will increase annually at 5%/year (1.11 cost/pin × .95 pins/year = 1.05 cost/year).

In the very competitive consumer electronics product environment, prices for high-volume, high-tech products such as PCs and cell phones tend to remain flat or even decrease. These same high-tech products typically also deliver twice the performance every two years. This is the end-use market environment of the leading-edge semiconductor manufacturer, and it is the fundamental economic driver behind the ITRS economic requirement to reduce cost per function (bits, transistors) at an annual 30% or faster rate (2× functionality/chip at flat price every two years = 29%/year).

If future semiconductor component products must be targeted to maintain constant or decreasing prices and the average number of pins per unit increases at 11% while the average cost per pin decreases at only 5%, then the following will occur:

1) the average packaging share of total product cost will double over the 15-year roadmap period, and
2) the ultimate result will be greatly reduced gross profit margins and limited ability to invest in R&D and factory capacity.

This conclusion is one of the drivers behind the industry trends to reduce the overall system pin requirements by combining functionality into Systems-on-Chip (SoC) and through the use of multi-chip modules, bumped chip-on-board (COB), and other creative solutions.

In addition to the need to increase functionality while exponentially decreasing cost per function, there is also a seemingly insatiable market demand for higher-performance, cost-effective products. Just as "Moore's Law" predicts that functions-per-chip will double every 1.5 years to keep up with consumer demand, there is a corresponding demand for processing electrical signals at progressively higher rates. In the case of MPUs, processor instructions/second have also historically doubled every 1.5–2 years. For MPU products, increased processing power, measured in millions of instructions per second (MIPs), is accomplished through a combination of "raw technology performance" (clock frequency) multiplied by "architectural performance" (instructions per clock cycle). The need for a progressively higher operational frequency associated with an increasing average chip size will continue to demand the development of novel process, design, and packaging techniques.

These considerations are reflected in Table 4, which includes line items contributed by the Design TWG to forecast the multiple categories of frequency trends. The highest frequency obtainable in each product generation is directly related to the intrinsic transistor performance (on-chip, local clock). The difference between this "local" frequency and the frequency of signals traveling across the chip (across-chip clock) tends to become progressively larger in the future due to degradation of signal propagation delay caused by line-to-line and line-to-substrate capacitive coupling. Additional signal degradation is associated with the inductance of wire bonds and package leads. Direct chip attachment may eventually be the only viable way to eliminate any parasitic effect introduced by the package. To optimize signal and power distribution across the chip, it is expected that the number of layers of interconnect will continue to increase. As size downscaling of interconnect also continues, wider use of copper (low resistivity) and various inter-metal insulating materials of progressively lower dielectric constant (κ~2–3) will be adopted in the chip fabrication process. Multiplexing techniques will also be used to increase the chip-to-board operating frequency (off-chip).

Table 4a Performance and Package Chips: Pads, Cost, and Frequency—Near Term Years

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
Chip Pad Pitch (micron)							
Pad pitch—ball bond	50	48	47	45	43	42	40
Pad pitch—wedge bond	45	43	42	40	39	38	35
Pad pitch—area array	200	200	200	200	182	165	150
Cost-Per-Pin							
Package cost (cents/pin) (cost-performance)—maximum	1.90	1.81	1.71	1.63	1.55	1.47	1.40
Package cost (cents/pin) (cost-performance)—minimum	0.90	0.86	0.81	0.77	0.73	0.70	0.66
Package cost (cents/pin) (Memory)—maximum	1.90	1.71	1.54	1.39	1.25	1.12	1.01
Package cost (cents/pin) (Memory)—minimum	0.40	0.38	0.36	0.34	0.33	0.31	0.29
Chip Frequency (MHz)							
On-chip local clock, (high-performance)	1,250	1,486	1,767	2,100	2,490	2,952	3,500
On-chip, across-chip clock (high-performance)	1,200	1,321	1,454	1,600	1,724	1,857	2,000
On-chip, across-chip clock, high-performance ASIC	500	559	626	700	761	828	900
On-chip, across-chip clock (cost-performance)	600	660	727	800	890	989	1,100
Chip-to-board (off-chip) speed (high-performance, reduced-width, multiplexed bus)	1,200	1,321	1,454	1,600	1,724	1,857	2,000
Chip-to-board (off-chip) speed (high-performance, for peripheral buses)	480	589	722	885	932	982	1,035
Maximum number wiring levels—maximum	7	7	7	8	8	8	9
Maximum number wiring levels—minimum	6	6	7	7	8	8	8

Table 4b Performance and Package Chips: Pads, Cost, and Frequency—Long Term Years

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
Chip Pad Pitch (micron)			
Pad pitch—ball bond	40	40	40
Pad Pitch—wedge bond	35	35	35
Pad Pitch—area array	150	150	150
Cost-Per-Pin			
Package cost (cents/pin) (cost-performance)—maximum	1.20	1.03	0.88
Package cost (cents/pin) (cost-performance)—minimum	0.57	0.49	0.42
Package cost (cents/pin) (memory)—maximum	0.74	0.54	0.39
Package cost (cents/pin) (memory)—minimum	0.25	0.22	0.19
Chip Frequency (MHz)			
On-chip local clock, (high-performance)	6,000	10,000	13,500
On-chip, across-chip clock (high-performance)	2,500	3,000	3,600
On-chip, across-chip clock (high-performance ASIC)	1,200	1,500	1,800
On-chip, across-chip clock (cost-performance)	1,400	1,800	2,200
Chip-to-board (off-chip) speed (high-performance, reduced-width, multiplexed bus)	2,500	3,000	3,600
Chip-to-board (off-chip) speed (high-performance, for peripheral buses)	1,285	1,540	1,800
Maximum number wiring levels—maximum	9	10	10
Maximum number wiring levels—minimum	9	9	10

ELECTRICAL DEFECT DENSITY

The latest targets for electrical defect density of DRAM, MPU, and ASIC (necessary to achieve 65–85% chip yield in the year of volume production) are shown in Table 5. The allowable number of defects is calculated by taking into account the different chip sizes, based on the latest chip size model forecasts, as reported in Table 1 and 2 for DRAM and microprocessors. The maximum chip area of ASIC products is assumed equal to the maximum available field size of the exposure tool. In addition, the data in the table are now reported at the production life-cycle point. Other defect densities may be calculated at different chip sizes at the same technology node by using the formula found in the *Defect Reduction* chapter. The approximate number of masks for logic devices is included as an indicator of the ever-increasing process complexity.

Table 5a Electrical Defects—Near Term Years

YEAR *TECHNOLOGY NODE*	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*
Defect Reduction							
DRAM at production electrical D_0 chip size at 85% yield (d/m^2) §	1,249	1,193	1,140	1,089	1,040	994	950
*MPU at ramp electrical D_0 chip size at 75% yield (d/m^2) ****	1,742	1,742	1,742	1,552	1,383	1,321	1,262
ASIC first year electrical D_0 at 65% yield (d/m^2)	562	562	562	562	562	562	562
Minimum, mask count—maximum	24	24	24	24	25	25	26
Minimum, mask count—minimum	22	23	23	24	24	24	24

Table 5b Electrical Defects—Long Term Years

YEAR *TECHNOLOGY NODE*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
Defect Reduction			
DRAM at production electrical D_0 chip size at 85% yield (d/m^2) §	828	723	630
*MPU at ramp electrical D_0 chip size at 75% yield (d/m^2) ****	1,101	960	837
ASIC first year electrical D_0 at 65% yield (d/m^2)	562	562	562
Minimum, mask count—maximum	28	28	30
Minimum, mask count—minimum	26	28	29

D_0—defect density

§ *DRAM Model—Generations 4× bits/chip every four years with interim 2× bits/chip generations; InTER-generation chip size growth rate model is 1.2× every four years; InTRA-generation chip size shrink model is 0.5× every three years beginning 1999.*

*** *MPU Chip Size Model—Both the cost-performance and high-performance MPUs target for InTER-generation chip size growth rate model is flat through 2001, then 1.2× growth every four years after 2001; InTRA-generation chip size shrink model is 0.5× every two years through 2001, then 0.5× every three years after 2001.*

POWER SUPPLY AND POWER DISSIPATION

Reduction of power supply voltage is driven by several factors: reduction of power dissipation, reduced transistor channel length, and reliability of gate dielectrics. The way in which the value of the power supply voltage is represented in the 1999 ITRS is the same as that used in the 1997 Roadmap. As seen in Table 5, the value of the power supply voltage is now given as a range.

Selection of a specific V_{dd} value continues to be a part of the analysis undertaken to simultaneously optimize speed and power for an IC, leading to a range of usable power supply voltages in each product generation. Values of V_{dd} as low as 0.5 volts by 2011 are still considered viable, and the target to go to .3 Volts by 2014 has been added to the Roadmap.

Maximum power trends (e.g., for MPUs) are still presented in the two categories: 1) high-performance desktop applications, for which a heat sink on the package is permitted, and 2) portable battery operations. In both cases, total power consumption continues to increase, despite the use of a lower supply voltage. The increased power consumption is driven by higher operating frequency and the higher overall capacitance and resistance of larger chips with more on-chip functions.

Table 6a Power Supply and Power Dissipation—Near Term Years

YEAR *TECHNOLOGY NODE*	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*
Power Supply Voltage (V)							
Minimum logic V_{dd} (V)—maximum (for maximum performance)	1.8	1.8	1.5	1.5	1.5	1.2	1.2
Minimum logic V_{dd} (V)—minimum (for lowest power))	1.5	1.5	1.2	1.2	1.2	0.9	0.9
Maximum Power							
High-performance with heatsink (W)	90	100	115	130	140	150	160
Battery (W)—(hand-held)	1.4	1.6	1.7	2.0	2.1	2.3	2.4

Table 6b Power Supply and Power Dissipation—Long Term Years

YEAR *TECHNOLOGY NODE*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
Power Supply Voltage (V)			
Minimum logic V_{dd} (V)—maximum (for maximum performance)	0.9	0.6	0.60
Minimum logic V_{dd} (V)—minimum (for lowest power))	0.6	0.5	0.30
Maximum Power			
High-performance with heatsink (W)	170	174	183
Battery (W)—(hand-held)	2.0	2.2	2.4

Cost

Table 7 is dedicated to cost trends. The ability to reduce the cost per function by an average 25-30% each year represents one of the unique features of the semiconductor industry and is a direct consequence of delivering twice the functionality on-chip every 1.5 years in an environment of constant or reducing prices. In support of this cost reduction, a continuously increasing amount of investment is needed for R&D and manufacturing capital. Even on a per-factory basis, the capital cost of manufacturing continues to escalate. Yet, the semiconductor industry has historically delivered four times as many functions per chip every three years with only a moderate 1.4× increase in chip size and 1.4× in cost (approximately constant cost per cm^2 of silicon). This technological and economic performance is the fundamental engine behind the growth of the semiconductor industry.

However, the customers in today's competitive market environment are resistant to even "moderate" increases in cost. Therefore, the semiconductor manufacturers must seek a new model to deliver the same cost-per-function reduction requirements that have fueled industry growth. Consequently, the 1999 ITRS participants have proposed a new model for achieving the required reduction: provide the customer twice the functionality every two years at a constant cost per chip. This new model results in the same 29% cost reduction of a function (bit, transistor, etc.) that has been achieved historically by delivering four times the functionality per chip every three years at 1.4× increase in cost per unit.

The new model has been used to set the trends for the affordable cost/bit and cost/transistor for DRAM and microprocessors, respectively. These cost targets, together with the technical targets, should guide the activity of the engineering community in planning and executing each technology-development program. One illustration of the new model, shown in Table 7, is that DRAM suppliers, to keep maximum average selling prices (ASPs) constant between (inter) generations, must introduce generations with 2× on-chip bits every two years and set targets to decrease the cost/bit at an average rate of 29%/year.

Extrapolation of historical trends would indicate an "at introduction" affordable cost/bit of approximately 42 microcents for 1-Gbit DRAMs in 1999. In addition, the historical trends indicate that, within a DRAM generation, a 45%/year reduction in cost/bit should be expected.[1] A corresponding analysis conducted from published data for microprocessors yields similar results.[2] In the case of MPUs, generations are now also targeted for 2× functionality (transistors) increase every two years. The 29%/year target for reduction in affordable cost/transistor from generation to generation is also being used in this case, along with the 45%/year reduction rate within the same generation.

As the number of functions/chip continues to increase, it becomes increasingly difficult and, therefore, costly to test the final products. This is reflected in the escalating cost of testers. Even though the cost/pin of testers is forecast to decline between 3% and 9% per year (Table 7), the number of pins grows at 11%/year (Table 3). Therefore, the need for accelerated implementation of Built-In-Self-Test (BIST) and Design-For-Testability (DFT) techniques will continue within the time frame of the 1999 International Technology Roadmap for Semiconductors. Further discussion is detailed in the *Test* chapter.

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[1] McClean, William J., ed. Mid-Term 1994: *Status and Forecast of the IC Industry.* Scottsdale: Integrated Circuit Engineering Corporation, 1994. McClean, William J., ed. Mid-Term 1995: *Status and Forecast of the IC Industry.* Scottsdale: Integrated Circuit Engineering Corporation, 1995.

[2] a) Dataquest Incorporated. *x86 Market: Detailed Forecast, Assumptions, and Trends.* MCRO-WW-MT-9501. San Jose: Dataquest Incorporated, January 16, 1995.
b) Port, Otis; Reinhardt, Andy; McWilliams, Gary; and Brull, Steven V. "The Silicon Age? It's Just Dawning," Table 1. *Business Week*, December 9, 1996, 148–152.

Table 7a Cost—Near Term Years

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
Affordable Cost per Function ++							
DRAM cost/bit at (packaged microcents) at samples/introduction	42	—	21	—	11	—	5.3
DRAM cost/bit at (packaged microcents) at production §	15	—	7.6	—	3.8	—	1.9
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction ***	1,735	—	868	—	434	—	217
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at ramp ***	1,050	—	525	—	262	—	131
High-performance MPU (microcents/transistor) (including on-chip SRAM) at ramp ***	245	—	123	—	61	—	31
Cost-Per-Pin (see Table 4)	—	—	—	—	—	—	—
Test							
Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—maximum	8	7	7	6	6	5	5
Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—minimum	4	3	3	3	3	2	2
Volume tester cost/pin ($K/pin) (cost-performance MPU)	8	8	7	7	6	6	5

Table 7b Cost—Long Term Years

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
Affordable Cost per Function ++			
DRAM cost/bit (packaged microcents) at samples/introduction	—	0.66	—
DRAM cost/bit (packaged microcents) at production §	—	0.24	—
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction ***	—	27	—
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at ramp ***	—	16	—
High-performance MPU (microcents/transistor) (including on-chip SRAM) at ramp ***	—	3.8	—
Cost-Per-Pin (see Table 4)	—	—	—
Test			
Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—maximum	5	5	5
Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—minimum	N/A	N/A	N/A
Volume tester cost/pin ($K/pin) (cost-performance MPU)	4	2	2

++ *Affordable packaged unit cost per function based upon Average Selling Prices (ASPs) available from various analyst reports less Gross Profit Margins (GPMs); 35% GPM used for commodity DRAMs and 60% GPM used for MPUs; 0.5x/two years inTER-generation reduction rate model used; .55x/year inTRA-generation reduction rate model used; DRAM unit volume life-cycle peak occurs when inTRA-generation cost per function is crossed by next generation, typically 7–8 years after introduction; MPU unit volume life-cycle peak occurs typically after four years, when the next generation processor enters its ramp phase (typically two years after introduction).*

§ *DRAM Model—Generations 4x bits/chip every four years with interim 2x bits/chip generations; InTER-generation chip size growth rate model is 1.2x every four years; InTRA-generation chip size shrink model is 0.5x every three years beginning 1999.*

*** *MPU Chip Size Model—Both the cost-performance and high-performance MPUs target for InTER-generation chip size growth rate model is flat through 2001, then 1.2x growth every four years after 2001; InTRA-generation chip size shrink model is 0.5x every two years through 2001, then 0.5x every three years after 2001.*

GLOSSARY

KEY OVERALL ROADMAP TECHNOLOGY CHARACTERISTICS (ORTC) TERMINOLOGY (WITH OBSERVATIONS AND ANALYSIS)

CHARACTERISTICS OF MAJOR MARKETS

TECHNOLOGY NODE (nm)—The ground rules of process governed by the smallest feature printed. The half-pitch of first-level interconnect dense lines is most representative of the DRAM technology level required for the smallest economical chip size. For logic, such as microprocessors (MPUs), gate length is most representative of the leading-edge technology level required for maximum performance. MPU and ASIC logic interconnect half-pitch processing requirements typically lag behind DRAM half-pitch. For cost reasons, high-volume, low-cost ASIC gate-length requirements will typically match DRAM half-pitch targets, but the low-volume leading-edge high-performance ASIC gate-length requirements will track closely with MPUs.

"MOORE'S LAW"—An historical observation by Intel executive, Gordon Moore, that the market demand (and semiconductor industry response) for functionality per chip (bits, transistors) doubles every 1.5 to 2 years. He also observed that MPU performance [clock frequency (MHz) × instructions per clock = millions of instructions per second (MIPS)] also doubles every 1.5 to 2 years. Although viewed by some as a "self-fulfilling" prophecy, "Moore's Law" has been a consistent macro trend, and key indicator of successful leading-edge semiconductor products and companies, for the past 30 years.

"COST-PER-FUNCTION" MANUFACTURING PRODUCTIVITY IMPROVEMENT DRIVER—In addition to "Moore's Law", there is a historically-based "corollary" to the "law," which suggests that, to be competitive, manufacturing productivity improvements must also enable the cost-per-function (microcents per bit or transistor) to decrease by -29% per year. Historically, when functionality doubled every 1.5 years, then cost-per-chip (packaged unit) could double every six years and still meet the cost-per-function reduction requirement. If functionality doubles only every two years, as suggested by consensus DRAM and MPU models of the 1999 ITRS, then the manufacturing cost per chip (packaged unit) must remain flat.

"Affordable" Packaged Unit Cost/Function—Final cost in microcents of the cost of a tested and packaged chip divided by ***Functions/Chip***. Affordable costs are calculated from historical trends of affordable average selling prices [gross annual revenues of a specific product generation divided by the annual unit shipments] less an estimated gross profit margin of approximately 35% for DRAMs and 60% for MPUs. The affordability per function is a guideline of future market "tops-down" needs, and as such, was generated independently from the chip size and function density. Affordability requirements are expected to be achieved through combinations of—1) smaller chip sizes from technology and design improvements; 2) increasing wafer diameters; 3) decreasing equipment cost-of-ownership (CoO); 4) increasing equipment overall equipment effectiveness; 5) reduced package and test costs; 6) improved design tool productivity; and 7) enhanced product architecture and integration.

DRAM Generation at ***(product generation life-cycle level)***—The anticipated bits/chip of the DRAM product generation introduced in a given year, manufacturing technology capability, and life-cycle maturity (Demonstration, Introduction, Sample, Production, Ramp, Peak).

MPU Generation at ***(product generation life-cycle level)***—The generic processor generation identifier for the anticipated Microprocessor Unit (MPU) product generation functionality (logic plus SRAM transistors per chip) introduced in a given year, manufacturing technology capability, and life-cycle maturity (Introduction, Ramp, Peak, Embedded).

Cost-Performance MPU—MPU product optimized for lowest cost by minimizing on-chip SRAM to level-one (L1) cache only (32Kbytes/1999). Logic functionality and L1 cache typically double every 2-year generation. This typically has a 6-year (introduction plus ramp plus peak) computer-market-application life-cycle before being replaced by the next generation cost-performance MPU, then continues on in embedded applications.

High-performance MPU—MPU product optimized for maximum system performance by using a shrunk cost-performance ramp-level MPU core combined with a large (2Mbyte/1999) level-two (L2) SRAM. Logic functionality and L2 cache typically double every two-year generation. Typically has only a 4-year (ramp and peak) life cycle in the relatively low-volume, higher-priced, high-performance computer market. There is no classic "embedded" application for the high-SRAM-content MPU, but that may change as future market demand develops for multiple-MPU-per box internet server and communication processor applications emerge. Those applications will provide increased demand for more cost-effective inTRA generation shrinks of the high-performance MPU, thus extending the life-cycles of future generations.

PRODUCT INTER-GENERATION—Product generation-to-generation targets for periodically increasing on-chip functionality and allowable chip size. The targets are set to maintain "Moore's Law," while preserving economical manufacturability. The 1999 ITRS consensus target for the rate of increase of DRAM and MPU inTER-generation functionality is 2×/chip every two years. The allowable inTER-generational chip size growth for DRAMs is 1.2× every four years. For MPUs, the allowable chip size growth is flat through 2001, then grows at 1.2× every four years. To add only 20% in area every four years, while quadrupling functionality, requires an inTER-generation design productivity which further reduces chip size by an additional minus 7–8 % per year. This design-related productivity reduction is in addition to the basic lithography-provided area reduction of -11% per year.

PRODUCT INTRA-GENERATION—Within a given product generation. The consensus-based targets reduce chip size (by shrinks and "cut-downs") utilizing the latest available manufacturing and design technology at every point through the roadmap. The ITRS consensus targets for both DRAM and MPU reduce chip size within a generation by minus 50% per technology node. For DRAM, this reduction of minus 50% occurs every three years, or minus 37% every two years. For MPU, the 50% reduction occurs every two years through 2001, then slows to minus 37% per two years (same as DRAM).

YEAR OF DEMONSTRATION—Year in which the leading chip manufacturer supplies an operational sample of a product as a demonstration of design and/or technology node processing feasibility and prowess. A typical venue for the demonstration is a major semiconductor industry conference, such as the International Solid State Circuits Conference (ISSCC) held by the Institute of Electrical and Electronic Engineers (IEEE). Demonstration samples are typically manufactured with early development or demonstration- level manufacturing tools and processes. Historically, DRAM products have been demonstrated at 4× bits-per-chip every three years at the leading-edge process technology node, typically 2–3 years in advance of actual market introduction. DRAM demonstration chip sizes have doubled every six years, requiring an increasing number of shrinks and delay before market introduction is economically feasible. Frequently, chip sizes are larger than the field sizes available from lithography equipment, and must be "stitched" together via multiple-exposure techniques that are feasible only for very small quantities of laboratory samples. Example: 1997/ISSCC/1Gb DRAM.

YEAR OF INTRODUCTION (DRAM)—Year in which the leading chip manufacturer supplies small quantities of engineering samples (<1K). These are provided to key customers for early evaluation, and are manufactured with qualified production tooling and processes. To balance market timeliness and economical manufacturing, DRAM products will be introduced at 2× functionality per chip every two years. In addition, manufacturers will delay introduction until a chip-size shrink or "cut-down" level is achieved which limits the inTER-generation chip-size growth to 1.2× every 4 years, or approximately 1.1× every 2-year generation. Example: 1999/1Gb DRAM.

YEAR OF SAMPLE (DRAM)—Year in which the leading chip manufacturers begin to supply volume quantities of qualification samples (10K–100K) of dynamic random access memories (DRAMs) that are manufactured with qualified production tooling and processes. The leading-edge DRAM production sample products are typically half-size-generation products which are "cut down" from the introduction-level generation design and manufacturing processes.
Example: 1999/512Mb DRAM.

YEAR OF PRODUCTION (DRAM)—Year in which leading chip manufacturers begin shipping volume quantities (millions per month) of product manufactured with qualified production tooling and processes. This product typically contains one-fourth (1/4) the bits per chip of the introduction-level generation design, from which it is "cut-down." Example: 1999/256Mb DRAM.

YEAR OF RAMP (DRAM)—Year in which leading chip manufacturers begin rapid expansion of production capacity, shipping high volumes (16–80 million per month) quantities of product manufactured using production tooling and processes which are being quickly "copied" into multiple modules of manufacturing capacity. Price per bit has "crossed over" the previous generation, which experiences a unit volume demand "peak" as it is replaced in the market. The ramp-level product generation is also "cut down" from the introduction-level generation design and manufacturing processes. Example: 1999/128Mb DRAM.

YEAR OF PEAK (DRAM)—Year in which the highest-volume DRAM generation is replaced by a next-generation product which is more cost-effective on a per-bit basis. After this cost-per-bit "cross-over" occurs volumes cease to grow, and then quickly drop, as the generation reaches the end of the life-cycle begun years earlier at its own introduction level. Typically this "peak" product generation will also be "cut-down" out of the present introduction-level generation design and process to minimize cost and maximize availability. However some portion of "peak" product capacity might also remain at the "ramp" chip size and technology to balance utilization of existing mature production tooling and process capacity. Example: 1999/64Mb DRAM.

YEAR OF INTRODUCTION (MPU)—Year in which the leading chip manufacturer supplies small quantities of engineering samples (<1K). These are provided to key customers for early evaluation, and are manufactured with qualified production tooling and processes. The introduction cost-performance MPU may be combined in a multi-chip module, along with L2 cache, in low-volume computer applications which demand high performance.

YEAR OF RAMP (MPU)—The year in which leading chip manufacturers begin rapid expansion of production capacity, shipping high volumes (2–10 million per month) quantities of cost-performance MPU product manufactured using production tooling and processes. As demand increases, the tooling and processes are being quickly "copied" into multiple modules of manufacturing capacity. Lower-volume, high-performance MPUs are also ramping concurrently as its co-existing cost-performance MPU core, but the L2 cache is now included on-chip but with twice the memory as its high-performance-generation predecessor.

YEAR OF PEAK (MPU)—An MPU generation experiences quicker and sharper unit volume demand "peak" as it is rapidly replaced in its primary computer market applications. High-performance MPUs peak in the same year as the cost-performance MPU that is used as the high-performance MPU core. Both cost-performance and high-performance MPU have shorter life-cycles than DRAM, and each is replaced rapidly by its respective higher functionality/performance inTER-generation MPU.

YEAR OF EMBEDDED (MPU)—Unlike DRAM products, the ramp-level MPU cost-performance product generation is not "cut down" from the overlapping introduction-level generation, and therefore cannot easily coexist in the same computer markets. Therefore, an MPU generation which is past the peak life-cycle stage will move into high-volume, but very low-cost, "embedded" applications as it shrinks to cost-effective levels.

Functions/Chip—The number of bits (DRAMs) or logic transistors (MPUs, application-specific integrated circuits [ASICs]) that can be cost-effectively manufactured on a single monolithic chip at the available technology level. Logic functionality (transistors per chip) include both SRAM and logic transistors. DRAM functionality (bits per chip) is based only on the bits (after repair) on a single monolithic chip.

Chip Size (mm^2)—The typical area of the monolithic memory and logic chip that can be affordably manufactured in a given year based upon the best available leading-edge design and manufacturing process. (Estimates are projected based upon historical data trends and the ITRS analyst consensus models).

Functions/cm²—The density of functions in a given square centimeter = ***Functions/Chip*** on a single monolithic chip divided by the ***Chip Size***. This is an average of the density of all of the functionality on the chip, including pad area and wafer scribe area. In the case of DRAM, it includes the average of the high-density cell array and the less-dense peripheral drive circuitry. In the case of the MPU products, it includes the average of the high-density SRAM and the less-dense random logic. In the case of ASIC, it will include high-density embedded memory arrays, averaged with less dense array logic gates and functional cores. Most typical ASIC designs will be slightly less dense than the high-performance MPUs, which are mostly SRAM.

DRAM Cell Array Area Percentage—The maximum practical percentage of the total DRAM chip area that the cell array can occupy at the various stages of the generation life cycle. At the introduction chip size targets, this percentage must be typically less than 70% to allow space for the peripheral circuitry, pads, and wafer scribe area. Since the pads and scribe area do not scale with lithography, the maximum cell array percentage is reduced in other inTRA-generation shrink levels (typically less than 55% at the production level, and less than 50% at the ramp level).

DRAM Cell Area (μm^2)—The measure of the maximum allowable DRAM memory bit cell area specified by the requirement to meet the target chip size and cell array area percentage requirements. May also be expressed as the cell area factor – number of equivalent units of area of a square of the DRAM half-pitch. Minimizing the area for the cell is in conflict with the desire to maximize the capacitance storage capability of the continuously shrinking cell. This creates a conflict between the technical feasibility of the cell area required to meet the economic constraints of the maximum allowable chip size.

DRAM Cell Area Factor—The measure of the maximum allowable DRAM memory bit cell area, expressed as the number of equivalent units of area of a square of the DRAM half-pitch.
Example: 1999: square of the half-pitch = $(180\ nm)^2$ = .032 μm^2; maximum cell area for 1Gb DRAM to be < 70% of total chip area = 0.26 μm^2; therefore, the maximum cell area factor = 0.26/0.32 = 8. The cell factor is also often expressed by equivalent aspect ratios of the half-pitch units (2×4 = 8, 2×3 = 6, 2×2=4, 1.6×1.6=2.5, etc.).

Usable Transistors/cm² (High-performance ASIC, Auto Layout)—Number of transistors per cm^2 designed by automated layout tools for highly differentiated applications produced in low volumes. High-performance, leading-edge, embedded-array ASICs include both on-chip array logic cells, as well as dense functional cells (MPU, I/O, SRAM, etc). Density calculations include the connected (useable) transistors of the array logic cells, in addition to all of the transistors in the dense functional cells. The largest high-performance ASIC designs will fill the available production lithography field.

CHIP AND PACKAGE—PHYSICAL AND ELECTRICAL ATTRIBUTES

Number of Chip I/Os - Total (Array) Pads—The maximum number of chip signal I/O pads plus power and ground pads permanently connected to package plane for functional or test purposes, or to provide power/ground contacts (including signal conditioning). These include any direct chip-to-chip interconnections or direct chip attach connections to the board (Package plane is defined as any interconnect plane, leadframe, or other wiring technology inside a package, i.e., any wiring that is not on the chip or on the board.). MPUs typically have a ratio of signal I/O pads to power/ground pads of 1:2, whereas the high-performance ASIC ratio is typically 1:1.

Number of Chip I/Os - Total (Peripheral) Pads—The maximum number of chip signal I/O plus power and ground pads for products with contacts only around the edge of a chip.

Pad Pitch—The distance, center-to-center, between pads, whether on the peripheral edge of a chip, or in an array of pads across the chip.

Number of Package Pins/Balls—The number of pins or solder balls presented by the package for connection to the board (may be fewer than the number of chip-to-package pads because of internal power and ground planes on the package plane or multiple chips per package).

Package cost (cost-performance)—Cost of package envelope and external I/O connections (pins/balls) in cents/pin.

Chip Frequency (MHz)

On-chip, local clock, high-performance—On-chip clock frequency of high-performance, lower volume microprocessors in localized portions of the chip.

On-chip, across-chip clock—On-chip clock frequency of microprocessors and ASICs for interconnect signals that run across the full width of the chip (Typically, this is lower than the localized clock performance due to capacitance loading of the long cross-chip interconnect.).

Chip-to-board (off-chip) speed (high-performance, reduced-width, multiplexed bus)—Maximum signal I/O frequency to specialized board reduced-width, multiplexed buses.

Chip-to-board (off-chip) speed (high-performance, peripheral buses)—Maximum signal I/O frequency to board peripheral buses of high and low volume logic devices.

Other Attributes

Lithographic Field Size (mm^2)—Maximum single step or step-and-scan exposure area of a lithographic tool at the given technology node.

Maximum Number Of Wiring Levels—On-chip interconnect levels including local interconnect, local and global routing, power and ground connections, and clock distribution.

FABRICATION ATTRIBUTES AND METHODS

Electrical D_0 Defect Density (d/m^{-2})—Number of electrically significant defects per square meter at the given technology node, production life-cycle year, and target probe yield.

Minimum Mask Count—Number of masking levels for mature production process flow with maximum wiring level (Logic).

MAXIMUM SUBSTRATE DIAMETER (MM)

Bulk or Epitaxial or Silicon-on-Insulator Wafer—Silicon wafer diameter used in volume quantities by mainstream IC suppliers. The ITRS timing targets, contributed by the Factory Integration Technology Working Group, are based on the first 20K wafer-starts-per-month manufacturing facility, versus the first-pilot-line timing target of the 1997 NTRS.

ELECTRICAL DESIGN AND TEST METRICS

Power Supply Voltage (V)

Minimum Logic V_{dd}— Nominal operating voltage of chips from power source for operation at design requirements.

Maximum Power

High-performance with heat sink (W)—Maximum total power dissipated in high-performance chips with an external heat sink.

Battery (W)—Maximum total power/chip dissipated in battery operated chips.

DESIGN AND TEST

Volume Tester Cost/Pin ($K/pin)—Cost of functional (chip sort) test in high volume applications divided by number of package pins.

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS
1999 EDITION

SYSTEM-ON-A-CHIP

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SYSTEM-ON-A-CHIP

Historically, the Roadmap has emphasized the technological limits of silicon production, leading to the specification of the most complex chips that can be developed in the categories of memory, microprocessor, and ASIC at a particular technology node. With the growing importance of high-volume consumer markets and the ability to integrate almost all aspects of a system design on a single chip, the ITRS has included an additional vehicle to capture the requirements of this important, emerging area. This vehicle is referred to as a System-On-a-Chip (SoC, sometimes called System LSI). Two classes of SoC can be distinguished by applications: the *mainstream, cost-driven* SoC (C-SoC) targeted towards high-volume consumer markets, and the *high-end, performance-oriented* SoC (P-SoC), targeted towards lower-volume, high-performance markets. The primary differences between these categories are illustrated in Table 8.

Table 8 Major Characteristics and Emphasis of SoC Classifications

CHARACTERISTIC	*C-SOC* *MAINSTREAM SOC*	*P-SOC* *HIGH-END SOC (FORMERLY ASIC)*
Major Drivers	Low-cost, low-power	Performance, complexity
Power	Lowest possible	Upper technological limits
Package	Very low cost	High-performance, expensive
Pins–I/Os	Few	Many

WHAT IS A SYSTEM-ON-A-CHIP?

There are a number of characteristics that distinguish an SoC, but the main consideration is that it is primarily defined by its cost rather than by technological limits. Rather than asking, "How complex a chip can I build?" and then asking, "How much will it cost?" (the P-SoC emphasis), in the C-SoC category the question most often asked is, "If my budget for this component is $N, how much capability (gates, memory, performance, and so on) can I expect to get?" The answer to this question is a complex combination of many factors. If one assumes a high-volume consumer part and so ignores nonrecurring engineering (NRE) costs related to design, then production costs include the fundamental technological factors contemplated in the ITRS (feature size, yield, field size, metal layers) as well as such factors as the cost of packaging and the cost of testing the SoC.

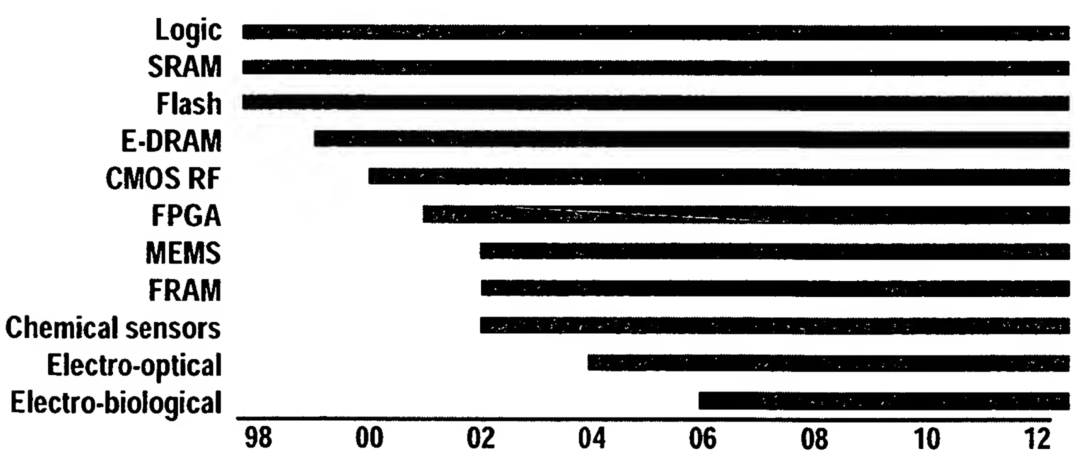

Figure 1 Technologies Integrated on SoC in the Standard CMOS Process

SoCs are also distinguished by other factors. As a *system*-on-a-chip, they are often mixed-technology designs, including such diverse combinations as embedded DRAM, high-performance or low-power logic, analog, radio frequency (RF), and even more esoteric technologies like Micro-electro Mechanical Systems (MEMS) and optical input/output.

In all categories of the Roadmap, design productivity is a key requirement. Design reuse will grow as a major tool in achieving the productivity requirements. This is particularly true for the SoC category, where time-to-market for a particular application-specific capability is a key requirement of the designs. The building blocks combined to form the SoC may be a controller core, embedded SRAM memory, and some dedicated logic. In some cases specific components/technological features may be added such as embedded Flash, embedded DRAM, MEMS, chemical sensors, or ferroelectric RAM (FRAM). The particular expectations for such mixed technologies are included in Figure 1. The number of such additional technological features on a specific SoC is likely to be limited to one or two for cost reasons.

For SoC, it is imperative that any additional technologies like those listed in Figure 1 be integrated into the standard CMOS logic process. Thus, process modules are needed that have little interference with the rest of the process and can be selected or de-selected freely depending on the application.

MAIN EMPHASIS—COST-BASED DESIGNS

The major new suggested emphasis of the SoC category is the C-SoC cost-based design.

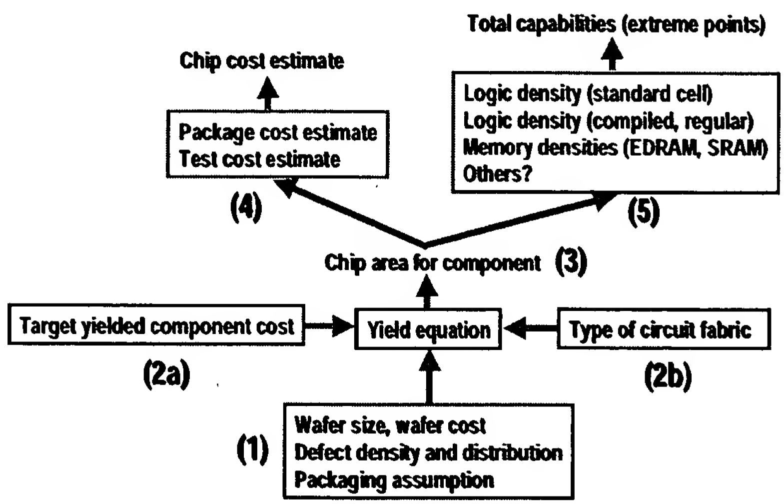

Figure 2 Possible Flow for Estimation of New Roadmap Entries

Given the nonlinear relationship between chip area and yielded die for a given technology node, as well as the post-processing yield enhancement techniques available for certain fabrics (such as DRAM repair), it is not as simple as determining a cost-per-mm^2 and then multiplying by chip area. For these reasons, we have approached the problem as outlined in Figure 2. Based on raw manufacturing data (1) and yield considerations for a particular class of circuit (2b), it is possible to predict the maximum yielded die area (3) of a particular class of circuit for given cost (2a). Given the likely I/O requirements and performance requirements of the circuit, package and test costs can be predicted, based on empirical data and projected new technology capabilities (4). Also predictable are required upper bounds for these aspects of the design, given a desire to maintain packaging and test at a particular percentage of overall chip cost (5).

Process technology is only one consideration that determines the cost-per-unit functionality of a particular family of circuits. Issues such as post-manufacture repair, test requirements, and binning play an important role in determining final cost. For a given process node, different circuit-styles, which have particular

functional density and yields, are known as particular *circuit fabrics*. Table 9 contains a partial list of such fabrics, some of which have reasonable cost models. However, some cost models are either not available or remain a difficult research problem to determine.

Table 9 Example of Circuit Fabrics

Hand-designed static CMOS logic
Standard-cell auto place and route logic
Regular logic structures (datapath)
Dynamic CMOS logic
SRAM
Embedded DRAM
Integrated CMOS analog
Integrated CMOS RF circuits
Processor cores

There are many factors for each fabric that effect cost. The most well-defined aspect of analysis, based on data already present in the ITRS, is the expected manufacturing cost for a particular size of chip and for a particular class of circuit (fabric). This data is projected in the ITRS for DRAM, hand-crafted logic, and auto-placed-and-routed logic—the circuit fabrics that have approximate cost projections, as shown in Figure 3.

Using this information, along with the memory and logic density numbers in the ITRS Overall Technology Characteristics tables, it is possible to estimate the capabilities of such a chip for various combinations of logic and memory.

From this information, a series of plots for each technology node of the form shown in Figure 3 could be developed.

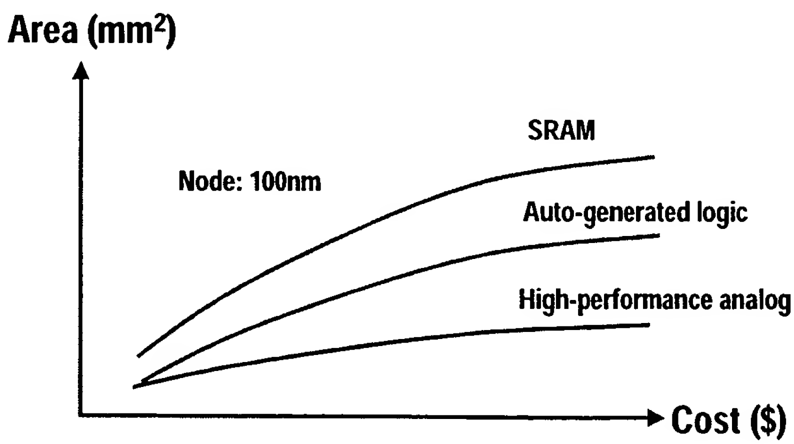

Figure 3 Schematic Representation of Area-cost Curves for Particular Circuit Fabrics at a Technology Node

PROGRAMMABLE VERSUS HARD-WIRED

Another factor to be considered in the context of this new SoC category is that of programmability (via software or programming gates, as in an field programmable gate array (FPGA)). The SoC provides a useful vehicle for introducing the notion of embedded software and its implications in the Roadmap. This aspect is of particular importance for design and test, as the methodological implications of a programmable versus nonprogrammable (hard-wired) implementation of an SoC are very significant. In the consumer marketplace, as well as in the high-performance ASIC markets, there are legitimate reasons for employing

both approaches, having to do with extreme points of performance, cost, and power dissipation. Some example applications in each category are listed in Table 10 to illustrate the point.

Table 10 Example Applications of Programmable and Nonprogrammable SoCs

	PROGRAMMABLE	*NON-PROGRAMMABLE*
C-SoC	Low-cost PDA chip Digital camera chip FPGA Microcontroller-based SoC	Sensor interface Low-cost home RF front end
P-SoC	High-end game platform Set-top box High-end network router DSP	Read-channel for disc drive High-performance network chip

PROCESS REQUIREMENTS FOR ADVANCED TECHNOLOGIES

It is expected that SoC will continue to use a number of exotic circuit fabrics, including those listed in Table 9 and some of the technologies listed in Figure 1. It will require the integration of technologies that are not part of the basic CMOS flow. In all cases, the goal should be to add additional steps to the CMOS process to incorporate these additional capabilities without altering the basic CMOS flow. The designer will then be able to choose the additional fabrics needed (such as RF and Flash memory) and estimate their impact on overall chip cost, performance, reliability, and power without disturbing the basic cost of the standard CMOS portion of the chip.

Examples of specific technologies that might be developed to support the integration of these mixed circuit fabrics include the following:

- Special wiring and metallization for high-performance analog and RF
- Special upper-layer processes and passivation for integrated MEMS
- Special localized processing for integrated optical sensors
- Use of discretionary implants for critical low-power regions of a chip (such as dual threshold)

Other process adjustments may be necessary and may be identified in the future.

The process complexity will be a major factor in the cost of the SoC applications. The more combinations of technologies that are assembled on a single chip, the more complex the processing will be. The total cost of processing will be hard to predict for these new materials and combinations of processing steps but an attempt at estimating this is shown in Table 11.

Table 11 shows an estimate of the increasing complexity of the new combinations of technologies in the units of extra lithography mask levels necessary to add this technology to the standard CMOS logic technology. The data in this table illustrates that the embedded additions of technologies add significant processing complexity and are compounded as the technologies are added together. The addition of more than two embedded technologies would increase the complexity incrementally.

Table 11 Added Process Complexity for SoC Technologies

C st of adding technology in units of mask levels	Logic	SRAM	Flash	DRAM	CMOS RF	FPGA	MEMS	FRAM	Chemical Sensors	Electro Optical
Logic	0									
SRAM	1–2	0								
Flash	4	3–4	0							
DRAM	4–5	3–4	7–9	0						
CMOS RF	3–5	5–9	6–9	6–10	0					
FPGA	2	2–4	4–6	3–7	5–7	0				
MEMS	2–10	3–12	6–14	6–15	5–15	4–12	0			
FRAM	4–5	3–4	7–9	2–3	7–10	6–7	9–15	0		
Chemical Sensors	2–6	3–7	6–10	6–11	5–11	4–8	4–16	6–11	0	
Electro-Optical	5–8	6–9	9–12	9–13	8–12	7–10	7–18	9–13	7–14	0

PACKAGING CONSIDERATIONS

SoC designs will require a wide range of packaging solutions and will be responsible for driving many aspects of the packaging industry from low-cost, low pincount packages for C-SoC, to high-performance, high pincount packages for P-SoC. In addition, the mix of technologies, from analog and RF to optical and even MEMS devices will require a broad range of special packaging options. Some of the issues in each of these areas are discussed in this section.

SYSTEM-ON-A-CHIP PACKAGING

The ever-increasing CMOS density is a very important driving force for SoC in low-cost and hand-held applications. For example, when the lithography feature size improves in the succeeding generation, the chip size of a standalone micro-controller core may be limited by the pad pitch and pad count, and will not reduce accordingly. Very often, the combination of a controller core plus a digital signal processor (DSP) core may result in a chip I/O count less than either the controller or the DSP core alone and may still fit in such an I/O pad-limited chip area. The cost of two packages is replaced by one of equal or less cost (the package cost becomes less than one half), and the printed wiring board area being occupied is reduced. This also eliminates many of the off-chip driver circuits and the associated delay time and power consumption. Furthermore, the availability of on-chip wiring may allow substantial increase in the data bandwidth between these two cores, thus improving the performance. Similar benefit may also be achieved by the integration of A/D and D/A converters into the DSP and controller cores after one more technology generation. In some applications, programmability is essential, which may be achieved by a small embedded-Flash memory.

The main challenges in SoC packaging are in maintaining signal integrity and verification. Techniques like de-coupling, shielding, and better grounding will be necessary to handle mixed analog and digital signals in a minimum size package. Design emulation and verification of intent will require early packaging involvement in SoC design. The complexity of testing at both the wafer probe and package levels should be considered at the design stage.

In some applications, the chip size is not limited by the I/O pads, even when it should decrease in the succeeding generation. The reduction in chip size will decrease the chip cost. The integration of two cores into one chip may impact the chip yield and increase the overall chip cost. The replacement of two packages by one of equal or less I/O leads may cut the packaging cost by more than a factor of two. The cost of chip plus package may decrease or increase, depending on the individual application. However, the elimination of the off-chip driver delay and power consumption, the reduction in the wiring board area, and the

possibility of improved bandwidth between the two cores, may become important considerations for the adoption of the performance-oriented SoC applications.

RF AND MIXED-SIGNAL PACKAGING

The challenges in this area will become important as low-cost mobile and high bandwidth products drive across several market segments. The increasing performance of silicon ICs will enable lower cost solutions in the frequency domain below 10GHz. GaAs ICs, and now SiGe ICs will be used for higher frequency or higher power applications. Signal integrity and cost issues become dominant. Flip chip attachment to package and embedded passives on the package will be key enabling technologies to package level performance. Low inductance and high-density packages like fine pitch ball grid array (FBGA)/chip scale packaging (CSP) will enable designers to use lower cost partitioning solutions than the traditional ceramic modules.

Integrated modeling and simulation tools are required to decrease design cycle time to acceptable levels. Performance, physical size, and cost driven integration will continue to arrive at a single chip radio that combines memory, processor, and mixed-signal functions, as discussed above. Fast design cycle time and accurate simulation at both the chip and package levels are enablers of this integration. High-speed test and higher level of functional test at the package level also become development challenges. MEMS will be used in the fabrication of filter, switch, oscillator, and other components in the next 2–4 years. They offer the benefit of small size, low insertion loss, low power consumption, integration with ICs, and the potential of low cost with batch fabrication. Reliability, potential temperature sensitivity, and hermetic/vacuum packaging of MEMS devices are key development challenges.

MULTI-CHIP PACKAGES, MULTI-CHIP MODULES, AND SYSTEM-IN-A-PACKAGE

The production volumes of multi-chip modules (MCMs) have lagged behind expectations in the marketplace but tracked the acceptance of the flip chip bump technology by the system houses. However, few-chip modules (2–3 chips) are in volume production, and by extending the definition of multi-chip packages (MCPs) to include RF and mixed-signal products, it is now expected that 4–5 chips (or more complex) modules will be common in the next few years. The MCP is often referred to as a system-in-a-package (SiP), which primarily addresses time-to-market needs for mixed-technology, highly-complex systems. As the SoC becomes feasible both technically and economically, the number of ICs on an MCP will most likely be reduced to realize both product cost and size gains.

For certain limited volume, high-performance products the system packaging technology of choice will still be classical (complex) MCMs because they provide the best cost and performance package solution. Very often, tens of logic and memory chips with high I/O lead count are placed at close proximity to minimize the time-of-flight delay between chips. In fact, the wiring capacity needed to implement such systems on ceramic MCMs is one order of magnitude larger than the plastic MCM technology can support today. The important considerations are the overall system cost, the system performance needs, and the reliability of the CMOS based system, not just the cost of the packaging alone. Because the DCA for extremely high I/Os is available for ceramic MCMs now, and is expected for plastic-based MCMs in the future, the whole system can be packaged in a very small area that still permits the lowering of the junction temperature through standard refrigeration techniques. This capability increases the reliability of the CMOS chips by 3–5 times and the performance of the CMOS chips by up to 15%. Since the drive for better system reliability is expected to increase in the future, the extended used of MCMs in the system design will follow.

In general, MCP/MCM/SiP will be driven by densification and cost reduction for low end C-SoC products, and by densification and performance for high end P-SoC products. Flip-chip technology will soon be used pervasively for MCP/MCM/SiP technology (whether few-chip MCP or classical MCM) so that enabling solutions for flip-chip technology (such as underfill) become among the key enabling solutions for MCP/MCM/SiPs as well. Other critical, enabling solutions for MCP/MCM/SiPs include:

- Special physical design tools that facilitate performance-driven place-and-route for simple or complex MCP/MCM/SiPs

- High density substrate and metallization technology
- Low-cost, available known good die (KGD). Chip reworkability and module testing will be major factors in determining the feasible complexity of multi-chip modules.

TEST FOR SOC

Historically, IC testing has been performed by automatic test equipment (ATE) that applied external stimulate to devices under test (DUTs) followed by observation of the response that was compared with stored expected results. The ATE were either purely digital, or they also contained analog instruments that were synchronized to the digital. Recently, a number of ATE manufacturers have begun selling "SoC testers" that are capable of testing DUTs containing digital, analog, memory, and RF elements; however, the tests are all externally applied.

It is becoming clear that if SoCs are ultimately implemented as a collection of heterogeneous circuit fabrics (from analog and RF to high-performance logic and memory), it will be necessary for test methodologies to be developed specific to a particular fabric and integrated into the fabric design flow. In other words, from a performance perspective and a cost perspective, an on-board form of test is essential. This prediction is also evident in the *Test* chapter of the ITRS, where it is predicted that traditional test methods will give way to ATE that stimulate testing circuits designed within the DUT. In the *Test* chapter, a low-cost ATE is described that is able to load digital SCAN chains within a DUT and observe the result. This digital tester has roughly 64-signal pins plus hundreds of lower-performance pins that simply observe whether or not most of the DUT pins can actively swing between 1 and 0 states. Built-in-self-test (BIST) is also being used to test embedded memory, but the art of BIST for analog or RF circuits is still in its infancy.

If the SoC is programmable, or contains a controller of some form, it is most likely that an hierarchical form of test will be employed in future systems. The programmable component will test itself and then be responsible for the coordinated testing of the other on-chip subsystems, possibly via some form of BIST in the component itself. Both performance issues as well as cost issues will motivate the final choices.

Table 12 on SoC Test technology requirements highlights six areas where solutions must be pursued or there are no know solutions for solving the complex testing issues that are arising with SoCs. These are as follows:

- New fault models will be required to handle crosstalk and new failure modes that will result from multi-level metal structures. The "stuck-at" single fault model is becoming less effective for computing expected test results for complex SoC fabrics.
- New test methods involving BIST are required that will allow low-speed, low-cost ATE to test the digital portions of SoCs at high speed.
- New Design for Testability techniques are required for analog testing, higher-level behavioral testing and others.
- BIST techniques must be developed to include memory testing with self-repair for redundant configurations, repair of logic circuits, analog, and others.
- Standards must be developed for test programming languages, test data, and fault models so that test reuse is possible to shorten SoC test development time.
- Test costs must be reduced through test time reduction, faulty chip repair, and new failure analysis techniques.

Table 12a SoC Test Technology Requirements—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
Fault Model							
Stuck-at fault model	Single fault	Single fault	Single fault	Single fault	Single fault	Single fault	Single fault
Delay fault model	Gate/path delay	Gate/path delay	Gate/path delay	Gate/path delay	Gate/path delay	Gate/path delay	Gate/path delay
New fault model (crosstalk and others)			XX	XX	XX	XX	XX
New fault model (RT level fault model)				XX	XX	XX	XX
Test Method							
Low cost test technique for embedded DRAM (BIST + direct access)		XX	XX	XX	XX	XX	XX
High speed test using low speed tester (BIST with on chip clock generator, test circuit on tester board)			XX	XX	XX	XX	XX
Test technique for asynchronous circuit			XX	XX	XX	XX	XX
Crosstalk test			XX	XX	XX	XX	XX
Test strategy for IP core-based design (test control integration, test scheduling)			XX	XX	XX	XX	XX
Whole chip path delay test				XX	XX	XX	XX
IDDQ test for low-Vth circuit				XX	XX	XX	XX
Low power consumption test technique (test pattern adjustment, test scheduling)				XX	XX	XX	XX
ATPG for interleave at-speed tester				XX	XX	XX	XX
Self diagnostic technique on maximum frequency							XX
DFT							
DFT at gate level design (scan design)	XX	XX	XX	XX	XX	XX	XX
DFT at RTL design (DFT, testability analysis, overhead estimate)	XX	XX	XX	XX	XX	XX	XX
DFT at RTL design (fault simulator, ATPG)				XX	XX	XX	XX
DFT at higher level design (behavior level, hardware/software co-design)							XX
DFT at higher level design (high level synthesis with testability analysis)							XX
DFT for analog / mixed-signal	Block isolation test	Block isolation test	BIST, JTAG	BIST, JTAG	BIST, JTAG	BIST, JTAG	BIST, JTAG
Test integration (IP core isolation test)	XX	XX					
Test integration (test integration tool supporting cost-, area-, speed- and power-driven DFT selection)			XX	XX			
Test integration (fully automated cost-, area, speed- and power-driven test integration tool)					XX	XX	XX
DFT circuits generation (memory BIST, logic BIST, JTAG)	XX	XX	XX	XX	XX	XX	XX
At-speed test with low speed tester			XX	XX	XX	XX	XX

XX—applicable node years

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 12a SoC Test Technology Requirements—Near Term (continued)

YEAR / TECHNOLOGY NODE	1999 / 180 nm	2000	2001	2002 / 130 nm	2003	2004	2005 / 100 nm
BIST							
Embedded memory BIST	Restricted use	Restricted use	Practical use	Practical use	Practical use	Practical use	Practical use
Embedded memory BIST (redundant configuration, self repair, many kinds of test algorithm)			XX	XX	XX	XX	XX
Logic BIST	Restricted use	Restricted use	Practical use for stuck-at faults	Practical use for stuck-at faults	Practical use for stuck-at faults	Practical use for stuck-at faults	Practical use for stuck-at faults
Logic BIST (high fault coverage, at-speed test on system operation, test time restraint, low power, low area overhead)			XX	XX	XX	XX	XX
Logic BIST (faulty chip repair)			XX	XX	XX	XX	XX
Analog/mixed-signal BIST			Restricted use (PLL, ADC)	Restricted Use (PLL, ADC)	Restricted Use (PLL, ADC)	Restricted Use (PLL, ADC)	Restricted Use (PLL, ADC)
Others							
Standardization							
Test data	WGL, VCD, STIL	WGL, VCD, STIL	STIL on EDA/ATE	STIL on EDA/ATE	STIL on EDA/ATE	STIL on EDA/ATE	STIL on EDA/ATE
Test method/test interface	P1500	P1500	P1500 on IP core/ EDA	P1500 on IP core/ EDA	P1500 on IP core/ EDA	P1500 on IP core/ EDA	P1500 on IP core/ EDA
Fault model/fault coverage	Stuck-at model	Stuck-at model	Standard fault models, SoC level coverage	Standard fault models, SoC level coverage	Standard fault models, SoC level coverage	Standard fault models, SoC level coverage	Standard fault models, SoC level coverage
Test Cost							
Test time reduction (full-scan IDDQ)	XX	XX					
Test time reduction (IP core-based design)			XX	XX	XX	XX	XX
Faulty chip repair (memory BISR)			XX	XX	XX	XX	XX
Faulty chip repair (logic BISR and others)							
Failure Analysis							
Electron beam tester	XX	XX					
Chip backside analysis	XX	XX	XX				
Design/package for backside analysis				XX	XX	XX	XX
Integrated failure analysis environments				XX	XX	XX	XX
Test generation for failure analysis				XX	XX	XX	XX
Failure analysis for analog circuits							XX
BIST pattern exchange technique							XX

XX—applicable node years

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 12b SoC Test Technology Requirements—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
Fault Model			
Stuck-at fault model	Single fault	Single fault	Single fault
Delay fault model	Gate/path delay	Gate/path delay	Gate/path delay
New fault model (crosstalk and others)	XX	XX	XX
New fault model (RT level fault model)	XX	XX	XX
Test Method			
Low cost test technique for embedded DRAM (BIST + direct access)	XX	XX	XX
High speed test using low speed tester (BIST with on chip clock generator, test circuit on tester board)	XX	XX	XX
Test technique for asynchronous circuit	XX	XX	XX
Crosstalk test	XX	XX	XX
Test strategy for IP core-based design (test control integration, test scheduling)	XX	XX	XX
Whole chip path delay test	XX	XX	XX
IDDQ test for low-Vth circuit	XX	XX	XX
Low power consumption test technique (test pattern adjustment, test scheduling)	XX	XX	XX
ATPG for interleave at-speed tester	XX	XX	XX
Self diagnostic technique on maximum frequency	XX	XX	XX
DFT			
DFT at gate level design (scan design)	XX	XX	XX
DFT at RTL design (DFT, testability analysis, overhead estimate)	XX	XX	XX
DFT at RTL design (fault simulator, ATPG)	XX	XX	XX
DFT at higher level design (behavior level, Hardware/software co-design)	XX	XX	XX
DFT at higher level design (high level synthesis with testability analysis)	XX	XX	XX
DFT for analog / mixed-signal	BIST, JTAG	BIST, JTAG	BIST, JTAG
Test integration (IP core isolation test)			
Test integration (test integration tool supporting cost-, area-, speed- and power-driven DFT selection)			
Test integration (fully automated cost-, area-, speed- and power-driven test integration tool)	XX	XX	XX
DFT circuits generation (memory BIST, logic BIST, JTAG)	XX	XX	XX
At-speed test with low speed tester	XX	XX	XX

XX—applicable node years

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 12b SoC Test Technology Requirements—Long Term (continued)

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
BIST			
Embedded memory BIST	Practical use	Practical use	Practical use
Embedded memory BIST (redundant configuration, self repair, many kinds of test algorithm)	XX	XX	XX
Logic BIST	Extension of handling fault model	Extension of handling fault model	Extension of handling fault model
Logic BIST (high fault coverage, at-speed test on system operation, test time restraint, low power, low area overhead)	XX	XX	XX
Logic BIST (faulty chip repair)	XX	XX	XX
Analog/mixed-signal BIST	Total use	Total use	Total use
Others	Tester on chip	Tester on chip	Tester on chip
Standardization			
Test data	Analog data	Analog data	Analog data
Test method/test interface	Automated SoC test integration	Automated SoC test integration	Automated SoC test integration
Fault model/fault coverage	New standard fault model, its coverage	New standard fault model, its coverage	New standard fault model, its coverage
Test Cost			
Test time reduction (full-scan IDDQ)			
Test time reduction (IP core-based design)	XX	XX	XX
Faulty chip repair (memory BISR)	XX	XX	XX
Faulty chip repair (logic BISR and others)	XX	XX	XX
Failure Analysis			
Electron beam tester			
Chip backside analysis			
Design/package for backside analysis	XX	XX	XX
Integrated failure analysis environments	XX	XX	XX
Test generation for failure analysis	XX	XX	XX
Failure analysis for analog circuits	XX	XX	XX
BIST pattern exchange technique	XX	XX	XX

XX—applicable node years

Solutions Exist   *Solutions Being Pursued*   *No Known Solutions*

International Technology Roadmap for Semiconductors
1999 Edition

Design

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DESIGN

SCOPE

The objective of the semiconductor business is to produce chips that create profit for integrated circuit manufacturers, their customers, and their suppliers and strategic partners. The increased difficulty in designing, verifying, and testing these chips has become a larger barrier to achieving this objective than providing the technology for manufacturing them. This chapter describes the challenges in producing correct, performing designs and potential solutions for meeting them. While test equipment and the test of manufactured chips is covered elsewhere, this *Design* chapter addresses design for testability, including built-in self test (BIST). As in the other areas covered, both advances in and roadblocks to technology solutions create problems and opportunities in design.

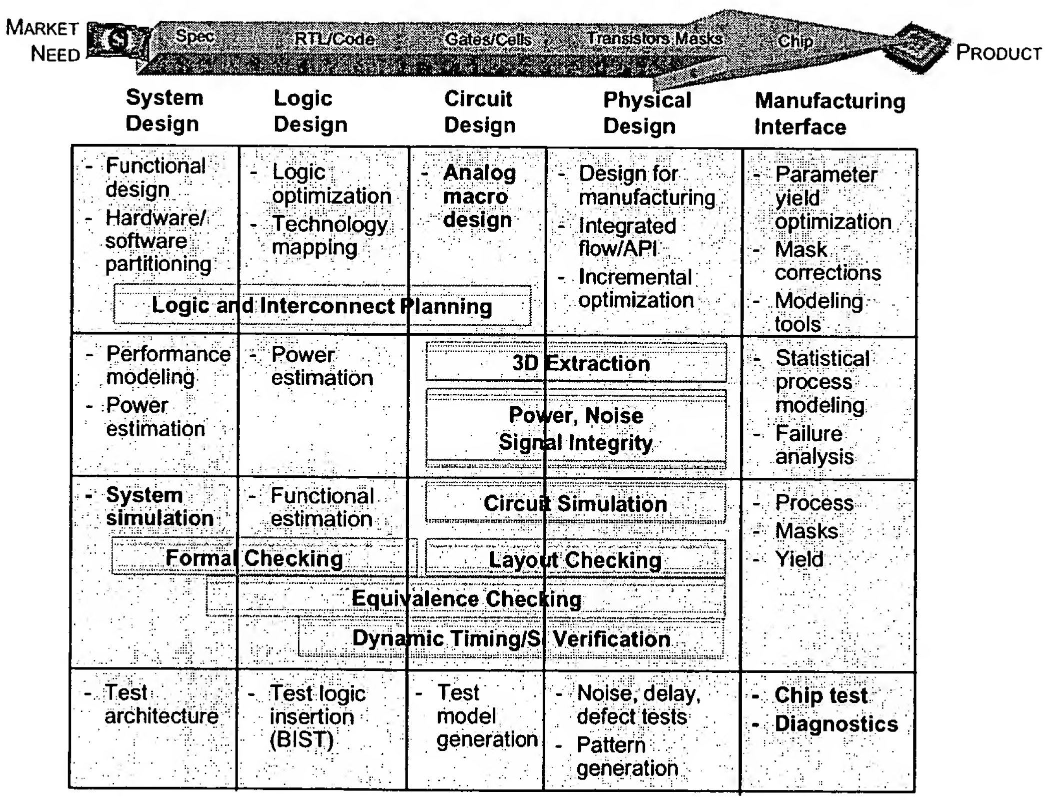


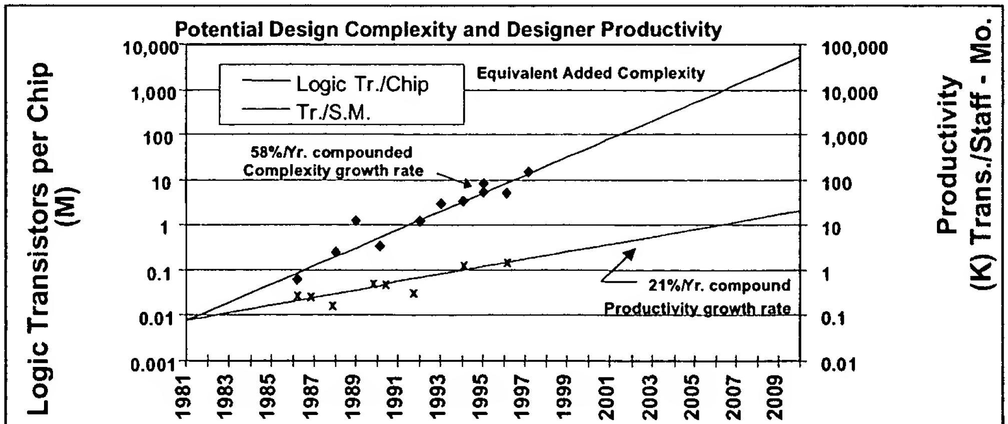
Figure 4 Issues in IC Design

The increasing complexity of design requires a corps of highly skilled and more broadly trained designers, and computer-aided design tools that take into account factors that could be ignored in previous technology generations. Figure 4 illustrates that tools, which earlier could concentrate on discrete parts of the design problem, now must be aware of a broader range of factors. For example, logic synthesis tools now must take interconnect and physical placement into account and increasingly accommodate the transistor-level properties of dynamic circuit families and the noise effects at smaller feature sizes and higher frequencies. The design flow must assure functional correctness and timing, power, reliability, manufacturability, signal integrity, and testability requirements. Thus, design complexity increases superexponentially, but automated

tools are handicapped by having to run on the previous generation of computing equipment. This complexity has a similar effect on designers (whose abilities are not tracking the Moore curve), with distinctions being blurred between logic design, layout, and circuit design.

As designs move from digital microprocessors and application-specific integrated circuits (ASICs) to system-on-a-chip (SoC), designers and design tools also encounter complex embedded software, more heterogeneous systems, and the challenges of providing a diverse range of components on a single chip. Analog and mixed-signal, radio frequency (RF), microelectromechanical systems (MEMS), electro-optical, electro-biological, and other nontraditional elements arise from and give rise to changes in technology. With this rapid rise in heterogeneity, technology advances, and new product requirements, reuse of already designed intellectual property (IP), once considered to be a mitigating factor in design productivity, becomes difficult. Moreover, incorporation of several separately-designed components on a chip requires significant integration and verification cost.

The rapidly changing technological environment also shrinks product life cycles, making time to-market one of the most critical issues for semiconductor customers. This demand is driven by growth of personal information flow through wired and wireless voice and data communication, and the internet. There is great pressure to reduce the total time to create a chip for products that are not obsolete before they are brought to market. This time is dominated by the system design and verification phase. Investment in technology improvements has dominated product creation resources, and design productivity has not been able to keep pace with transistor density growth. Figure 5 indicates the growing productivity gap between transistors available and those which can be designed in microprocessors. As noted above, design reuse addresses only part of the productivity gap. Increase in design team size has problems with respect to productivity of large groups and is limited by integration and software issues.



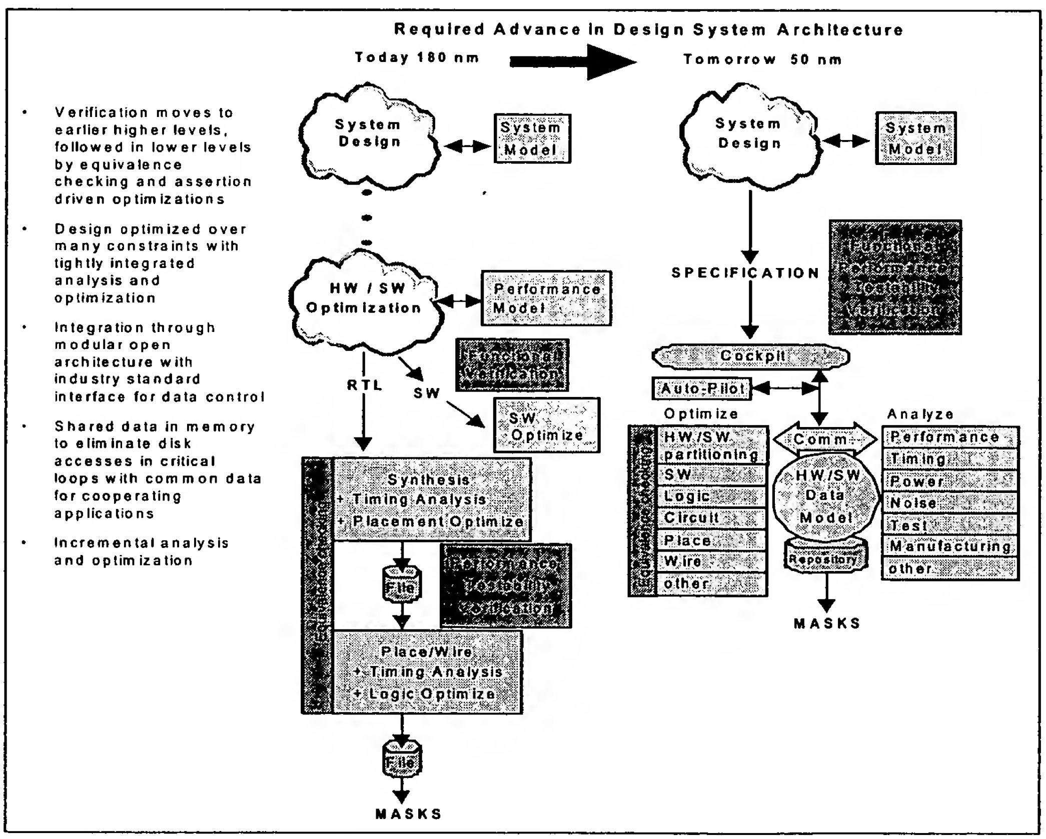
Year	Technology	Chip Complexity	Frequency	3 Yr. Design Staff	Staff Cost*
1997	250 nm	13 M Tr.	400	210	90 M
1998	250 nm	20 M Tr.	500	270	120 M
1999	180 nm	32 M Tr.	600	360	160 M
2002	130 nm	130 M Tr.	800	800	360 M

* @ $150K / StaffYr. (In 1997 Dollars)

Figure 5 The Design Productivity Gap

As time-to-market issues and system-on-a-chip become more common, embedded software emerges as a key design problem. The software content of products and its cost continues to rise. Issues surrounding this include high-level architectural design space exploration; analysis of the tradeoffs (design cycle time, performance, cost) of doing designs in hardware and software; high level design planning and estimation; hardware/software co-design at all design levels; and difficult verification and analysis issues. Software reliability becomes a greater factor, especially in critical applications and in distributed systems. Software, previously designed to run on a dedicated processor now runs in a global, interconnected environment with open systems. High-level design and the accompanying design automation tools are often considered key to design productivity improvement; however, to avoid frequent rework and iteration, decisions made at higher levels of design must be based on accurate estimation of the effects of lower level decisions, and/or must permit later adjustments to logical and physical factors. Figure 6 illustrates the transition of design systems from the traditional chart in which design proceeds independently at discrete levels, to an integrated system in which logical, physical, layout, and other tools can operate together. The designer will manipulate controls invoking automated design tools with "autopilot" aids in a cockpit setting.

Finally, it should be noted that the *Design* chapter of the ITRS, while increasingly important to the overall effort and time-to-market required to produce products and profit, is fundamentally different from the technology roadmap chapters, especially regarding the alignment of required design techniques to technology nodes. Technology advances tend to occur in discrete increments when all needed elements can be put in place in manufacturing. However, improvements in design techniques or the design process can normally be put in place when developed and can lead to improved productivity, or quality, or overall cost reduction immediately.



HW/SW—hardware/software

Figure 6 Required Changes in Design System Architecture

DIFFICULT CHALLENGES

Design challenges come about because of increases in the complexity of the component being designed; the technology in which it is being designed; and the tools used to design it. The system size, in terms of number of transistors and complexity of embedded software, is increasing exponentially. Additionally, the number of factors that designers and design tools must take into account as system heterogeneity increases and feature size decreases also is going up. Figure 7 indicates a range of factors that must be considered.

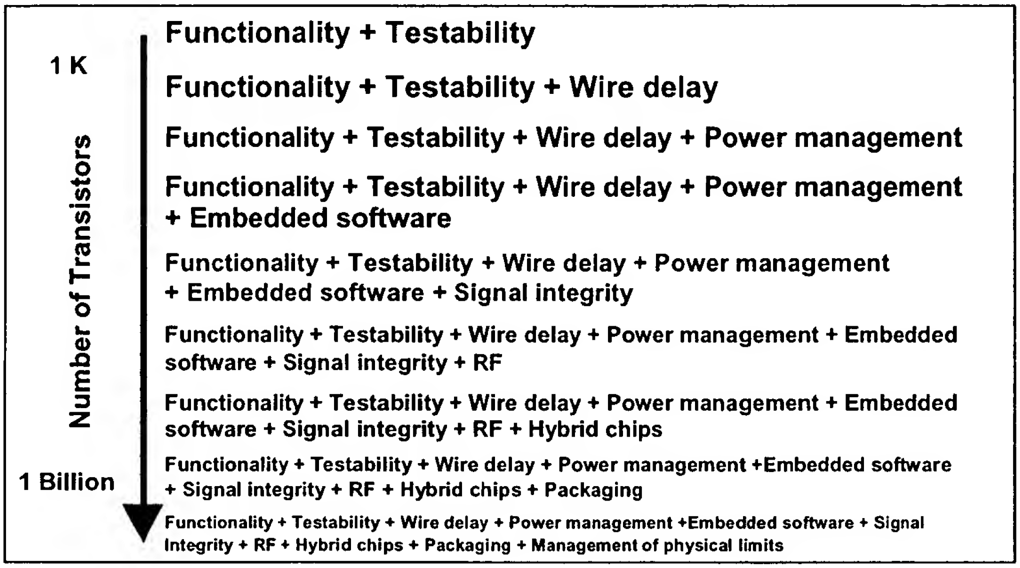


Figure 7 Superexpoenetially Increasing Design Complexity

Table 13, describing the difficult challenges in design, is grouped according to the drivers giving rise to five different complexity scales, and is ordered by immediacy of need. *Silicon complexity* is brought about by technology advances—smaller feature sizes not only allow more devices, but bring effects previously able to be ignored to prominence. *System complexity* has enabled this increase in capacity. The driver for system complexity is consumer demand for applications with increasing function leading to shorter time-to-market and lower cost. *Design procedure complexity* increases because of both technology and system factors. And the *verification and analysis*, and *test and testability*, of chips, packages, and entire products also become more complex.

TECHNOLOGY REQUIREMENTS

Table 14 illustrates the need to greatly increase designer productivity if the advances of technology are to be realized in actual designs. The solutions for achieving these numbers are greatly dependent on the application being designed—high degrees of design reuse, reliance on software and memory on-chip, and improved design tools are all attempts at bridging the productivity gap. The assumptions in the table are for design cycles to decrease slightly, and design teams to remain fixed at about 50 designers for ASICs and 300 designers for microprocessors. Increasing the team sizes beyond this is difficult because of the increased human communication problems that are introduced without methodologies to address them.

Table 13 Design Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥ 100 nm / THROUGH 2005	SUMMARY OF ISSUES
Silicon complexity	Large numbers of interacting devices and interconnects
	Impact of signal integrity, noise, reliability, manufacturability
	Power and current management; voltage scaling
	Need for new logic families to meet performance challenges
	Atomic-scale effects
	Alternative technologies (such as copper, low κ dielectric, SOI)
System complexity	Embedded software as a key design problem
	System-on-a-chip design with a diversity of design styles (including analog, mixed-signal, RF, MEMS, electro-optical)
	Increased system and function size
	Use of open systems and incorporation into global networks
	Integrated passive components
Design procedure complexity	Convergence and predictability of design procedure
	Core-based, IP-reused designs and standards for integration
	Large, collaborative, multi-skilled, geographically distributed teams
	Interacting design levels with multiple, complex design constraints
	Specification and estimation needed at all levels
	Technology remapping or migration to maintain productivity
Verification and analysis complexity	Formal methods for system-level verification
	System-on-a-Chip specification
	Early high-level timing verification
	Core-based design verification (including analog/mixed-signal)
	Verification of heterogeneous systems (including mixed-signal, MEMS)
Test/testability complexity	Quality and yield impact due to test equipment limits
	Test of core-based designs from multiple sources (including analog, RF)
	Difficulty of at-speed test with increased clock frequencies
	Signal integrity testability
FIVE ADDITIONAL DIFFICULT CHALLENGES < 100 nm / BEYOND 2005	
Silicon complexity	Uncertainty due to manufacturing variability
	Uncertainty in fundamental chip parameters (such as signal skew)
	Design with novel devices (multi-threshold, 3D layout, SOI)
	Soft errors
System complexity	Total system integration including new integrated technologies (such as MEMS, electro-optical, electro-chemical, electro-biological)
	Design techniques for fault tolerance
	Embedded software and on-chip operating system issues
Design procedure complexity	True one-pass design process supporting incremental and partial design specification
	Integration of design process with manufacturing to address reliability and yield
Verification and analysis complexity	Physical verification for novel interconnects (optical, RF, 3D) at high frequency
	Verification for novel devices (nanotube, molecular, chemical)
Test/testability complexity	Dependence on self-test solutions for SoC (RF, analog)
	System test (including MEMS and electro-optical components)

κ—dielectric constant *SOI—silicon on insulator* *IP—intellectual property*

Table 14a Design Technology Requirements—Near Term

YEAR *TECHNOLOGY NODE*	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*
MPU new design cycle (months)	36	36	36	32	32	32	30
MPU transistors per designer-month (300-person team) (thousand)	2	3	4	7	10	15	20
ASIC new design cycle (months)	12	12	12	12	12	12	12
ASIC transistors per designer-month (50-person team) (million)	0.3	0.4	0.5	0.7	1.0	1.3	1.8
Portion of verification by formal methods	15%	15%	15%	20%	20%	20%	30%
Portion of test covered by BIST	20%	20%	20%	30%	30%	30%	40%

Table 14b Design Technology Requirements—Long Term

YEAR *TECHNOLOGY NODE*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
MPU new design cycle (months)	28	26	24
MPU transistors per designer-month (300-person team) (thousand)	65	200	600
ASIC new design cycle (months)	11	10	9
ASIC transistors per designer-month (50-person team) (million)	5	13	36
Portion of verification by formal methods	40%	50%	60%
Portion of test covered by BIST	50%	60%	70%

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

SYSTEM-LEVEL DESIGN

Design is bounded by two endpoints, (1) at the highest level is system design, where architecture must implement the functions needed for the end product, and (2) at the lowest level are primitive building blocks—logic gates, amplifiers—controlled largely by the underlying device technology. Thus, overall system design is the creation of complex architectures using primitive building blocks facilitated by computer aided design (CAD) automation tools. This conceptual picture is significant, because system performance is a strong function of primitive circuit building blocks, and these are rapidly reaching their performance and functionality limits as technology scales into the deep submicron regime. In addition to impending technology limits, system complexity is also growing rapidly as systems become more capable and include more complex algorithms and software as part of large distributed systems. All these factors have serious consequences for system design.

System design has two definitions. It is the development of new architectures and algorithms for complex applications in the context of limited technology capabilities (design). Also, it is the process of creating a system, using the CAD methodology and tools that assist the designer in assuring that all constraints are met in a feasible, near-optimal implementation (design automation).

The "design" portion of system design pertains to the following:

- exploration of the design space at a high level to compose an overall architecture—including *circuit blocks, software*, and *communication* that implement the *algorithms* that accomplish the system function.
- exploitation of the opportunities/limitations of available silicon and packaging technology options and decomposition of the system into a manageable hierarchy of smaller subsystems.

The "design automation" portion of system design

- encompasses specification development, requirements and constraint capture, algorithm tradeoff, initial architecture partition and budgeting, including high-level block and wire floorplanning.
- produces an initial specification of partitioned, smaller blocks and their respective interconnect elements. Each block or interconnect element is budgeted and floorplanned on a global basis.

The boundary between pure digital design and circuit design is changing. For example, placement and interconnect delays (which can only come from physical design) must be considered when trying to bring the logic design to timing convergence. "Logic synthesis" must become more focused on cell selection and optimization in light of these physical constraints.

Similarly, the boundary between systems and digital design is blurring. Timing boundaries and discrete logic specification should appear earlier in the design cycle. For example, logic design can not turn a general algorithm into an optimized design where internal bit widths meet a budgeted error or accuracy goal. Instead, global accuracy and error must be traded off. Also, protocols and methods to specify the transference of data both spatially and temporally have a big impact on the algorithm implementation.

DIFFICULT CHALLENGES IN SYSTEMS DESIGN (≥100 nm, THROUGH 2005)

Down to the 100 nm technology node, system design needs the following capabilities and developments:

- The fastest buffered interconnect for a long wire can be over 100× the switching time of an individual gate. Given expected global clock rates approaching 3 GHz, it will be difficult to achieve synchronous, on-chip operation without introducing multi-cycle latencies in the interconnect. System design must comprehend the timing issue more fully.
- The large currents being introduced with increasing power densities and lower voltages all lead to larger supply rail inductive noise. Synchronous systems worsen the problem by scheduling the power switch surges around regular time periods. Thus, supply rail design to reduce effects such as voltage drop or current surges are required early in the design process.
- Estimation techniques will be necessary for supply distribution (such as voltage drop, ground bounce) in light of large current swings (> 500 A) and for clock distribution in light of power surges due to powering up sub-circuits, and power-up / reset condition surges.
- Process technology support for increased switching is not keeping up with the trend in clock rate increase. Thus, design techniques such as reducing the number of logic levels between clocked registers allow the current trend for clock rate increase. Careful consideration of single versus multi-cycle paths and circuits will become more important early in the design process. Specifically, locally synchronous but globally asynchronous design techniques will need to be supported by the tools.
- Floor planning and constraint budget planning will be required especially in light of hard IP blocks and dominance of interconnect over transistor switching time.
- New estimation techniques for interconnect and protocol delays between blocks will need to take into account signal noise (such as coupling), thermal gradients due to power disparities, and other effects. Major interconnect busses and lines will need to be designed early in the floor plan and block partition process.
- Behavioral synthesis has had limited applicability due to poor estimation of the final area or time tradeoff between the various alternatives. This estimation before operator selection and scheduling must be improved to enable this capability. Techniques to aid the estimation are a large selection of pre-defined library (IP) elements and quick synthesis techniques that bypass detailed, final optimization. These same estimation techniques will aid other forms of behavioral synthesis (protocol and datapath synthesis, for example) that in turn aid the system designer in early block partitioning tradeoffs and analysis.
- Embedded software will play a greater role in ASIC and SoC designs, bringing with it the following increased design challenges: hardware/software co-design and design partitioning and tradeoff analysis; software verification and its complexity; hardware/software skills and design team makeup; mixed hardware/software reliability and test; software reuse and software IP.

DIFFICULT CHALLENGES IN SYSTEMS DESIGN (<100 nm, BEYOND 2005)

- An inflection point is reached at around 100 nm design and below. More automated detailed design cannot occur until unbuffered, predictable timing synthesis of small blocks is possible. For 100 nm technology, this implies irregular logic blocks must be no larger than about 100K gates. For an ASIC, this implies that approximately 200 to 400 such blocks must be specified and planned before detailed design can start. This is too much complexity for the system design phase and therefore requires the introduction of a new "middle" layer of design between detailed logic design and system specification/partitioning. Defining the entry into and exit out of this middle layer of the design process will be required.
- Power densities at 100 nm and below are predicted to surpass the ability for all circuits to switch simultaneously. Therefore currents would exceed 1000 A and would be switching within a clock cycle from 0 to 1000 A. Even carefully designed supply rails cannot handle this current without severe impacts on voltage drop and other effects. Techniques to manage the instantaneous power needs and average out the power requirements will need to be put in place. Tools to take this into account during algorithm development will be required to meet optimum performance and power tradeoff points.
- With clock speeds possible exceeding 5 GHz, and across-chip communication taking upwards of 5 to 20 clock cycles, an approach is needed to building a hierarchy of clock speeds with locally synchronous and globally asynchronous interconnect. Tools to handle asynchronous, multi-cycle interconnect as well as locally synchronous, high-performance near-neighbor communication are needed. Abilities to design with two or more clock rates that vary by two orders of magnitude or more within the same block are needed. Communicating asynchronous regions (asynchronously coupled blocks) and multi-cycle interconnect paths will dominate.
- Due to the high cost of "system" communication across the chip, globally accessible register and buffer structures will no longer be possible. Therefore, the cost of communication with various forms of memory will become desperate depending on which block is involved. Design systems that allow for specification and design of distributed memory architectures and the tradeoff with on-chip busses will be required. This makes a major impact on the algorithm tradeoff tool also.
- The prioritization of design tradeoffs must be determined for the new technology beyond 100 nm rules. The biggest impacts of an integrated circuit implementation of such a complex system must be identified and characterized. The impacts can then be built into the tools to allow support in the system design tradeoffs, as early as specification capture if needed. For example, if an algorithm or specification requires random access to twenty 1 Gbit frame buffers, then the cost of implementing a 20 Gbit random access memory must be taken into account early and tradeoffs made to minimize the impact or maximize the specification on a target architecture.
- Multi-tasked, multi-rate systems will be the norm for single chip, encapsulated systems that consume so many transistors. Methods of specifying, verifying, manipulating, and trading-off the various task implementations and their requirements for different response times and data processing rates will be required. Most likely, such multi-tasked systems will need to share resources as seen in multi-media processing of today. Everything from interconnect busses, buffer memory and functional units are shared within complex tasks; each with different data processing requirement rates and response times.
- Additional algebraic or other discrete mathematically based formalisms to cover the various application domains will need to be developed. It is only with more formal specification forms that automated tools can be developed to capture, verify, and then optimize a design. Digital Signal Processing theory, when mapped to the various models of computation such as dynamic data flow, or synchronous data flow, is an example of a new algebra for specifying and manipulating systems in their domain and at a higher abstraction level.
- Even in large electronic systems design today, it is difficult to imagine a completely new design that does not reuse some previous components or capability. Incremental design where less than 25% of the design is new will become more the norm. Tool environments to support such incremental design as opposed to expecting 100% new system specification capture and manipulation need to be developed.

- The ability to insert robustness automatically into the design will become a priority as the systems become too large to test functionally at manufacturing exit. The automatic introduction of techniques such as redundant logic for fault tolerance is needed.

SYNTHESIS AND LOGIC DESIGN

Logic design is the process of mapping the register transfer level (RTL) hardware-specific outputs from the system design phase into a gate-level representation suitable for input to the physical design stage. At this design stage, the RTL represents only digital hardware functionality, which has previously been "scheduled" to specific clock edges. For reasons of design productivity, most technology mapping and logic optimization improvements in logic design require automation within logic synthesis tools and algorithms.

DIFFICULT CHALLENGES IN LOGIC DESIGN (≥100 nm, THROUGH 2005)

As the number of transistors per chip increase, the present-day problem of interconnect delay uncertainties will continue to increase. As a result, greater use of block-based and hierarchical design techniques are required at both architectural and logic levels. The physical location of various blocks to be connected will contain greater variability across-chip. This requires automated interconnect exploration and analysis of many candidate placement choices, coupled with advanced synthesis algorithms. Since all system-level operational constraints must also be satisfied, these constraints will be analyzed concurrently as an integral part of the logic design process. Advanced floorplanning tools must evolve to a larger and more central role, eventually becoming the designer's primary "command and control" center for both logical and physical views of the design.

Even at reduced operating voltages, the predicted growth rate of digital functionality per chip will require substantially more power than supported by known thermal packaging options or anticipated battery life enhancements. As a result, architectural and logic-level power management strategies must be integrated—and automated—within the synthesis environment. However, power estimation algorithms will need some means to handle large design scale capacities and heterogeneous digital/analog/software tradeoffs, prior to the existence of simulation vectors. Long simulation run time for power characterization must be replaced by sophisticated conversion to statistical forms that preserve more relative accuracy for earlier estimation and optimization. The algorithms will need to apply lessons learned from prior synthesis and physical design passes to statistically improve accuracy for re-synthesis in subsequent passes.

Signal integrity and reliability concerns will grow to unmanageable levels if not addressed until placement and routing. New techniques must be developed to support design methodologies that avoid obvious or likely violations as part of the synthesis process. This implies new requirements for concurrent logical and physical design, as synthesis becomes more physics-aware and applies context-sensitive rules to avoid downstream reliability concerns for electromigration, voltage drop, channel hot carrier-induced slew rate degradation, and probable antenna violations. Fundamental signal integrity issues such as crosstalk immunity and noise tolerance must become a tradeoff equal to timing, area, and power.

The increasing integration of many different functions and design styles on silicon, warrants the need for better resolution to differentiate among these styles and apply specialized algorithms suited to optimize for a particular style. However, this need for specialization also requires new algorithms that are capable of recognizing these different styles in the input description and then merging the results. This may include specialized synthesis for datapaths and memories that perform localized silicon compilation, where detailed routing is included for those specific design styles.

Logic design trends indicate increased optimization for power and timing using multiple on-chip voltages and scaled voltage operation. It will be necessary for future synthesis environments to optimally consider, tradeoff, and select not only the best library elements, but also which voltage level is to be applied to satisfy design goals. This implies additional enhancements to library characterization flows.

As new materials and manufacturing processes are adopted, subsequent changes will be required to the synthesis environment. Copper-based interconnects offer faster performance, but if mixed with aluminum at different metal levels could create a major challenge requiring more elaborate integration with detailed

routing to fully resolve. Similarly, low κ dielectrics between layers can improve circuit speeds, but also present a challenge for estimating interconnect performance and critical paths at the logic design stage. Silicon-on-insulator offers yet another process technology enhancement with very similar challenges. The challenges extend beyond library characterization, reaching into detailed optimization heuristics and algorithms.

While most digital logic functionality will continue to be input at the RTL level, the heterogeneous nature of silicon-based applications of 10–50M gates demand that neighboring blocks of analog or RF be explicitly considered. Synthesis will need to adopt special design mapping and/or optimization rules to help ensure the overall integrity of the physically co-located system. Similarly, reused hard IP blocks placed adjacent to new logic could also need special treatment, especially under an assumption that synthesis, placement, and (some) routing algorithms merge.

Present-day concerns over testability will become insurmountable at future logic densities without more automated and thorough test insertion strategies.

While current approaches add test features as an afterthought, future test requirements (as specified during the system design phase) must be satisfied in a more routinely automated fashion. Synthesis algorithms should be developed that are capable of automatically inserting test structures while satisfying all other timing, power, density, reliability, and signal integrity constraints. Test insertion must include self-test logic, and leverage the use of on-chip processors (possibly implemented with supplemental firmware code).

DIFFICULT CHALLENGES IN LOGIC DESIGN (<100 nm / BEYOND 2005)

As silicon manufacturing technology progresses below 100 nm, additional logic design considerations must be addressed. Due to anticipated low voltage transistor operation, extremely tight thresholds and margins, extreme power management problems, and multi-gigaHertz performance requirements, static CMOS may be complemented or replaced with alternative logic families. Logic synthesis must support technology mapping and optimization algorithms for new logic styles required (for example, partial-swing, multi-threshold, or clock-delayed domino cells).

In the sub-100 nm regime, where hundreds of millions of transistors and their interconnect must operate without fail, synthesis tools will be required to automatically integrate fault-tolerant logic design techniques. Fault-tolerant features include hardware redundancy, re-programmable interconnect, and re-configurable control logic. All of these will be expected to operate under the control of on-chip self-test logic.

Heterogeneous system-on-a-chip designs will integrate neighboring analog, mixed-signal, and RF circuits within a single die. Special attention will be required by the digital logic to minimize the likelihood of problematic signal integrity issues. Robust design requirements must be handled on the digital side, yet design productivity needs prevent this from being feasible without automation. These concerns include crosstalk, switching noise, substrate noise, electromagnetic interference, and voltage drop issues. As MEMS, electro-chemical, and electro-biological technologies find their way into silicon, fault tolerance may require additional avoidance techniques.

Given the enormous amount of logic to be generated under such intimidating system and silicon constraints, design reuse and incremental re-design become mandatory. Incremental synthesis that merges both new design features with existing synthesized logic, while preserving most of the existing design realization, will be a grand challenge. Beyond 2005, existing designs that may include custom designed regions should be capable of participating in incremental synthesis and optimization.

Below 100 nm, soft errors are predicted to be frequent enough to severely impact both semiconductor yields and field-level product reliability. Protection from these soft errors may require advanced and dedicated tools to analyze their statistical likelihood by cell, transistor type, and placement, and performed out of cycle as a characterization step. Then automated methods must be discovered for modifying and adjusting the logical and physical design to prevent these errors, without violating any other design constraint within the chip.

VERIFICATION AND ANALYSIS

Verification and analysis continue to be serious bottlenecks for the timely design of complex ICs and SoCs. It is estimated that verification requires over one half of the design resources, human and computer, and slows the "time-to-profit" of new products substantially (Figure 8). Research contributions to this area, therefore, represent the greatest potential improvement in development of new products.

Accuracy of verification relies on accuracy of the model used. Speed of the verification simulation is a function of the simulation application software; the hardware platform on which the simulation is run; and the complexity of the model. Since simulation speed is critical to "time-to-profit," good tradeoffs must be made between simulation speed and accuracy. Methodologies need to be developed that include various levels of simulation accuracy as the design progresses.

Typically designs are modeled at many different levels of abstraction including system, architectural, micro-architectural, register transfer, gate, switch, and layout. For models at the register transfer (RT) level and below, many verification tools and methodologies exist, but they are only marginally adequate—due to reduced device feature size, increased clock speeds of synchronous designs and increased dominance of interconnect over device area—not to mention mixed-signal issues. For efficient core reuse, characterization of a block with respect to functionality, timing, and electrical properties becomes increasingly important. System-level design initiatives and hardware/software co-design initiatives are just beginning to produce commercially usable tools that solve the difficult verification and analysis problem. Embedded cores, system-on-a-chip complexity, integration of digital and analog, and the integration of devices such as sensors or actuators reinforce the analysis and verification challenges. For digital designs, the capabilities for "in circuit" emulation, simulation technologies and formal verification are far from optimum even for today's IC complexities. For mixed-signal (digital and analog) chips, there are some tools for analysis and verification, but much improvement is needed.

SYSTEM LEVEL ARCHITECTURAL VERIFICATION AND ANALYSIS

For designs requiring novel architectures, a top-down design approach is needed with the overall architecture being described by a form of high-level behavioral language. The designer will use this high-level language to exactly describe all the inputs and outputs of the chip and the major blocks within the chip. To do this, the designer must pay close attention to block interface specification. The better the designer does with this level of verification, the smoother the rest of the design will go and the easier subsequent derivative products can be developed with the reusable blocks from the platform design. Better tools are needed for top-level architectural definition that can be used by designers to more quickly and accurately describe complex SoCs by the tools themselves comprehending the language used by various types of systems (networking, telecom, computer, and others). These tools must also interface with the hardware description language (HDL) tools at the next level down to facilitate rapid verification.

Verification at the system architectural level and below requires extensive use of many cooperating abstractions that must be heterogeneous. Currently, the menu of available abstractions is inadequate; methods for defining and manipulating abstract views of a system are almost nonexistent; and the problem of maintaining consistency between several abstract views of the same system, especially as the design evolves, is unsolved.

DIGITAL VERIFICATION TOOLS

Current industrial practice relies mostly on HDL or gate-level simulation with manually generated test cases or pseudo-random inputs, along with timing analyzers and other simple rule checkers. Over the past decade, advances in formal verification techniques have resulted in verification tools that exceed the capabilities of traditional, simulation-based approaches in their ability to detect and diagnose difficult design errors. Much of this work has been based on exploiting regularity in homogeneous design abstractions, such as via symbolic model checking. Advances in equivalence checking by formal verification have greatly reduced verification time at the gate or netlist logic level. Despite these advances, existing formal verification tools do not scale to handle the size and complexity of gigascale systems.

Model checking is currently employed by a number of companies but has not yet become the mainstream methodology. Simulation-based approaches cover a small percentage of the possible inputs, but current model checkers must either be applied to a small fragment of a design or to a highly abstracted description. Theorem proving has mostly been used in research environments. Symbolic simulation is a different formal verification paradigm that has had some success. Symbolic simulation can be used with various symbolic representations, including binary decision diagrams (BDDs) or logical expressions. Symbolic simulation is promising when dealing with designs that are more data-oriented.

HARDWARE/SOFTWARE SYSTEM LEVEL VERIFICATION

The anticipated heterogeneous components of future gigascale systems require specialized, but cooperating, verification methods. Furthermore, new verification methodologies must be embraced to partition the verification challenge into manageable components. Components may include analog, RF, phase-locked loops, and digital fabrics. The new digital fabrics will include many different design styles for a wide variety of applications, such as digital signal processor (DSP), embedded processors, protocol engines, memory subsystems, and video streams. In addition, sensor and actuator components must interact with the real world and verifying their correctness depends on modeling the physical environment.

New models, notations, and verification techniques for continuous behavior systems must be developed, including analog, RF, new interface fabrics, and embedded controllers. Rather than trying to create a single mathematical model and verification technique that covers the complete range of system designs, heterogeneity presents an opportunity to use domain-specific specification and verification techniques. These can leverage what is known about a particular application or design style to increase the effectiveness of verification by orders of magnitude. In some areas, such as analog, RF, and physical-environment modeling, new theories must be devised to apply any systematic reasoning process. For this to happen, new circuit fabrics must be developed with verification in mind. Simply designing heterogeneous fabrics without consideration for how they will be verified will likely result in large systems that cannot properly be verified. Similarly, formalizing and checking components that act as signal converters between subsystems based on different paradigms, such as analog-to-digital signal levels or asynchronous-to-synchronous timing, is not possible without careful construction of the associated fabrics.

Large-scale system verification is best performed by a heterogeneous collection of tools, allowing tradeoffs between the level of assurance, the tool capacity, and the tool performance. These tools should be integrated as much as possible, using compatible representations for system elements, interfaces, and properties to be verified. The electronic design automation (EDA) industry will continue its development of methods to achieve faster evaluation performance via efficient simulation algorithms and hardware emulation. Well-disciplined techniques for analyzing system correctness are needed. This will include a combination of improved and expanded formal verification techniques, as well as "semi-formal" techniques that occupy intermediate points between simulation and formal verification. These multiple techniques need to be integrated into a common verification framework.

As embedded processors become widespread, the correctness of software is part of the overall system verification. To date, formal methods for software verification have not had widespread industry impact due to limitations of existing tools and methodologies. Formal verification research must also focus on the forms of software found in embedded systems, such as schedulers, device drivers, and protocol converters. Such low-level software can be viewed as extensions of hardware and verified by similar means, but using higher levels of abstraction in modeling the storage and manipulation of data. For other forms of software, semi-formal and testing-based approaches that have been developed in the software engineering community must be leveraged. Methods for software verification will become even more important as the ever-decreasing product life cycle creates the need for more and more software re-configurable circuits.

Hardware emulation via massive PC boards with arrays of configurable gates has proven to be a useful form of verification for complex logic systems. The major difficulty with these methods has been the partitioning problem and getting signals that are normally on-chip to move between chips of gate arrays without disrupting the desired timing. Another difficulty is that the fastest emulators are always a generation or so behind the chip being designed and are not fast enough to represent the new design. Emulation is better

suited to pure digital designs such as mixed-signal designs that are not easily verified. Emulators do provide a good means of co-verification of the hardware with the software.

TIMING VERIFICATION

Even for seemingly generic digital components, timing verification faces challenging obstacles. Timing verification is generally performed at the end of the design cycle when the layout has been completed and parasitics can be accurately estimated. Research in timing verification over the last decade has yielded solutions to several long-standing problems, including verification of circuits using multiphase clocking and level-sensitive latching, and the ability to automatically prune away logically unsensitizable, or false, signal paths. However, deep submicron technologies present new problems, such as those due to dominant coupling capacitance, whereby coupling to adjacent wiring can cause delays to vary by as much as 300–400%, depending on the switching state of adjacent wires. This forces functional and timing verification to be done concurrently–at minimum, a quasi-static performance verification. New methodologies for incremental timing verification of digital systems that include dominant interconnect coupling must be developed. Another example of new problems brought about by technology advances is that SOI designs exhibit a "memory" effect due to charge storage in floating wells, such that timing errors arise due to threshold voltage changes. These effects in this case are highly pattern dependent and activity dependent, causing inaccuracies when using static timing verification.

Of further concern for deep submicron are the variations in performance due to manufacturing fluctuations. Statistical verification methodologies that will serve as enabling technologies for reliable design and test must therefore be developed. These methodologies will be incremental in enabling new synthesis and physical design capabilities and must also support abstractions across all levels of design. Therefore, semantic information such as the distinction between data and control signals, or between an opcode, an address, or an operating mode, must be exploited to manage timing verification complexity without compromising its accuracy.

POWER ANALYSIS

Better methods of accurate power prediction and analysis are more important than ever. Power prediction must be done as early and as accurately as possible in the design cycle, if possible at the architectural design phase. More and more applications have power budgets that cannot be exceeded for one reason or another, usually portability or reliability for a given package or system. Inaccurate power estimates often result in rework of the design architecture, logic, timing or sometimes costly rework of an analog block and results in delays in the design.

TESTABILITY ANALYSIS

Testability must be designed in at the earliest possible time. Testability planning must be done during the architectural design phase and any special testability cells inserted in the design early so that the effects on timing as well as test coverage may be analyzed and assessed. The objective is to have high fault coverage with minimal adverse affects on circuit performance, area, or power. Methodologies must ensure that simulations and analysis done earlier in the design do not have to be redone after test insertion.

NOISE ANALYSIS

One of the biggest problems in design of today's high-performance logic or mixed-signal chips is that of noise analysis and minimization. This is due largely to the complexity of the noise problem that includes parasitic capacitance and inductance of both on-chip and package interconnects, interconnect crosstalk, and noise injection via the substrate. Tools are needed that will quickly and accurately tell the designer when the signal-to-noise limits are exceeded in the digital and the analog domain.

ANALOG CIRCUIT VERIFICATION

Some analog circuits such as an RF amplifier may have as few as three or four transistors, however the verification of such circuits over voltage and temperature may require tremendous simulation times due to precise modeling of all the passive elements, including parasitic elements. As more complexity is added, verification of large analog blocks can take many weeks of simulation time. Ever-faster simulators are the

historical solution. New solutions need to include statistical techniques to eliminate many voltage-temperature simulations as well as better compact models that allow faster simulations without sacrificing accuracy.

PHYSICAL DESIGN VERIFICATION

The physical design verification phase is also a critical step in timing verification as it is only during this phase that exact timing information can be extracted. As we move into deep sub-micron (DSM) designs, verification of the physical designs will take longer due to the added complexity of the interconnect parasitics to include R, C, and now L. Currently only a moderate contributor to design cycle time, the verification of the physical design can involve significant resources and is not always a smooth process. Designers often use CAD tools from multiple sources during this phase because one suppliers's tool may do a much better job than another. These different tools do not have standard interfaces to each other, which causes many extra days of program delay. Standard interfaces must be developed to enable tools from different suppliers to communicate smoothly.

DESIGN FOR VERIFICATION

Over the next decade one of the key promises of component-oriented design is its potential to leverage formal verification methods. Disciplined, component-oriented design requires partitioning the system into subsystems of manageable complexity communicating through well-defined and fully characterized interfaces. Verification can exploit this modularity, verifying the interfaces, components, and overall system at appropriate levels of abstraction. To realize this potential, new formal and semi-formal verification techniques must be developed and integrated.

Parameterized modules, where details such as word size, capacities, and detailed functionality can be determined during instantiation will be very important in component-based designs. Methods for verifying the correctness of a parameterized module before instantiation will be highly advantageous, because verification will only need to be done once by the designer, rather than by each customer who instantiates the module. Verification of parameterized components can be done by abstractions that reduce a module of size n to a fixed-size verification problem; by special decision procedures; or by the use of induction in a general-purpose theorem prover. Research results have been published on such techniques, but current capabilities are limited and require great effort and expertise on the part of the user.

Verification of gigascale systems must exploit many levels of hierarchy and abstraction. It is widely recognized that abstraction is the key to verifying large systems, but most uses of abstraction in current verification methods are ad hoc and extremely labor intensive. In applying existing formal verification techniques, the most time-consuming activity and the one requiring the greatest expertise is the construction of abstractions and simplifications that are coarse enough to be checkable yet fine enough to reveal useful information and be logically correct. Methods must be devised to generate suitable abstractions in a more automated way. Generating these abstractions will be greatly aided by use of a more systematic, top-down design methodology. Verification can be coupled into the layered abstractions used during the system design process.

INTEGRATED VERIFICATION ENVIRONMENT

The current practice in industry is to use a diverse collection of verification tools including multiple forms of simulators, timing analyzers, and others. Significant effort is expended translating between incompatible circuit formats and setting up environments that will automatically invoke appropriate tools as a design evolves. Efforts to develop industry standards for tool integration have had limited success. As we add in new forms of tools, including ones that comprehensively analyze different facets of a design and that view the system at different levels of abstraction, tool integration becomes more critical and challenging. In addition to compatible formats, we need methods to ensure consistency of the different representations as well as to evaluate the completeness of the overall verification methodology.

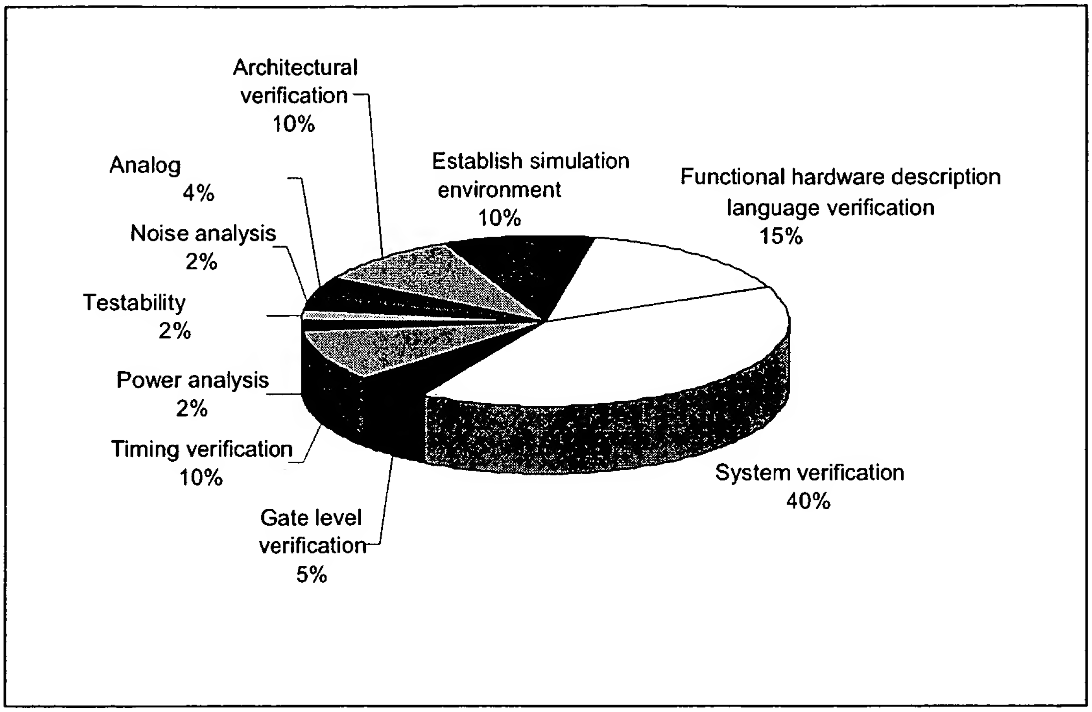


Figure 8 Allocation of the >50% of Design Effort Devoted to Verification

SUMMARY: ISSUES AND NEEDS

The semiconductor industry needs mathematically precise models of system and architectures, automated analysis tools that handle the complexity now routine on a single chip, and automated verification tools that can guarantee compliance of a model with a lower level model of the same design. Increasing complexity demands more automation of the design process. New ideas and more automated tools in formal verification, simulation, emulation, and hybrid approaches are needed now to handle the synthesis, analysis and verification problem.

PHYSICAL DESIGN

Physical design deals with aspects of the chip implementation related to the spatial embedding of devices and interconnects. With advancing technology, it is harder to estimate and abstract the effects of physics and embedding on achievable design quality, where quality is measured by the key objectives: timing, power, signal integrity, reliability, and manufacturability. Thus, physical design will continue to become more closely linked with system-level design and logic-level design. In addition, physical design requires a new manufacturing interface that enables close ties to circuit implementation and the underlying process technology. The surrounding design methodology, as depicted in Figure 6, must support tight coupling of

1. (incremental) modeling, analysis and abstraction of the key objectives with appropriate accuracy,
2. (incremental) design synthesis and optimization of these abstracted objectives, and
3. (incremental) (re-)specification of the design at multiple levels of representation.

These needs apply equally to the design of digital, mixed-signal, and analog systems.

DIFFICULT CHALLENGES BEFORE 2005

Silicon Complexity—Increasing silicon complexity creates challenges in power management, signal integrity, and layout complexity. New tools will be required for power and current management. This will include both

design tools for power delivery as well as analysis tools for IR drop and active power dissipation. Additionally, power density issues will need continuous attention to keep silicon within its operating temperature window. Finally, power dissipation need higher priority while resolving the different cost functions involved at all major junctures in the design flow.

Efforts to ensure acceptable signal integrity will need to address noise as well as coupling effects. Interconnects and their dynamic physical interactions become a major source of uncertainty in achieving signal integrity closure. Tools must comprehend and manage these interactions without compromising the quality of the embedding, such as routability.

Balancing the different cost functions while converging to an acceptable layout solution is another key challenge. Since physical design will increasingly entail large-scale interacting multi-level, multi-objective global optimizations, new paradigms for optimization must be developed, such as constraint-dominated global optimization, incremental optimization, resource-bounded optimization, and optimization with partial or probabilistic design information.

System complexity—Increasing system complexity will have its unique set of challenges for physical design due to diverse design styles and the industry trend towards system level integration. This will lend itself to layout tools comprehending critical signal isolation, IP block placement, and interconnect considerations allowing the handling of mixed design styles and types (analog, digital, mixed, RF). Distinctions between high-frequency digital design and analog/mixed-signal design will blur. Controllability and observability will need to be understood at layout as testing and verification responsibilities are dispersed into the physical design flow.

Design procedure complexity—Design procedure complexity challenges with IP block insertion and reuse will affect productivity unless addressed. This will require new tools for reuse-driven block characterization and abstraction, design data management, and flexible functional/physical hierarchy management. Process technology mapping to aid reuse across process generations will become necessary to maintain productivity improvement.

Increasing clock frequencies and large switching currents imply a need for tools that unify the synthesis of power, clock and test distribution, along with reliability- and noise-driven layout. As reflected in the new design system architecture of Figure 6, data models, repositories and interfaces must be re-engineered for "unifications" such as concurrent logical-physical design, or tight analysis-synthesis loops. Manufacturing variability implies a need for statistical design and design centering tools, such as timing analysis and physical verification tools that comprehend parasitics, delays and geometries that are parameterized by distributions.

Manufacturing variability (and the proliferation of new materials and processes) also requires a new design-manufacturing interface that supplies design rules and other process abstractions to layout. Key drivers include planarized multilayer interconnect processes and subwavelength optical lithography, both of which affect physical verification and the nature of appropriate handoffs to manufacturing. Physical design may also drive future process development.

Verification complexity—Verification complexity increases as system level integration pervades integrated circuits. Additionally, as feature sizes shrink and frequencies increase, the dominant parasitics take on new forms.

One of the challenges that needs addressing is functional and performance verification for both the IP block and it interface connections. Tools must verify both functionality and timing of the individual blocks and their sum across different design styles and design types.

Timing verification must comprehend the physical models and dominant parasitics for both device and interconnect at these small feature sizes and high frequencies. Dynamic timing verification will replace current static timing tools. Additionally, modeling will need to comprehend minimal guard banding to allow a solution space to exist.

Testing complexity—As design and manufacturing processes evolve to address challenges of DSM, economics will drive test considerations into all aspects of the design process. Circuit implementations will move away from standard static CMOS and include dynamic logic, asynchronous circuits and will include mixed analog and RF elements. These process and circuit complexity drivers will impact test by increasing effects of noise, crosstalk, and soft error. To address these challenges, increased reliance on Defect Based Testing will require that physical design tools extract fault locations for new types of defects. The drive to rapid production ramps will require that tools be developed to support rapid diagnosis of failures on this wide variety of circuit types.

DIFFICULT CHALLENGES BEYOND 2005

Silicon complexity—Silicon complexity will become compounded with the inclusion of new novel devices to comprehend in the layout activity. Extraction tools will need to identify and model both active (RF/mixed/digital) and passive (inductors) devices. Analysis tools will need to comprehend the operation of these devices as well as on-chip process variation effects.

System complexity—System complexity will increase with the integration of new technologies (such as MEMS, electro-optical). Tools will need to recognize the special requirements of these technologies during the physical planning and layout activity.

Design procedure complexity—Given the increase of novel devices and technologies, a true incremental one-pass design process, as shown in Figure 6, becomes essential to fully explore the solution space of the design.

Verification complexity—Complexity will increase due to introduction of more novel devices and structures, issues that were mentioned prior to 2005 are still applicable.

Test complexity—Layout tools will need to support BIST and built-off-chip-self-test (BOST) activities as traditional post silicon testing methodologies become prohibitive in terms of cost and complexity. These tools will recognize and add supporting circuitry automatically.

PHYSICAL DESIGN POTENTIAL SOLUTIONS

Given these critical challenges, the roadmap of physical design needs includes the integration of the many disparate activities currently found in the design flow. Analyses and syntheses must be unified to erase barriers between today's disparate flow stages to close the analysis-synthesis loop. Constraints will drive synthesis, and estimated parasitics drive analysis, in a "construct by correction" iterative improvement process. An "analysis backplane" will support semantically consistent design views and performance analyses across multiple implementation phases. Such analyses must be increasingly informed by the functional intent of the upstream syntheses, in order to achieve performance convergence.

Layout-level and system-level design must be unified. Modeling capabilities (for both design instances and tool behaviors) must be developed to enable forward estimation-driven syntheses and design exploration. In addition to new support for hierarchy and reuse, the spanning of multiple implementation levels implies greater need for auto-interactive use models and iterative design. Design productivity requirements may also require more "structured" design methodologies and circuit fabrics, such as to simplify verification of crosstalk noise or clock skew at the expense of performance or area.

Technology mapping can be integrated with layout synthesis while timing optimization, clock synthesis and test synthesis can be integrated with placement. Such coexistence of system timing management, logic optimization, placement and routing in a single environment should mature within the next process generation.

SUMMARY AND PRIORITIZATION

While the above elements of context and need are all critical, issues that absolutely must be solved in the near term in priority order include

1. design system reengineering to enable unification of analyses-syntheses and layout/logic-level design,
2. an incremental optimization design flow that will provide substantial productivity over the current cyclic flow now in use, and
3. power management. These lower priority ordered items need an existing infrastructure consisting of the higher prioritized items in place to be useful.

TEST METHODOLOGY

THE NEED FOR DESIGN FOR TESTABILITY

In the past, it has been common to view design-for-testability as a design option, something that could be included or not, depending on various economic parameters. Implicit in this view is the assumption that circuit designers would be able to write extensive tests of chip functionality and that automated test equipment (ATE) would be able to apply these complex functional tests in a manner that matched expected chip operation and to accurately distinguish chips that would work from those that would not. It is now apparent that each of these implicit assumptions will fail, either now or in the very near future, and that major changes are underway in test methodology and application.

The cost of designer-developed functional test vectors is increasing exponentially for successive chip generations. It is no longer feasible to commit huge manpower resources to functional test development, even for very high volume products. In addition, as designs become more complex, it becomes increasingly difficult to translate test input and output data from a block boundary, with which a designer is familiar, to the chip boundary, where the ATE interface exists. It is also difficult to extract synchronized, deterministic, chip-level data from a system simulation environment, especially when inherently asynchronous and/or nondeterministic signals such as interrupts and bus transactions are involved.

Even if functional vectors were available, ATE performance is not improving at the same rate as chip performance. Tester overall timing accuracy (OTA) makes up an increasing portion of minimum device period, and is expected to exceed device period within seven years. This means that ATE will not be able to accurately identify failing parts for at-speed functional tests, resulting in either substantial yield loss or inadequate shipped quality. Furthermore, the ATE environment is different from the system environment, usually featuring substantially higher loads per pin. Finally, high-performance ATE is very expensive. Developing the circuitry needed to precisely deliver and measure signals and power in a noise and temperature controlled environment at the speeds predicted by the roadmap is a daunting task. It is therefore likely that functional test cost per manufactured transistor will not change substantially, even as transistor manufacturing cost drops.

As functional test becomes increasingly nonviable, alternatives must be developed. All of these will involve adding test functionality to the design, whether this takes traditional forms such as scan design, and/ or more innovative approaches. If off-chip methods are no longer able to evaluate chip performance, or test data for deeply embedded blocks cannot be brought to the chip boundary, then alternative on-chip methods (built-in self-test) must be developed. These changes are expanded upon in the next section

ANTICIPATED REQUIREMENTS IN TEST METHODOLOGY

Test continues to be a major expense in the IC development and manufacturing chain, with up to 35% of nonrecurring engineering (NRE) costs attributed to test development and debug, and with ATE cost per transistor expected to remain flat. Changing processes and design methods are pushing testability beyond economic limits. Rapid improvements must be made to improve overall testability and test economics.

- *Built-in-self-test* will be needed as chip performance begins to outpace tester timing accuracy, and as overall test data volume exceeds ATE and chip boundary capability. BIST needs to be made usable in short-design cycle environments by novice designers. Logic BIST methods must be developed that provide

high coverage for all fault types required. Power management and test sequencing must be addressed by BIST tools. The concept of BIST needs to be extended to include additional on-chip parametric measurements currently performed by ATE.

- *Divide-and-conquer* techniques such as scan wrappers around hierarchical blocks and localized BIST will be needed to manage test complexity, as the task of developing adequate tests will become impossible for flat designs.
- *Reuse of cores* requires the encapsulation and reuse of test as well. Standardized interfacing and access methods for core testing are needed, as are composition methods to assemble complete chip tests for chips with multiple cores, including analog cores. Methods to test the interconnect between cores must also be developed, and signal integrity standards developed to assure that cores, when embedded, function as expected within the larger chip, even in the presence of noisy power, grounding, and interconnect. In addition, standardized test data formats, such as standard test interface language (STIL), will be needed to ensure portability.
- *New fault types* must be identified, and test methods developed for them, as net timing and signal integrity problems increase dramatically and introduce new modes of chip failure.
- *Design for testability* must be tightly integrated into all steps of the overall design flow, including synthesis, validation, and physical design, and include automatic test generation with high coverage for all relevant fault types (such as stuck-at faults, timing, bridging, signal integrity). These DFT techniques must apply to complex chips with multiple timing domains, and must include methods to simplify probing requirements at wafer test.
- *Signal integrity* and electromagnetic (EM) phenomena will become an increasingly important test issue as chips and test equipment become complex. New fault models (including soft error models) that incorporate the effects of EM fields must be developed. Relationships between design constraints and manufacturability and testability must be developed for different design domains. Test generators must be sensitive to signal integrity issues.
- *Timing tests* are impacted by interconnect delays, slow synthesis system drivers, increased frequencies, multiple timing domains and clock skew. Automatic test generation will be necessary to accommodate the large number of near-critical paths, and BIST systems will have to guarantee high coverage of timing faults.
- *Quiescent current (IDDQ) testing* requires extensions for manufacturing test as background currents increase, although it will remain a valuable technique for failure analysis. Single threshold IDDQ testing is no longer viable for many CMOS processes, and other approaches will be needed to ensure device reliability.
- *Hardware/software co-design* will provide opportunities for system software to be used as an aid for test. All high-level design methodologies must be sensitive to the fact that they may target unknown libraries and processes with special test problems and unknown fault statistics.
- *Analog/RF systems* present continuing challenges for test, primarily because they require test to specifications rather than structural test. As a result, there is inherent difficulty in presenting any simplification to create a meaningful fault model. Embedded analog blocks will likely require the development of BIST approaches.
- *Yield improvement and failure analysis* tools and methods will be needed to provide for rapid yield learning with very complex chips containing embedded cores (on the actual chips, not simplified test devices), and for highly automated failure analysis where faults can no longer be visually detected. Design and synthesis for diagnosis must be included if short failure analysis and yield improvement cycles are to be realized.

Other issues include the insertion of testability circuitry in systems limiting the operating speed of the system. Figure 9 shows the increase in test time relative to ITRS pincount projection. Power consumption during test must be carefully considered so test programs do not put the system into modes that consume excessive power. Application of test programs must also not cause excessive noise with the possibility of soft errors.

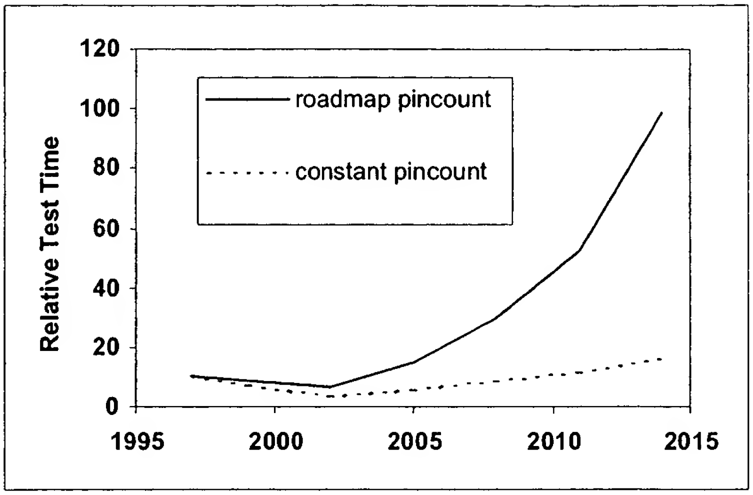


Figure 9 Increase in Relative Test Time

DESIGN TECHNIQUES AND METHODOLOGIES

IC design over the next decade will be dominated by wireless and wired telecom (broadband) as well as signal processing and advanced computing. A looming problem, however, is that IC design complexity increases superexponentially with the expansion of chip function and performance as evidenced by both larger scale digital systems and SoC. On the other hand, design complexity is also growing as the design space becomes more difficult with the onset of physical and technological barriers.

The traditional rules of IC architecture design are being severely strained by these trends, mandating new approaches in the decade ahead. Some of the most widely-held rules include: (1) system-wide synchronicity, (2) use of a switching device—the CMOS transistor—that has no prescribed intrinsic size (that is, it must be scaled for faster performance, and such scaling introduces a statistical variability in transistor behavior), and (3) the capability to fabricate chips with 100% working transistors and interconnects.

DESIGN TECHNIQUES

Design techniques pertain to the implementation of the steps that comprise a methodology. These address the circuit building blocks (or, primitives) themselves, and these are coupled to the technology infrastructure as well as the end product. Emerging concerns are power management, circuit noise, signal delay and integrity in the interconnect, clock generation and distribution, methods to increase frequency operation of circuit blocks, and faster logic families.

High-performance Digital Logic

Microprocessors, DSPs, and core-based designs (ASIC, SoC) will be the major drivers for high-performance digital logic. Digital logic must evolve to satisfy two disparate demands, as follows:

1. *The MOS transistor is becoming less ideal* as it approaches the practical scaling limit, expected to occur soon after the 70 nm technology node. Deep submicron CMOS circuits need special configurations to accommodate, among others, higher gate and drain leakage currents, the limits of constant-field MOS transistor scaling, higher source/drain resistances, shrinking V_t and V_{dd}, and poor scaling of parasitics.
2. *New alternatives to static CMOS required for high-performance designs*—The need for high speed logic now means that "high-performance logic" may be defined to be "not static CMOS." The lower voltage swing and precharged nodes of some logic breeds facilitate the quest for more speed, though at a higher power, more susceptibility to noise, and a substantial increase in the difficulty of design. For some applications, these may be acceptable tradeoffs. Dynamic logic may find limited use, given the need for

performance, but its design difficulty and susceptibility to noise may limit its usage. New research into fast logic implementations must proceed.

Interconnects

Future design issues with interconnect are: (1) the *interconnect performance bottleneck*, relating to the growing signal transmission delay of global signals relative to the clock rate and gate delay; (2) *signal integrity* concerns stemming from increasing crosstalk and electromagnetic interference, including noise from line termination mismatches; (3) *electro-migration*, which imposes severe restrictions on signal and bus line scaling; (4) need for *CAD capabilities* that address interconnect design early in the design flow to provide maximum degrees of freedom downstream for performance optimization; and (5) *power distribution networks* that produce equipotential planes across the chip.

A key distinction exists between local and global interconnect. Typical wire length distributions for microprocessor architectures, for example, show that well over 90% of wiring instances have lengths that span the physical area of less than 40 logic gates. Estimates of local wiring delay show it to be scaling as rapidly as gate delay scales, and it can be up to 10× smaller than overall gate delay. However, the situation for *global signaling* is quite different. Chip size is increasing, implying an increase in global wire lengths. Clock rates are increasing. The ratio of global wire delay to gate delay is going up rapidly, meaning that wire delay will dominate, and its delay can exceed a clock cycle. In summary, in signal space, the "interconnect problem" refers to the wire delay of global signals.

Technology advances in interconnect—particularly copper and low permittivity dielectrics—have helped postpone the onset of serious global signaling problems for one or two technology generations. By early 1999, copper was nearing production, and low κ dielectrics were regarded to be mid-term research. Optical transmission of global signals may be the next available global interconnect scheme. It seems more probable that industry will exhaust design solutions to solve the interconnect bottleneck before moving on to costly methods. Advances in the following capabilities must occur:

- Interconnect-aware CAD tools to consider wiring constraints early in the overall design cycle, thereby providing maximum degrees of design freedom. This implies both physical and logical design views are considered in parallel from the highest abstraction levels, and integrated into EDA tools.
- Optimal usage of repeaters to facilitate shorter global signal transmission delays
- Technology maturation of low κ dielectrics for use in production alongside the improvements over copper metal systems
- Refinement of on-chip wiring hierarchies that use combinations of available metal systems (Al, Cu, SiO_2, low κ, and others) and a formalized *interconnect architecture optimization* method to determine the number and functions of wiring levels
- New circuits and systems architectures that avoid the longer global wires
- Novel transmission line designs that minimize crosstalk, skews, reflections. This will likely involve the use of ground planes.
- Innovative system architectures to maximize local communications and minimize global signaling.
- Better packaging schemes that reduce parasitics. This includes new concepts such as chip-on-board. Power and global signal wiring may be handled in the package. This assumes that efficient chip-to-package signaling and fast trans-package signaling can be done.
- Synchronous and quasi-synchronous architectures.
- Innovative clocking schemes that utilize encoding, extraction, multi-state, and local-phase optimization to compensate for skew and latency concerns.

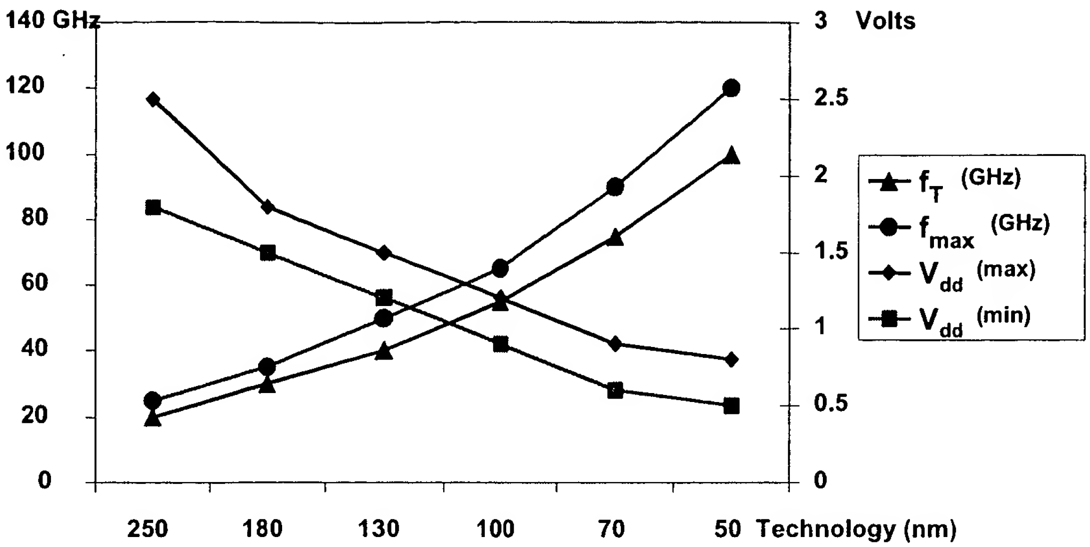


Figure 10 Analog MOS f_T and f_{max} with V_{dd} versus Technology Node

With the need for higher performance SoCs, technology scaling does aid in achieving this performance, since device fT increases; *however*, scaling of power supply voltage (shown in Figure 10) does not favor analog circuits. To gain continued performance increases, innovations in the design are required at both the architectural and the circuit-level. Without new design techniques, the incremental improvements in performance will decrease as the integrated circuit processes continue to scale (Figure 11).

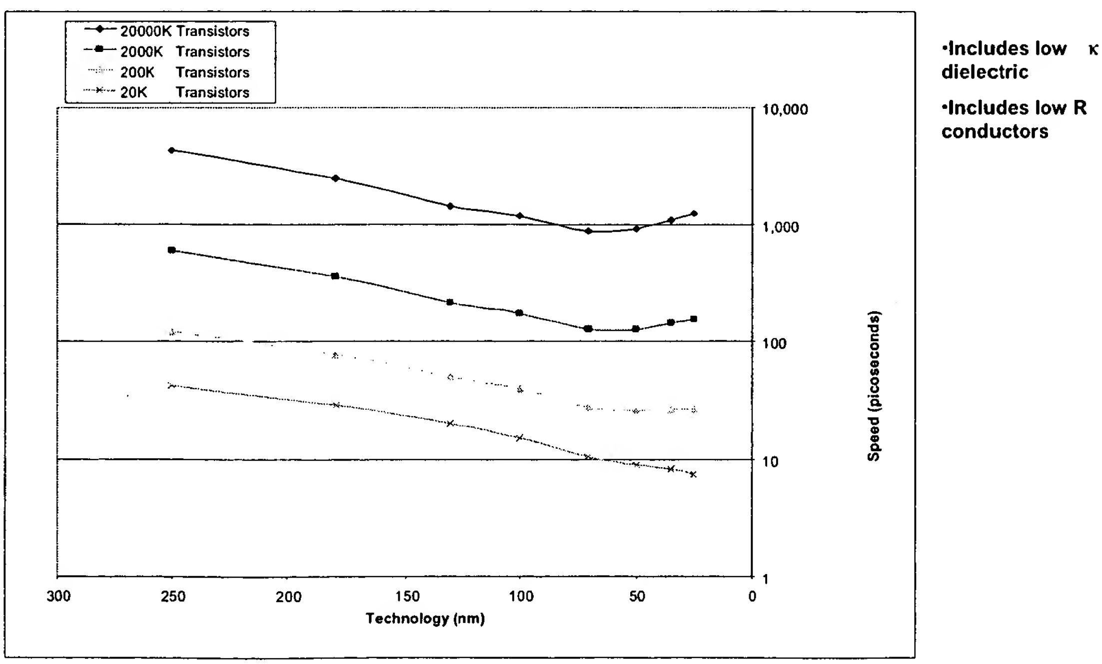


Figure 11 Minimum Half Perimeter Delay for Various Size Cores

Clocking and Global Signal Transmission

By 2014, global clock rates are predicted to rise to approximately 3.5 GHz with local clock rates exceeding 10 GHz. Rising and falling edges usually occupy about 25% of the clock pulse width. Given that it takes five or more harmonics to correctly represent a rising/falling edge, the signal frequency content on the interconnect could approach 25 GHz. Moreover, there is the issue of timing skew, a quantity that designers need to control in design. By the 50 nm node, timing skew budgets will likely drop below 40 ps. Superimposed on these performance targets is the need for noise immunity, vis-à-vis, signal integrity. Also, there is the overall issue of delay that is embodied in the previous discussion of interconnect.

There is a need for better methods for clock design and for systems that do not require system wide synchronicity. Clocks of high-performance systems will be locally synchronous. The interfaces between locks will be quasi-synchronous meaning the phase may need to be realigned. The clock frequency in these blocks may be a much higher frequencies than the interfaces.

DESIGN METHODOLOGY

Design methodology is the shared enterprise of the design and CAD communities. It is defined as the sequence of steps that creates a system. This sequence guides the design flow to produce a design as close as possible to the design target within the feasible design space. Conceptually, this emerges by combining top-down and bottom-up constraint propagation. The top-down path implies planning and enforcement of system specifications. Conversely, the bottom-up path asserts the underlying device infrastructure and its associated physics and technology limits. This dual top-down/bottom-up method has pervaded design all along in an *ad hoc* manner; however, in the VLSI era, the number and difficulty of the constraints require a deeper knowledge of the constraints in higher level CAD tools. Corollary to the top-down/bottom-up method is identification and solution of problems as high in the design hierarchy as possible. This provides the maximum opportunity to find a workable design space.

Future design methodologies and associated CAD tools have their origins in several emerging trends, such as:

Expansion of top-down and bottom-up design methodologies and architectures across disciplines to facilitate SoC design. In addition, such capabilities must include software, RF, and analog into traditional digital flows. There are needs for extensions beyond the electrical realm to interface to the human and physical world. These interfaces might include such domains as user interface, electromechanical, sensors, and photonics. Also, comprehensive simulation systems for design at multiple levels of hierarchy in this expanded set of domains are needed.

Intellectual property (IP) (Core based design and reuse)—The design community must have available a framework that permits encapsulated IP to be readily incorporated and used. To that end, standard core interfaces should become as pervasive as 7400-series TTL. Block-level "handshaking" protocols must be established, as an example, for timing, and signal levels.

High-level estimation—Many low-level problems can be solved at the system level if they are known and representable. Thus, an emerging design methodology is to accommodate low-level needs by using high-level estimations of low-level physical and technological quantities relating to interconnect and transistor/gate performance. Estimations at this level require only relative accuracy, sufficient to choose from among a discrete number of architectural options.

Correct-by-construction design—Verification is costly. It is better to minimize iteration between various levels in the design hierarchy. The goal is to move to correct-by-construction design at the behavioral level including electrical characteristics. Functions previously in verification will be included in synthesis.

Robust, fully-integrated device modeling and simulation—As design margins shrink, the task of assuring first-pass silicon is becoming very difficult. Adding to this is the problem of many design styles and devices, such as those in SoC designs. Thus, fully integrated and robust systems must exist to provide models and simulation capabilities for analog/mixed-signal and high-performance digital logic. These include:

- Sensitivity analyses to ascertain the criticality of model parameters
- Extensible compact models with variable model complexity
- Comprehensive circuit simulation/analysis capabilities for noise (phase, jitter, linearity), frequency-dependent behaviors
- Models for deep submicron devices, interconnects, parasitics, substrate effects, noise, thermal variations (self-heating), and distributed effects for RF regime

Signal integrity—Design methods must materialize to preserve signal integrity through synthesis. Signal integrity considerations must include crosstalk, reflections, EMI, and substrate coupling.

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

1999 EDITION

TEST AND TEST EQUIPMENT

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TEST AND TEST EQUIPMENT

SCOPE

The Test Roadmap focus has been expanded in 1999. The number of tables for test equipment will be expanded from two to nine and will address memory needs for the first time. The test challenge is growing with the ever-increasing device frequency, power, and pincount while trying to reduce cost.

The 1994 and 1997 Roadmaps presented built-in-self-test (BIST) and design-for-testability (DFT) as potential solutions for achieving simpler and affordable test equipment. Unfortunately, no predictions were made as to when DFT/BIST accompanied by low-cost automatic test equipment (ATE) would be widely accepted. The progress toward lower-cost testers has been slow, but the increased use of BIST and DFT IC designs will cause a change in test equipment requirements and reduced cost in the near future. Table 15 showing the difficult testing challenges highlights these issues, together with other challenges that are making test difficult, especially with the introduction of systems-on-a-chip (SoCs). Fundamental physics problems, timing inaccuracies, noise, along with escalating cost demand a change in test methods.

The 1999 ITRS *Test* chapter also contains a new section listing the requirements for developing ATE specifically designed to test ICs with DFT and BIST. Although an IC with DFT and BIST may have one or two thousand pins, only a small number of I/O signal pins are required in the ATE (perhaps < 64). On the other hand, provision must be made to ensure that all the remaining pins will toggle properly. ATE designed for testing DFT/BIST ICs could reduce equipment cost by a factor of ten, and thereby avoid the cost of traditional high-frequency, high-pincount ATE from approaching $20M, as predicted in previous roadmaps.

The trend of more system functionality on a single piece of silicon (SoC) will increasingly blur the lines between traditional digital, analog, RF/microwave and mixed-signal devices. This trend will drive test equipment toward a single platform solution that can test whatever happens to find its way onto a single piece of silicon. The digital requirements for mixed-signal test equipment are the same as for purely digital chips and are shown in the Microprocessor and ASIC tables. The trend in test equipment is toward a modular high-speed and high-pincount digital test platform where high-performance analog/RF/microwave instruments can be added as needed. The analog test issues and test technology limiters are higher bandwidth, higher direct conversion sampling rates, higher dynamic range, lower noise floors, and seamless integration of the digital and analog instruments and cost.

Memory testing, previously excluded in the 1994 and 1997 SIA roadmaps, has been included for both commodity and embedded DRAMs, and for commodity and embedded FLASH memories. In the future, SoC memory testing will be challenging if external chip access is not readily available. BIST and built-in self-repair for memories will be essential.

High-frequency, serial communications devices are rapidly becoming important. Testing devices for applications such as SONET, Fibre Channel and Firewire require test systems that have a small number of pins capable of generating and receiving differential signals up to 10 GHz with voltage swings as low as 100 mV. Differential device-under-test (DUT) input signals must have timing skews as low as 10 ps. At the present time this kind of testing can only be done using expensive specialty instruments and not by general purpose ATE. It is almost impossible to predict how this fast moving field will develop through the roadmap period to the year 2014.

The ultimate dream of test engineers is wafer-level testing and burn-in. Handling singulated chips in a test and burn-in operation will always be cost prohibitive as compared to achieving the quality and reliability specifications at the wafer level. This leads to the concept of known good die (KGD). KGD is being actively pursued by IC manufacturers and will require the development of new infrastructure to support new test and reliability methods as well as new shipping and handling media (waffle-pak, gel-pak, tape and reel, and

others). The development of wafer-level burn-in techniques is also an important requirement to support KGD.

DIFFICULT CHALLENGES

Table 15 lists the five most difficult challenges through and beyond the year 2005. Perhaps the most difficult challenge will be to develop low-cost ATE for testing ICs with DFT when analog circuits and high-speed serial communications buffers are present. Another problem with this kind of ATE will be the need to test thousands of pins with "reduced-function" pin electronics when testing several DUTs in parallel. The section on testing devices with DFT tends to sidestep these issues.

The topic of IDDQ testing has been omitted from the difficult challenges table, even though it appeared in the 1997 table. When ICs contain tens of millions of transistors, leakage currents will mask currents generated by faults. This does not necessarily render the technique useless, but different approaches are required. A special section has been included on this topic later in this chapter.

Table 15 Test and Test Equipment Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥ 100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
BIST and DFT	Test equipment costs will rise toward $20M and wafer yields may suffer without DFT and BIST. DFT required for at-speed test with a low-speed tester. Tools required for inserting DFT and BIST and estimating cost. Analog BIST needed. Access to SoC cores needed when using DFT and BIST.
DUT to ATE interface	A major roadblock will be the need for high-frequency, high pin-count probes and test sockets; research and development is urgently required to lower inductance and cost. Increasing pincounts lead to larger test heads and longer I/O round-trip delays (RTD). This problem can be avoided using two transmission lines, but I/O pins must then drive 25 ohms. Power and thermal management problems Nonuniform wafer temperatures and the requirement for active DUT temperature control Simulation needed for the path from the device through the package to the ATE pin electronics Interface circuits must not degrade ATE accuracy or introduce noise. Especially for high-frequency differential DUT I/O Faster, multi-socket, automatic package handlers are required.
Mixed-signal instruments	IC manufactures must partner with the ATE suppliers to ensure ATE capability will match the mixed-signal requirements These will require more bandwidth, higher sample rates, and lower noise. Testing chips containing RF and audio circuits will be a major challenge if they also contain large numbers of noisy digital circuits.
Failure analysis	3D CAD and FA systems for isolation of defects in multi-layer metal processes New fault models, such as for crosstalk. Automatic test generators for fault diagnosis. CAD software for fault diagnosis using new fault models to support DFT and BIST requirements.
Test development.	Automatic test program generators to reduce test development time Test standards, such as STIL , IEEE P1500 Reuse of core tests for SoC to reduce test development time Simulation of the ATE, interface, and DUT to avoid test development on expensive ATE. (virtual testing) Data management needs to be integrated into test program development

Table 15 Test and Test Equipment Difficult Challenges (continued)

FIVE DIFFICULT CHALLENGES < 100 nm / BEYOND 2005	
DUT to ATE interface	Optical probing techniques Full wafer test Power and thermal management problems, especially with 300 mm wafers and increasing parallel test sites Contactless probing using BIST (see DFT/BIST section)
SoC test methods	New DFT techniques (SCAN and BIST have been the mainstay for over 20 years). New test methods for control and observation are needed. Tests will need to be developed utilizing the design hierarchy. Analog BIST Logic BIST for new fault models and failure analysis Deterministic self-test instead of pseudo random test patterns EDA tools for DFT selection considering cost/performance issues
MEMS, sensors, and new IC technologies	Develop new test methods.
New burn-in techniques.	Research is required. Test during burn-in using burn-in DFT/BIST capability; low-cost, massive parallel test during burn-in
Failure analysis.	Realtime analysis of defects in multi-layer metal processes New fault models, such as noise New CAD tools for diagnosis Failure analysis for analog devices

FA—failure analysis
SCAN—A test method in which test patterns are scanned in and out of the DUT.
STIL—IEEE Standard Test Interface Language

TECHNOLOGY REQUIREMENTS

The basic capabilities of the automatic test equipment must keep up with device scaling trends toward lower voltage, greater transistor and pincount; extended digital test patterns, improved accuracy, along with memory, and mixed analog and digital signals. The main issues seen by the test working group are as follows:

- Potential yield losses as the cycle time of manufactured devices becomes comparable to the timing accuracy of the ATE
- Increasing cost of capital equipment, driven by increasing pincount, high frequency, and ATE test features
- Requirement of test to support yield learning and defect detection, and failure analysis
- Changes in IDDQ focus as a test method

POTENTIAL YIELD LOSSES

Most of the technology problems causing major yield losses and cost increases are related to the slower growth of ATE speeds versus the ever improving device speed as shown in the *Overall Roadmap Technology Characteristics (ORTC)* Tables 1-6. For example, microprocessor and ASIC speeds require increasing accuracy for resolution of timing signals. While tester accuracy has improved at a rate of 12% per year, semiconductor speeds have improved at 30% per year. Typical headroom of testers five times faster than device speeds in the 1980s have all but disappeared. If the current trends continue, tester timing errors will eventually approach the cycle time of the fastest devices. In 1999, yield losses due to tester inaccuracy are becoming a problem. Table 16 shows the forecast trend for overall timing accuracy as defined by the SEMI

standards draft # 2928, *Specification For Overall Digital Timing Accuracy.*[3] Also shown is the device period, or cycle time, of high-end products over the roadmap period.

Table 16 Yield versus Test Accuracy

YEAR		1999	2001	2003	2005	2008	2011	2014
Yield	%	87	84	79	73	64	56	50
Device period	*ps*	830	700	580	500	400	340	260
Overall ATE accuracy (OTA)	*ps*	200	160	130	100	100	100	100
Overall device accuracy requirement	*ps*	42	35	29	25	20	17	13

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

AUTOMATED TEST EQUIPMENT COST

The ATE cost per pin for high-performance machines has remained essentially flat for the past 20 years at around $10–12K/pin. In 1999 this cost has begun to fall below $8K/pin. The future demands of higher speed, greater accuracy, more time sets, and increased vector memory will offset all the gains seen for reducing ATE cost. Therefore it may be difficult for high-pincount, 2000 MHz ATE to fall below $5K/pin in the future. That trend is expected to continue toward > $20M test systems unless there is a major change in IC device design incorporating more BIST, DFT, and high-frequency serial communication. By 2014, it may cost more to test a transistor than it costs to manufacture the transistor. This trend will mean a major change for the high-performance test systems and methodology that will allow DFT/BIST techniques to replace the traditional high-cost, at-speed function test.

TEST AND YIELD LEARNING

Although there are test issues related to cost and performance, test provides another major service for the semiconductor industry. Today the best tool for analysis of defects in the manufacturing process is the test equipment. Time-to-yield, time-to-money, time-to-quality, and time-to-market are all gated by test. The feedback loop derived from the test process is the only way to analyze and isolate many of the defects in today's processes. Test must continue to support cost-effective process measurements and defect isolation. The emergence of complex microprocessors as technology leaders in place of RAM devices is making these goals harder to realize.

The migration of CMOS technology towards 100 nm feature sizes will severely challenge the device failure analysis process. Improvements are needed in fail verification, fault localization, de-processing, and physical characterization. Two categories of needs are discussed: evolutionary or incremental, and revolutionary or breakthrough. While much will be served by evolutionary solutions, the fault localization challenge is especially acute and in need of major breakthroughs. It represents by far the most critical failure analysis need. Understanding failure mechanisms and providing corrective action cannot occur without the ability to localize faults to an area of the chip that can be inspected in a practical and cost-effective manner. Likewise, tools for yield improvement cannot be developed.

[3] SEMI. Standards Draft #2928, *Specification For Overall Digital Timing Accuracy.* In ballot phase.

EVOLUTIONARY NEEDS FOR DIAGNOSTICS

Incremental improvements to existing tools and techniques are required to keep pace with technology. Examples include regular increases in scanning electron microscope (SEM) resolution and the development of plasma delayering processes for new films. Many routine developments of this nature are required across the failure analysis process as follows:

- Wet and dry delayering processes for new films
- Focused ion beam cross-sectioning, milling, and deposition
- SEM and acoustic microscope resolution
- Integration of CAD navigation across the FA tool set
- Algorithms and software techniques to quickly determine defect locations
- Depackaging processes
- X-ray radiography resolution
- E-beam tester resolution, cross-talk, and others.
- Statistical techniques to extract information

REVOLUTIONARY NEEDS FOR DIAGNOSTICS

Revolutionary needs require major shifts in capability, driven by drastic changes in analytical method. Examples include high spatial resolution wafer backside thermal mapping and back-side waveform acquisition. Developments in this area are the most critical and require major efforts of industry, academia, the national laboratories, and analytical equipment suppliers. The following is a prioritized list of these needs:

1. Software-based fault localization tools compatible with major test methodologies such as SCAN, IDDQ, BIST, stuck-fault, AC test, dynamic logic, embedded cores. An especially important subset of these are tools for localization of AC or performance fails.
2. Hardware-based fault localization tools to complement and supplement the above as appropriate (such as migration of existing capability [waveform acquisition, emission testing, thermal mapping] to the backside of the chip and backside thinning techniques)
3. Inspection techniques beyond optical microscopy that offer high resolution without sacrificing throughput
4. Internal node DC micro-probing capability for characterizing individual circuit or transistor parameters or isolating leakage paths (Existing opto-mechanical systems are inadequate).
5. Signature analysis techniques to significantly reduce or eliminate the need for physical failure analysis
6. Software based diagnostics with the ability to locate defects on single transistors or on sections of conductors

IDDQ TESTING

Normal background leakages (both the amplitude and variability) are increasing to the point where IDDQ testing as it has historically been practiced may face difficulty for high end devices in the future. IDDQ provides a rich source of information about a manufactured chip and in many cases today plays a vital role in both defect detection and characterization. Alternative solutions must be developed to provide the same benefits in the face of the rising background leakage currents of future technologies.

Table 17 shows projected IDDQ values for performance-oriented products in future technologies. These values should not be precisely interpreted; instead they are meant to provide relative values as technology scales. Also, these numbers will be significantly lower for low-power technologies. These ranges are derived from the maximum device I_{OFF} (from *Process Integration* chapter Table 28), transistor counts (from ORTC Table 1), typical W/L ratios, and assuming a percentage of off transistors. It is assumed that the IC is designed appropriately to enable IDDQ testing. It is important to understand that actual values may be one

or two orders of magnitude lower for technologies optimized for power consumption. On the other hand, large high-performance ICs may exhibit larger values.

Table 17 Projected Performance-Oriented IC IDDQ Values

YEAR	MAXIMUM IDDQ
1999	5–30 mA
2001	30–70 mA
2003	70–150 mA
2005	150–400 mA
2008	400 mA–1.6 A
2011	1.6–8 A
2014	8–20 A

Not only are IDDQ values projected to increase in magnitude, but also the variability of IDDQ (for a given technology and product) is expected to be high. For example, although the IDDQ values in Table 17 represent the maximum, typical values could be significantly lower. It is important to better understand the components of this variability and to develop new test techniques so that this variability can be tolerated.

Below is a list of potential opportunities (both test methods and design-for-test techniques) for continuous use of IDDQ testing.

- Substrate biasing to control V_t
- Processing changes to have higher V_t (either for all devices or selected ones) or lower V_t variance
- IDDQ testing at low temperature or low voltage.
- Power supply partitioning at chip level. Use of multiple power sources
- Use of large "footer" devices that limit leakage currents in the transistor path.
- Transient IDD or other techniques that are less sensitive to higher background leakage currents
- "Signature-based techniques" — such as using IDDQ characteristics instead of single pass/fail threshold
- Built-in IDDQ sensors or other on-chip measurement aids

IDDQ has been an important failure analysis and characterization technique. Physical failure analysis relies on IDDQ for defect localization and defect type identification. In addition, there is important information about defective circuit behavior in the relationship between IDDQ and conditions such as temperature, voltage, and circuit state. As IDDQ goes up, however, some loss of diagnostic effectiveness using traditional techniques is possible.

There is also a need to improve the rate at which IDDQ measurements can be performed. Test equipment improvements or supported test fixture aids are preferred. Furthermore, IDDQ measurement resolution and accuracy at high currents must improve—particularly for emerging "signature-based" techniques.

HIGH-FREQUENCY SERIAL COMMUNICATIONS

Input/Output buffers for high-speed serial communications are now becoming essential for back plane applications, short and long-haul communications, and connecting computer peripherals. The rapid deployment of differential signal I/O buffers in ASICs and other ICs for systems such as such as SONET, Firewire, Gigabit Ethernet, and Fiber Channel is presenting several challenges for ATE manufacturers. At the present time, testing the functionality of these ICs can only be done by using expensive stand-alone pattern-generators and bit-error-rate detectors. The excessive test time and cost makes this approach impossible for volume production. There is an urgent need for ATE manufacturers to design multi-port, differential instruments and integrate them into test systems, including control software.

THE FOLLOWING ARE SOME OF THE CHALLENGES:

Frequency—The frequency of Si BiCMOS serial devices such as SONET, Gigabit Ethernet, and Fiber Channel is rapidly exceeding 1 Gbits/s and approaching 2.5 Gbits/s in 1999. With the development of SiGe technology, a 10 Gbits/s serial bus can potentially be integrated into CMOS ASICs in the near future. Meanwhile, ATE manufacturers are only beginning to introduce new systems with limited 1Gbits/s capability in 1999.

ATE comparators—also face challenges for device output specifications as low as 100 mV for LVDS buffers, 172 mV for Firewire, and 400 mV for most 2.5 Gbits/s buffers. While most comparators are designed with a minimum overdrive requirement of about 150 mV, special efforts are required to accurately strobe signals below 250 mV peak-to-peak.

Differential signals—Generally the differential signal voltage swing is smaller than V_{oh} - V_{ol} and can lie anywhere within the V_{oh} to V_{ol} range. For example, a 250 mV swing positioned between 1025 mV and 1375 mV. Therefore the signal cannot be tested using a single-ended comparator with a fixed voltage reference level. A true differential-mode comparator and a common mode comparator are needed for each pair of differential DUT output pins in addition to two single-ended comparators with V_{oh} to V_{ol} voltage reference levels. So far, very few ATE manufacturers have addressed this issue.

Differential timing skew—is another critical specification. Differential signals in serial communications circuits such as SONET, Gigabit Ethernet and Fiber Channel, must have cross-over points that are less than 20–25 ps from the true 50% crossing point. This timing skew is much smaller than the calibrated edge-placement-accuracy (EPA) of most ATE, which is generally above +/- 80 ps. One approach to achieving a 20 ps timing skew is to integrate pairs of tester drivers and comparators on the same piece of silicon with carefully matched cable lengths leading to the DUT.

HIGH-PERFORMANCE ASIC TEST REQUIREMENTS

The high-performance ASIC test requirements, Table 18, illustrates the demands that automatic test equipment (ATE) manufacturers must meet in terms such as pincount and frequencies. It is unlikely that ATE will ever be required to meet all of these demands on all pins simultaneously. For example, the highest off-chip data frequencies will probably occur on a relatively small number of serial communications pins operating at 1.25, 2.5 or 10 GHz rates, while the majority of DUT pins will probably operate at lower frequencies. This may restrict the total signal pins to a number below 3000 by the year 2014. The frequencies shown in Table 18 are for signal pins other than the serial communications pins. The number of externally stored, non-scan test vectors has not been shown. This number is around 32M in 1999, and could climb toward 1000M by the year 2005 if not constrained. Since this could greatly increase the cost of ATE and result in long vector load times, there is an urgent need for DUT designs incorporating DFT and BIST in the near future.

High-frequency local clocks are often generated on-chip using phase-locked-loop (PLL) oscillators. The demands on clock signals generated by the ATE at lower frequencies therefore lie more in the area of low jitter requirements that can be below 10 ps RMS when mixed-signal circuits are embedded. Quite often the ATE will provide a special clock pin that can provide a return-to-zero (RZ) waveform at the same rate as the nonreturn-to-zero (NRZ) input data to the DUT. This requires a special driver that can operate at twice the frequency of the normal data drivers in the pin electronics. The accuracy of the frequency generated by the ATE clock driver can range from +/- 20 ppm for SONET to +/- 100 ppm for other high-frequency serial communications devices.

Table 18a High-performance ASIC Test Requirements—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
Off-chip data frequency MHz NRZ* (see text)	600	700	800	900	1000	1100	1200
Overall timing accuracy (% period)	+/-5	+/-5	+/-5	+/-5	+/-5	+/-5	+/-5
ATE RMS clock jitter peak-to-peak ps	20	20	10	10	5	5	5
Signal peak-to-peak range V	1.5–3.3	1.4–3.3	1.3–3.3	1.2–3.3	1.0–3.3	1.0–2.5	0.9–2.5
Power/device DC with heat sink W	90	100	115	130	140	150	160
Transient power with heat sink W	135	150	170	195	210	225	240
Tester cost per high-frequency signal pin $K	4–8	3–7	3–7	3–6	3–6	2–5	2–5
Maximum number of I/O signal pads. Power and ground could double number for wafer test. (see text)	700	900	1100	1300	1500	1700	1900

Table 18b High-performance ASIC Test Requirements—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
Off-chip data frequency MHz NRZ* (see text)	1400	1600	1800
Overall timing accuracy (% period)	+/-5	+/-5	+/-5
ATE RMS clock jitter peak-to-peak ps	2	2	1
Signal peak-to-peak range V	0.6–2.5	0.5–2.5	0.4–2.5
Power/device DC with heat sink W	170	175	183
Transient power with heat sink W	255	262	275
Tester cost per high-frequency signal pin $K	2–5	2–5	2–5
Maximum number of I/O signal pads. Power and ground could double number for wafer test (see text)	2300	2700	3000

**NRZ—nonreturn-to-zero waveform (NRZ data rates are often referred to as Mbits/s)*

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

HIGH-PERFORMANCE MICROPROCESSOR TEST REQUIREMENTS

For years the VLSI test industry has been driven by increasing component requirements such as pincount, memory size, the number of patterns, system accuracy, voltage, and current. And for years the ATE industry has been able to keep up. It is no longer clear that the ATE industry can stay ahead of test requirements when bus speeds are approaching 1 GHz, power supplies must deliver hundreds of amps at one volt, and timing accuracy is measured in tens of picoseconds. And at what cost?

A look at the following microprocessor roadmap, Table 19a and b, suggests a continuation of these trends. ICs are becoming more complex due to higher levels of integration. Wide, very high-speed busses are common, analog circuits are appearing in digital ICs, and high levels of memory are also being embedded. Although product characterization and debug requirements will drive these trends, the ATE industry should not be led to believe that the semiconductor industry will be interested in doing volume production while functional testing at GHz speeds with pico second accuracy. More likely is a move to include DFT/ BIST, and more test methods all intended to do one thing—lessen the semiconductor industry's reliance on traditional, high-cost, full-feature testers.

Engineering development and debug will continue to need higher pincounts, higher bus frequencies, and hyper accurate testers, but the number of test systems required for engineering will be a fraction of the number of simpler systems needed for volume production. A later section on ATE requirements for testing ICs designed with DFT and BIST describes these simpler test systems in more detail.

In microprocessors roughly two-thirds of the pins are required for power and ground. This is to reduce the inductance and resistance in the power and ground connections that must conduct hundreds of amperes. In an engineering environment, microprocessors are generally characterized at temperature and voltage extremes that lead to test requirements beyond the needs of production. For example, low temperatures and high V_{dd} values will cause devices to run at higher frequencies with higher currents from the power supplies. Also, in a tester environment, the power supplies are far removed from the DUT. This necessitates large

bypass capacitors on the loadboard near the DUT socket to provide good regulation in the presence of high transient currents. The inclusion of 6000 uF in the footnotes should be translated to mean "power supplies that will not oscillate with high capacitive loads."

Microprocessors must also be tested with highly accurate test systems (Overall Timing Accuracy of roughly 70 ps) to avoid the yield loss illustrated in Table 16 near the beginning of the Test Roadmap. Not only is accuracy required to avoid yield loss, but it is also necessary for accurately binning parts into different frequency categories. High timing accuracy is also needed to perform accurate measurements on high-speed busses. The high timing accuracy requirement tends to keep the tester cost per pin high, and the mean time between failures (MTBF) low, compared with systems for testing less demanding ASICs.

Table 19a High-performance Microprocessor Test Requirements—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
Pincount							
Pincount I/O signal channels (maximum pins) [2]	768	1024	1024	1024	1024	1024	1024
Pincount power and ground (maximum pins)	1536	1536	2018	2018	2018	2018	2018
Busses							
Clock input frequency (MHz) [3]	800	933	1066	1200	1333	1466	1600
Clock accuracy (ps) [4]	62	53	47	42	37	34	31
Off-chip bus data rate (Mbits/s)	600	700	800	900	1000	1100	1200
Accuracy OTA (ps)	75	70	67	62	60	57	50
Number of independent clock domains	2	2	4	4	4	4	4
Number of independent busses	4	4	8	8	8	8	8
Embedded memory (Mbits)	32	32	64	64	128	128	256
APG frequency (MHz)	200	200	400	400	800	800	800
Algorithmic pattern generator (#X, Y addresses)	16	16	16	16	32	32	32
Algorithmic pattern generator (#Z addresses)	4	4	4	4	8	8	8
Power Supplies							
Power supply voltage range (volts) [1]	1.3–3.3	1.3–3.3	1.3–3.3	1.3–3.3	0.9–3.3	0.9–3.3	0.9–3.3
Power supply accuracy (% of programmed value AC+DC)	5	5	5	5	5	5	5
Maximum current (A)	200	200	220	220	242	242	266
Dynamic current slew rate response time (us)	1.00	1.00	0.90	0.90	0.81	0.81	0.73
Dynamic current slew rate settling time (us)	30	30	27	27	24	24	22
Patterns							
Vector memory (Meg–vectors per pin)	64	64	128	128	256	256	512
Vector memory load time (minutes)	15	15	15	15	15	15	15
Independent pattern management (# of patterns)	1000	1200	1200	1400	1400	1600	1600
Cost							
Tester cost per pin ($)	8000	7500	7000	6500	6000	5500	5000
Reliability							
MTBF (hours)	1000	1000	1150	1150	1323	1323	1521
MTTR (hours)	2	2	1	1	1	1	1
Availability (%)	98	98	98	98	99	99	99
Setup time (hours)	0.5	0.5	0.4	0.4	0.3	0.3	0.2

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Notes for Table 19 a and b High-performance Microprocessor Requirements

[1] *The power supply should be capable of handling 6000 uF, and current switching of 2X maximum current. The circuit can wake up between 1 to 20 cycles of the CPU clock.*

[2] *Maximum pincount is for debug tester purposes. Debug testers typically utilize the higher pincounts.*

[3] *Tester should be capable of handling RAMBUS type of Data Rates and protocol. Characterization testers need to meet full data rate requirements. Production tester—Accuracy of measurement of "output to output" will be critical.*

[4] *The tester needs to supply the clock as a bypass mode for the device for debug. On board PLL will be the main test strategy.*

Table 19b High-performance Microprocessor Test Requirements—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
Pincount			
Pincount I/O signal channels (maximum pins) *[2]*	1280	1408	1472
Pincount power and ground (maximum pins)	2560	2816	2944
Busses			
Clock input frequency (MHz) *[3]*	1866	2133	2400
Clock accuracy (ps) *[4]*	27	23	20
Off-chip bus data rate (Mbits/s)	1400	1600	1800
Accuracy OTA (ps)	45	40	35
Number of independent clock domains	4	4	4
Number of independent busses	8	8	8
Embedded memory (Mbits)	512	2048	2048
APG frequency (MHz)	1200	1600	1600
Algorithmic pattern generator (#X, Y addresses)	64	64	64
Algorithmic pattern generator (#Z addresses)	16	16	16
Power Supplies			
Power supply voltage range (volts) *[1]*	0.6–2.5	0.6–1.3	0.6–1.3
Power supply accuracy (% of programmed value AC+ DC)	5	5	5
Maximum current (A)	293	322	355
Dynamic current slew rate response time (us)	0.66	0.59	0.53
Dynamic current slew rate settling time (us)	19	17	15
Patterns			
Vector memory (meg–vectors per pin)	1024	4096	4096
Vector memory load time (minutes)	15	15	15
Independent pattern management (# of patterns)	2074	2488	2986
Cost			
Tester cost per pin ($)	4000	2000	1500
Reliability			
MTBF (hours)	1500	1700	2000
MTTR (hours)	1	1	1
Availability (%)	99	99	99
Setup time (hours)	0.2	0.2	0.2

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

LOW-END MICROCONTROLLER TEST REQUIREMENTS

Low-end microcontrollers are not the drivers for leading edge silicon technology, but due to their tremendous volume and sales (1998 estimate—4B units and $10B+ in sales) they have driven the development of ATE systems optimized for testing microcontrollers.

Microcontrollers are chips that contain a 4, 8, 16, or 32 bit processor, some type of memory, I/O, and various other peripherals such as A/D and D/A converters, PLLs, sensors, and timers. Microcontroller pincounts range from 3 pins for serial I/O devices used in smartcards, to hundreds of pins for applications such as PDAs and engine controllers. Microcontroller bus frequencies range from the low-end 5-10MHz range up to 50–60MHz.

Microcontrollers that are driving the optimized tester are typically low-cost, sometimes sub-dollar priced, 4 and 8 bit microcontrollers. This very high-volume segment has driven the development low-speed digital

ATE systems capable of testing 4–8 microcontrollers in parallel. For some of these very low-cost microcontrollers, test cost exceeds their manufacturing costs. Testing of this segment of microcontrollers has driven tester costs down to the $2K/pin range.

The difficult challenges for microcontroller testing generally concern reducing the overall cost of test. Lowering the tester purchase price is a large part of this challenge as well as increased multi-site testing and equipment utilization. As microcontroller integration levels increase, there will be an increasing need for more mixed-signal test capability in low-cost testers. See Table 20.

Table 20a Low-End Microcontroller Test Requirements—Near Term

YEAR TECHNOLOGY NODE	*1999 180 nm*	*2000*	*2001*	*2002 130 nm*	*2003*	*2004*	*2005 100 nm*
Device Characteristics							
Pincount: minimum/maximum total pins	3/160	3/180	3/200	3/210	3/220	3/230	3/250
Bus frequency (MHz)	60	70	80	85	90	95	100
Clock frequency (MHz)	60	70	80	85	90	95	100
Internal frequency (MHz)	60	100	150	175	200	225	250
Low V_{dd} (V)	1.8	1.4	1.2	1.0	0.8	0.8	0.8
# of DPS (device power supply) per device	3	3	3	3	3	3	3
Device power (mW)	300	300	300	300	300	300	300
Maximum driver level (V) *[A]*	8	10	12	12	15	20	30
Maximum comparator level (V) *[A]*	8	10	12	12	15	20	30
Embedded memory (Mbits)	8	12	*16*	*20*	*32*	*32*	*32*
Mixed-signal circuitry	A/D, D/A	Audio	Video	Sensors	RF	—	—
Tester Characteristics							
Overall timing accuracy (% period)	5	5	5	5	5	5	5
RMS clock jitter (ps)	100	100	100	75	75	50	50
External test vectors (M) *[B]*	8	8	8	12	12	12	12
Tester cost range ($K/per pin)	2–4	2–4	2–4	1.5–3	1.5–3	1.3–3	1.3–3
Reliability—MTBF (hrs)	2000	2200	2500	2800	3000	3200	3400
DPS maximum voltage (V)	8	8	8	8	8	12	16
Maximum DPS in tester	16	32	32	48	48	64	64
Maximum devices for parallel testing *[C]*	8	16	16	16	24	24	24
Maximum tester pins	1024	1024	1024	1024	1536	1536	1536
Mixed-signal instrumentation	A/D, D/A		Audio Frequency	—	Video Frequency	—	Sensors

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Notes for Table 20a and b Microcontroller Requirements

[A] *Driver and comparator levels increase to support additional mixed-signal and other special test requirements. All pins will not require this higher voltage.*

[B] *Without BIST or DFT. Number will be smaller if acceptable BIST and/or DFT solutions are developed*

[C] *This category is for parallel testing of microcontrollers, and is not to be confused with parallel testing of memories.*

Table 20b Low-End Microcontroller Test Requirements—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
Device Characteristics			
Pincount: minimum/maximum pins	3/270	3/300	3/350
Bus frequency (MHz)	120	150	200
Clock frequency (MHz)	120	150	200
Internal frequency (MHz)	300	350	450
Low V_{dd} (V)	0.8	0.7	0.6
# of DPS (device power supply) per device	2	2	1
Device power (mW)	400	500	400
Max driver level (V) *(Note A)*	30	30	50
Max comparator level (V) *(Note A)*	30	30	50
Embedded memory (Mbits)	64	96	128
Mixed-signal circuitry			
Tester Characteristics			
Overall timing accuracy (% period)	5	5	5
RMS clock jitter (ps)	50	25	25
External test vectors(M) *(Note B)*	16	24	32
Tester cost ($K/per pin)	1.2–3	1–3	0.5–2
Reliability—MTBF (hrs)	4000	5000	6000
DPS maximum voltage (V)	16	16	16
Maximum DPS in tester	64	64	128
Maximum devices for parallel testing *(Note C)*	32	32	64
Maximum tester pins	1536	2048	2048
Mixed-signal instrumentation			

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

MIXED-SIGNAL TESTING

The trend of more system functionality on a single piece of silicon will increasingly blur the lines between traditional digital, analog, RF/microwave and mixed-signal devices. This trend will drive test equipment toward a single platform solution that can test whatever happens to find its way onto a single piece of silicon. The digital requirements for mixed-signal test equipment are the same as for purely digital chips and are shown in the Microprocessor and ASIC tables. The trend in test equipment is toward a modular high speed and high pincount digital test platform where high-performance analog/RF/microwave Instruments can be added as needed. The analog test issues and test technology limiters are higher bandwidth, higher direct conversion sampling rates, higher dynamic range, lower noise floors, seamless integration of the digital and analog instruments and cost.

The mixed-signal test equipment requirements focuses on test instruments rather than IC devices. As illustrated in Table 21, the current analog/RF/microwave testing methodology requires performance-based measurements; therefore, instrument needs reflect the increasing device performance predicted in the process/packaging technology roadmaps. This trend, of increasing instrument performance, is expected to continue and will drive up the cost of test equipment. Costs will also be driven up by the variety of analog instruments, and the quantity needed for multi-site testing. No proven alternative to performance-based analog testing, using external (from the chip) instruments, exists. More research in this area is needed. Analog built-in-self-test has been suggested as a possible solution and area for more research.

IMPORTANT AREAS OF CONCERN

The analog/RF/microwave signal environment seriously complicates load board design and test methodology. Noise, crosstalk, signal mixing, and load board issues will dominate the test development process and schedule.

Jitter and performance testing of high-speed serial interfaces is a serious challenge for automatic test equipment. The digital complexity and volumes for these devices will increase beyond the capability of current "rack and stack" test methodology. High-speed serial interfaces such as Gigabit Ethernet, SONET, and Fiber Channel are being designed into chips with larger digital content.

Parallel test of all analog functions is needed to reduce test cost. This requires multiple instruments with fast parallel execution of DSP test algorithms (such as FFTs). Parallel test has been used for many years for memory and large runner digital devices but not to a large extent on mixed-signal devices. Also, multiple analog functions on a single chip (for example dual, quad, octal LAN ports) must be tested simultaneously.

Better software tools that apply to more than one test equipment supplier are needed. Tools are required for digital and mixed-signal vector generation, circuit simulation of the device's analog circuitry along with the loadboard and the test instruments, and rapid mixed-signal test program generation. Currently mixed-signal test programs are manually generated, whereas automatic test program generators are widely used for generating digital test.

Table 21a Mixed-signal Test Requirements—Near Term

YEAR *TECHNOLOGY NODE*	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*
Low Frequency Source and Digitizer							
BW * (MHz)	15	15	100	100	100	100	100
Fs** MS/s***	5	5	5	5	5	5	10
Bits	20–23	20–23	20–23	20–23	20–23	20–23	20–23
Noise floor (dB/RT Hz)	-155	-155	-160	-160	-160	-160	-160
High Frequency Waveform Source							
Level V (peak-to-peak) accuracy (+/-)	4 0.5%	4 0.5%	4 0.5%	4 0.5%	4 0.5%	4 0.5%	4 0.5%
BW (MHz)	800	1200	1600	2400	2400	2400	3000
Fs (MS/s)	2000	3000	4000	6000	6000	6000	7500
Bits AWG/Sine†	10/14	10/14	10/14	10/14	10/14	10/14	10/14
Noise floor (dB/RT Hz)	-140	-140	-145	-145	-150	-150	-155
High Frequency Waveform Digitizer							
Level V (peak-to-peak) accuracy (+/-)	4 0.5%	4 0.5%	4 0.5%	4 0.5%	4 0.5%	4 0.5%	4 0.5%
BW (MHz) (undersampled)	1000	1500	2000	2500	2500	2500	3000
Fs (MS/s)	1/100	1/100	1/200	1/300	1/300	1/300	1/400
Bits	16/12	16/12	16/12	16/12	16/12	16/12	18/14
Noise floor (dB/RT Hz)	-140	-140	-145	-145	-150	-150	-155
High Speed Sampler							
BW (GHz)	2	3.6	3.6	5	5	5	5
Resolution (bits)	16	16	16	16	16	16	16
Time Measurement							
Jitter measurement (ps RMS)	5	3	3	2	2	1	1
Frequency measurement (MHz)	660	660	660	1320	1320	1320	2640
Single shot time capability (ps)	100	100	100	75	75	75	50
RF/Microwave Instrumentation							
Source BW (GHz)	6	6	10	14	14	18	18
Source phase noise low frequency close-in 1KHz (dBc/Hz)	-126	-126	-130	-136	-136	-136	-136
Source phase noise high frequency wideband 10MHz (dBc/Hz)	-160	-160	-160	-166	-166	-166	-166
Receive BW (GHz)	6	6	10	14	14	14	18
Receive noise floor (dBm/Hz)	-160	-160	-160	-160	-160	-160	-160
Receive dynamic range SFDR (dBc) ‡	95	95	105	105	105	105	105
Special Digital Capabilities							
D/A and A/D data rate (Mbits/s) §	150	150	300	300	400	400	400
Sample clock jitter (< ps RMS)	3	3	1.5	1.5	1	1	1
Serial data rate (Mbits/s)	2500	2500	4000	10000	10000	10000	10000

** BW—bandwidth*
*** Fs—sample rate*
**** MS/s—mega samples per second*
† AWG/Sin—arbitrary waveform generation/sine wave
‡ SFDR—spurious free dynamic range
§Mbits/s—mega bits per second

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 21b Mixed-signal Test Requirements—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
Low-Frequency Source and Digitizer			
BW * (MHz)	100	100	100
Fs** MS/s***	10	10	10
Bits	20–23	20–23	20–23
Noise floor (dB/RT Hz)	-160	-160	-160
High Frequency Waveform Source			
Level V (peak-to-peak) Accuracy	4 0.5%	4 0.5%	4 0.5%
BW (MHz)	4000	5000	5000
Fs (MS/s)	10000	12500	12500
Bits AWG/Sine†	10/14	10/14	10/14
Noise floor (dB/RT Hz)	-155	-155	-155
High Frequency Waveform Digitizer			
Level V (peak-to-peak) accuracy	4 0.5%	4 0.5%	4 0.5%
BW (MHz) (undersampled)	4000	5000	5000
Fs (MS/s)	1/600	1/800	1/1200
Bits	18/14	18/14	18/14
Noise floor (dB/RT Hz)	-155	-155	-155
High Speed Sampler			
BW (GHz)	5	5	5
Resolution (bits)	16	16	16
Time Measurement			
Jitter measurement (ps RMS)	1	1	1
Frequency measurement (MHz)	3000	3000	3000
Single shot time capability (ps)	30	30	30
RF/Microwave Instrumentation			
Source BW (GHz)	36	36	36
Source phase noise low frequency close-in 1KHz (dBc/Hz)	-136	-136	-136
Source phase noise high frequency wideband 10MHz (dBc/Hz)	-166	-166	-166
Receive BW (GHz)	36	36	36
Receive noise floor (dBm/Hz)	-160	-160	-160
Receive dynamic range SFDR (dBc) ‡	105	105	105
Special Digital Capabilities			
D/A and A/D data rate (Mbits/s) §	600	600	600
Sample clock jitter (< ps RMS)	0.5	0.5	0.5
Serial data rate (Mbits/s)	10000	10000	10000

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Notes for Table 21a and b Mixed-Signal Requirements

Low-Frequency Source And Digitizer—This is the basic, minimum, instrument set of any mixed-signal tester. Telecommunications, advanced audio and wireless baseband will drive these specifications. Differential inputs/outputs are needed.

High-frequency Waveform Source—Disk-drive read channels (PRML) will drive sample rate and bandwidth. Local area network (LAN) devices will drive sample rate, bit resolution and amplitude accuracy. Differential outputs are needed.

High-Frequency Waveform Digitizer—An undersampled (such as down conversion, and track-and-hold) bandwidth is shown. The sample rates and bit resolutions are for a direct conversion digitizer, which is usually preceded by the undersampler. PRML and LAN devices will drive digitizer specifications. Differential inputs are needed.

High-Speed Sampler—The high bandwidth, high resolution, undersampler could be replaced with the high frequency waveform digitizer when the digitizer had sufficient bandwidth.

Time Measurement—Phase Lock Loops (PLLs), which are increasingly being embedded in new designs, will require jitter and frequency measurements. A specialized class of instruments will have to be developed to make these measurements efficiently and accurately.

Rf/Microwave Instrumentation—Single chip RF/digital/baseband/audio devices will require RF instruments such as modulated carrier sources and low-noise receivers or down converters.

Digital Signal Data Rate—The digital signal data rates on a parallel bus will track A/D and D/A conversion rates. Serial pin data rates are driven by LAN, SONET and fiber communication channels.

TEST REQUIREMENTS FOR SEMICONDUCTOR MEMORIES

It is expected that the memory density will grow continually at an exponential rate. Semiconductor memories will continue to be the test vehicle for process technologies. The DRAM will continue to be the leading device to define the process technology, design and test. Refer to Tables 22 through 24.

COMMODITY DRAM TESTING

We expect that the number of DRAM bits will continue to quadruple in every three years. This increasing size will cause the test to be a manufacturing bottleneck. To enhance test productivity, new test oriented architectures will be required. Multi-bit testing, BIST and built-in self-repair will be essential to maintain production throughput and yield.

A considerable parallelism in test from the automatic tester equipment will be required. The number of devices simultaneously tested refers to the packaged devices tested at-speed. In the realm of 2 GHz and above, there is a bottleneck with the device exterior and the interface such as signal transmission method, socket, probing, and handling. Because of required timing accuracy and the increase in cost for test/device interface components, testers will not exceed 64 devices per test head.

The primary fault models for DRAMs will continue to be cell stuck-at, multi-cell coupling, decoder open, and data retention faults. For 100 nm feature sizes and below, inline defect detection will be necessary for product development. With inline defect monitoring, processing of defective wafers will be avoided and test time for wafer sort and package level test will be maintained.

Table 22a Commodity DRAM Test Requirements—Near Term

YEAR *TECHNOLOGY NODE*	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*
DRAM capacity (Gbits): R & D	1			4			16
Mass Production	0.256			1			4
DRAM data rate (GHz): R & D	1.0		1.3		1.6		2.0
Mass Production	0.250		1.0		1.3		2.0
DRAM access time (ns): R & D	2.5		2		1		0.5
Mass Production	8		4		2.5		2
DRAM bit width/device (Mass Production)	8		16		16		16
Tester data rate (GHz): R & D	1.0		1.3		1.6		2.0
Mass Production	0.25		1.0		1.3		2.0
Overall timing accuracy (ps): R & D	100		60		50		40
Mass Production	300		80		60		50
Simultaneous testing (devices/test head)	32		32/64		64		64
Test channels (Mass Production)	1500*		1200 2300**		2300		2300

** Assuming SDRAM with 32 devices/station, Driver 800, I/O 640*

*** Assuming RAMBUS with: (1) 32 devices/station, Driver 480, I/O 640; (2) 64 devices/station, Driver 960, I/O 1280*

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 22b Commodity DRAM Test Requirements—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
DRAM capacity (Gbits): R & D Mass Production	64 16	256 64	1024 256
DRAM data rate (GHz): R & D Mass Production	2.4 2.2	3.0 2.6	3.6 3.0
DRAM access time (ns): R & D Mass Production	0.3 1	0.2 1	0.15 0.8
DRAM bit width/device (Mass Production)	32	32	32
Tester data rate (GHz): R & D Mass Production	2.4 2.2	3.0 2.6	3.6 3.0
Overall timing accuracy (ps): R & D Mass Production	30 40	25 30	20 25
Simultaneous testing (Devices/test head)	64	64	64
Test channels (Mass Production)	3500*	3500	3500

* *Assuming RAMBUS with 64 devices/station, Driver 960, I/O 2560*

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COMMODITY FLASH MEMORY TESTING

Commodity Flash memory architecture varies substantially (serial, fixed block, boot block, burst) based on application. Continued architectural diversification is expected. Bit density doubling every two years is expected to continue along with a continued decrease in operating voltages. Bus width has followed that of micro-controllers, so a transition to 32 bits is expected during the next five years. Flash data burst rates are tied closely to the micro-controller roadmap.

Energy consumption of Flash memories that are used in battery powered applications is a critical parameter, therefore testers must provide a means of measuring the low levels of current or energy consumed by Flash components. Wafer test generally does not require the AC performance of package test, but it does require high control and flexibility of the device under test. Redundancy is essential for Flash memories and can be implemented during wafer and package testing. Error capture and analysis methodology should allow high flexibility to the test engineer.

Vector test capability is required because many Flash components contain an embedded processor for program/erase control. The presence of the embedded processor allows feature additions to commodity Flash devices that may force additional logic or analog test needs in the future.

Table 23a Commodity Flash Memory Test Requirements—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
Device Characteristics							
Density (Megabits): volume production	32	64	64	128	128	256	256
Density (Megabits): lead density	256	256	512	512	1024	1024	2048
Data width (bits)	16	16	32	32	32	32	32
Simultaneously tested devices (wafer test)	16	32	64	64	64	64	64
Simultaneously tested devices (package test)	32	64	64	64	64	64	64
Power Supplies							
Power supply voltage range (Volts)	1.3-5.5	1.3-5.5	0.6-5.5	0.6-5.5	0.6-5.5	0.6-3.3	0.6-3.3
Power Supply accuracy (% of programmed value)	5	5	5	5	5	5	5
Maximum current (mA)	200	200	200	200	200	200	200
Programming power supply voltage range (Volts)	1.3-13.0	1.3-13.0	0.6-10.0	0.6-10.0	0.6-10.0	0.6-10.0	0.6-10.0
Pattern Generator							
Tester channels	48	56	64	64	64	64	64
Vector depth (k)	128	128	1000	1000	1000	1000	1000
APG X, Y, Z addresses	16	16	16	16	16	16	16
Timing							
Maximum data rate (MHz)	50	66	80	100	125	133	166
Accuracy OTA (ns)	1	1	.75	.6	.6	.5	.5
Cost							
Tester cost per pin ($) *[1]*	1300	1150	1000	850	725	610	525
Reliability							
MTBF (hours)	2000	2500	3000	3500	4000	4500	5000
MTTR (hours)	1	1	1	1	1	1	1
Availability (%)	98	98	99	99	99.5	99.5	99.5
Setup time (hours)	.5	.5	.4	.4	.3	.3	.2

Notes for Table 23a and b Commodity Flash Memory Test Requirements:

[1] Overall tester cost is: (per pin cost) × (number of channels) × (number of simultaneously tested).

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 23b Commodity Flash Memory Test Requirements—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
Device Characteristics			
Density (Gbits): volume production	0.512	2.048	8.192
Density (Gbits): lead density	4.096	16.384	65.536
Data width (bits)	32	32	32
Simultaneously tested devices (wafer test)	64	128	128
Simultaneously tested devices (packaged test)	64	128	128
Power Supplies			
Power supply voltage range (Volts)	0.6–3.3	0.6–3.3	0.6–3.3
Power supply accuracy (% of programmed value)	5	5	5
Maximum current (mA)	200	200	200
Programming power supply voltage range (Volts)	0.6–8.0	0.6–8.0	0.6–8.0
Pattern Generator			
Tester channels	72	72	72
Vector depth (k)	2000	2000	2000
APG X, Y, Z addresses	16	16	16
Timing			
Maximum data rate (MHz)	200	250	300
Accuracy OTA (ns)	.33	.2	.1
Power Supplies			
Tester cost per pin ($) [1]	500	450	400
Reliability			
MTBF (hours)	6000	6500	7000
MTTR (hours)	.5	.5	.5
Availability (%)	99.5	99.5	99.5
Setup time (hours)	.2	.2	.2

Notes for Table 23a and b Commodity Flash Memory Test Requirements:

[1] *Overall tester cost is: (per pin cost) × (number of channels) × (number of simultaneously tested).*

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EMBEDDED DRAM AND EMBEDDED FLASH TESTING

The number of embedded DRAM bits will double every two years. The major concern in the merged logic-DRAM will be array noise and sense-amp imbalance. For 100 nm feature size and below, inline defect detection will be necessary for product development. With inline defect monitoring, processing of defective wafers will be avoided and test time for wafer sort and package level test will be maintained.

Embedded Flash memory bits will grow exponentially. It is also expected that more and more ICs will include both DRAM and flash memories. Oxide reliability, sense-amp imbalance, and oxide-nitride-oxide (ONO) scaling will be the major concerns in flash memories from 2001 and onwards. Refer to Table 25.

To enhance the test productivity, new test oriented architectures will be required. Built-in self-test and built-in self-repair will be essential to test embedded DRAM and embedded Flash memories and to maintain the production throughput and yield. The primary test algorithms for Flash memories will continue to be Read-disturb, Program-disturb, and Erase-disturb while March tests with all data background will be essential for embedded DRAM.

A considerable parallelism in test will be required. It is expected that by year 2001 and onwards, test will become cost effective in double insertion of devices rather than testing both logic and embedded memories on the logic tester. In double insertion, embedded Flash and DRAMs will be tested and repaired on the memory tester, while the logic blocks will be tested on the logic tester.

Table 24a Embedded DRAM Test Requirements—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
Embedded DRAM size (Mbits): R & D Mass Production	64 32		128 64		256 128		512 256
Failure concerns	Particle defects; data retention		Particle defects; array noise; data retention		Particle defects; array noise; sense-amp imbalance		Particle defects; array noise; sense-amp imbalance
Wafer level test	Single insertion		Double insertion		Double insertion		Double insertion
Usage of on-chip test	50% BIST 50% BISR		100% BIST 100% BISR		100% BIST 100% BISR		100% BIST 100% BISR

Table 24b Embedded DRAM Test Requirements—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
Embedded DRAM size (Gbits): R & D Mass Production	1 0.512	2 1	4 2
Failure concerns	Particle defects; array noise; sense-amp imbalance	Particle defects; array noise; sense-amp imbalance	Particle defects; array noise; sense-amp imbalance
Wafer level test	Inline defect detection; double insertion	Inline defect detection; double insertion	Inline defect detection; double insertion
Usage of on-chip test	100% BIST 100% BISR	100% BIST 100% BISR	100% BIST 100% BISR

Number of bits in mass production is approximately 50% of number of bits in R&D

Solutions Exist   *Solutions Being Pursued*   *No Known Solutions*

Table 25a Embedded Flash Memory Test Requirements—Near Term

YEAR TECHNOLOGY NODE	1999 180 NM	2000	2001	2002 130 NM	2003	2004	2005 100 NM
Embedded Flash size (Mbits): R & D	4		16		32		64
Mass Production	2		4		16		32
Embedded mixed memory size (Mbits): Flash	0.256		1		4		16
DRAM	1		4		16		32
Failure concerns	Oxide defects; # of erase cycles		Oxide defects; ONO scaling		Oxide defects; ONO scaling; over erase		Oxide defects; ONO scaling; over erase
Wafer level test	Single insertion		Single insertion		Double insertion		Double insertion
Usage of on-chip test	50% BIST 50% BISR		100% BIST 100% BISR		100% BIST 100% BISR		100% BIST 100% BISR

Table 25b Embedded Flash Memory Test Requirements—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
Embedded Flash size (Mbits): R & D	128	256	512
Mass Production	64	64	128
Embedded mixed memory size (Mbits): Flash	32	64	128
DRAM	32	64	128
Failure concerns	Oxide defects; ONO scaling; sense-amp imbalance	Oxide defects; ONO scaling; sense-amp imbalance	Oxide defects; ONO scaling; sense-amp imbalance
Wafer level test	Inline defect detection; double insertion	Inline defect detection; double insertion	Inline defect detection; double insertion
Usage of on-chip test	100% BIST 100% BISR	100% BIST 100% BISR	100% BIST 100% BISR

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

EQUIPMENT FOR TESTING DEVICES DESIGNED WITH DFT

This section describes low-cost ATE for testing ICs designed with DFT. This avoids the escalating cost of ATE predicted by a non-DFT scenario. Refer to Table 26 to review the technology requirements for DFT-BIST devices. If testers continue on the full-pin, at-speed, functional test route, costs will exceed $20M per tester by the year 2014. Similarly, test times on these very expensive testers will approach hours per device because of the increasing patterns required across the fixed bandwidth tester/device interface. Several device manufacturers have developed DFT methodologies with ATE costs approaching only $200/pin for currently available technologies. These methodologies utilize scan/boundary scan methods along with parametric tests to reduce the number of ATE full-function pins required to test a high pincount part . The full-function pins may only be 64. This allows the ATE design to be reduced to parametric functions only on all other pins. This also eases the requirements for parallel test allowing further reduction in effective test cost.

Further complication of this picture with today's technologies includes the addition of embedded DRAM, mixed-signal applications, FPGA, and nonvolatile storage.

TABLE ENTRY DESCRIPTIONS

- *Scan chains and scan vectors* show a flattening in later years as the industry approaches the "affordable" pattern application volumes and the "slack" is picked up by Logic BIST. The product of scan chains times vectors is smaller than signal channels times vectors shown in the Microprocessor Table 19 because of higher fault detection efficiency with scan. Many ATPG tools are available that support scan testing.
- *Non Scan pins*—Generally address the control of boundary isolation , scan and clocking of the digital portion, and control and test of non-scan tested elements on the DUT. This shows an increase over time to address the increasing complexity of the non-scan tested portion of the DUT, and to some extent the increase in complexity of the scan-tested portion.
- *Total "Full-Function" pins*—Pins equivalent in function to typical ATE digital pins. This is the total pin set required to test the internals of the DUT.
- *Total "Reduced-Function"*—This is the set of pins required to test the DUT external to the boundary scan chain. Functionality is that of typical ATE DC parametrics . These pins are required at some levels of test to verify the parametrics and do contact testing on pins other than the DUT full-function pins. The complication and cost of higher pincounts in later years will drive the economics for implementation of DFT for on-chip methods for doing these types of tests.
- *Parallel sites*—Parallel test is an excellent test cost reducer. In the case (for example wafer test) where only the full-function pins need be contacted, high parallelism (8–32) is easily realizable (typical of DRAM today). Tradeoffs can be made with the total full-function pins available per device and the number of parallel DUTs tested. In the case where the reduced-function pins are required, then lesser levels of parallelism are necessary, and again tradeoffs can be made between the maximum reduced-function pins available to a device and the number of devices that can be tested in parallel.
- *Base data rate*—This is essentially controlled by the scan rate. Higher on-chip speeds are attained using the high-speed clock function and/or structural AC testing and/or on-chip clock generation.
- *High speed clock*—These are a few pins capable of much higher frequencies than the rest of the machine for the purposes of running internal functional/Logic BIST (LBIST) patterns at speed internal to the DUT. These also have the requirement to be able to burst at high frequencies and have low skew relative to other high-speed clock pins in order to perform AC path delay measurements internal to the DUT. The relative skews/burst frequencies will be at the higher end of maximum chip frequencies to stress these conditions. These functions need to be higher than the roadmap clocking frequencies to stress these conditions. These functions will become inadequate in later years because of frequency/accuracy limitations of the ATE/ DUT interface, and will require on-chip DFT assistance.
- *Mixed-signal functionality*—These functions may be needed as the devices acquire mixed-signal content. Some of the circuits traditionally tested via mixed-signal techniques will be production tested by means of DC tests to avoid the additional costs of the mixed-signal features and performance board development costs. As analog content increases on chips, economics will drive DFT for mixed-signal to avoid—the ATE costs, the cost of serialized test of multiple analog functions. and the longer development times of mixed-signal tests, especially in the economics of lower volume ASICs markets.

DESIGN DFT REQUIREMENTS

- *Logic BIST*—As digital parts get progressively larger in the future, the external pattern volume (SCAN or other) becomes prohibitive to apply (test time = $$) and still maintain the "high" fault coverage necessary for the desired quality (even with the low-cost ATE). Development of a Logic BIST methodology to get past the tester/DUT bandwidth bottleneck is necessary, and it will be necessary to drive the LBIST coverage to higher and higher fault coverage percentages. The test time problem will be compounded by the addition of nondigital content to the DUT.
- *SRAM and DRAM BIST*—Addition of SRAM and DRAM BIST is an economic tradeoff between additional ATE cost and the cost of implementing these functions on-chip. Also entering into consideration is use in the final application, performance attainable, and tester/DUT bandwidth limitations on pattern application rate.
- *Noncontact parametrics*—As pincounts rise higher, the cost of applying parametric tests to the circuitry outside the boundary scan increases. At some point the economics justifies the inclusion of DFT for "noncontact parametrics" both from an ATE cost standpoint and a KGD standpoint.

- *Clocking DFT*—Delivering clocks in the high hundreds of MHz with jitter figures in the low tens of picoseconds is costly and somewhat problematic given the performance board constraints and the pincounts and contacting constraints. ATE performance specifications cannot take into account crosstalk and ground bounce induced jitter due to the performance board design, which may be a more significant factor in DUT performance. On-chip clock generation with frequency multiplication is often necessary to prevent the ATE/interface from limiting the chip performance, but a low-jitter clock input from the ATE is still required.

Table 26a DFT-BIST Device Test Requirements—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
DFT/BIST ATE Characteristics								
Scan chains (chains) (See text for comment on number)	16–64	16–64	24–64	24–64	32–92	32–92	32–128	*Logic Density*
Scan vectors (M-Vectors) (3 bits/ vector minimum) at maximum width	4–16	4–16	8–32	8–32	8–32	8–64	8–64	*Logic Density*
DFT Required to Cap test application time "Logic BIST"			Logic BIST to 90%	Logic BIST to 93%	Logic BIST to 95%	Logic BIST to 98%	Logic BIST to 99%	*Test Time*
DFT Required to prevent addition of APG into ATE "SRAM + DRAM BIST"	Yes	Yes	Yes	Yes	Yes	Yes	Yes	*Cost*
Vector rate (MHz)	50–100	100–200	100–200	100–200	100–200	200	200	*Test Time*
Nonscan pin vectors (M-Vectors)	4–8	4–16	4–16	4–16	4–16	8–24	8–24	*Logic Density*
Total "full function" pincount [Scan+nonscan per socket (pins)]	64–128	64–128	64–256	64–256	64–256	64–256	64–256	*Test Time*
System base data rate (MHz)	100–200	100–200	200	200	200	200	200	*Test Time*
Number of parallel sites (sites)	2–4	4–16	4–16	4–16	4–16	4–16	8–32	*Cost*
Specialized Functions								
Total "reduced function" pincount *	512–1000	512–1200	512–1350	512–1500	512–1700	512–1850	512–2000	*I/O Density*
DFT for noncontact parametrics	No	No	Maybe	Maybe	Maybe	Maybe	Yes	*Cost*
High speed clock pins (differential pairs)	1	2	2	4	4	4	4	*Clock Domains*
ATE high speed clock frequency (MHz)	800	1000	1600	2000	2500	3200	4000	*On-chip Clock Rate*
ATE high speed clock [Accuracy+skew (ps)]	100	75	50	40	30	25	20	*On-chip Clock Rate*
ATE high speed clock jitter (ps peak-to-peak)	50	30	25	20	15	12	10	*On-chip Clock Rate*
High speed clock burst number of pulses	4	5	5	6	6	10	10	*Sequential Depth*
High speed clock burst maximum frequency (MHz)	800	1000	1600	2000	2500	3200	4000	*On-chip Clock Rate*
DFT Required for clocks	No	Maybe	Maybe	Maybe	Yes	Yes	Yes	*Cost*
Signature compression per pin	Yes	Yes	Yes	Yes	Yes	Yes	Yes	*Test Methods*
Mixed-signal audio pin pairs	1	2	2	2	2	2	2	*SoC*
Mixed-signal video pin pairs	1	1	1	2	2	2	2	*SoC*
Mixed-signal RF pin pairs	—	1	1	2	2	2	2	*SoC*
DFT to aid ATE in meeting mixed-signal requirements and/or decrease cost	—	Maybe	Maybe	Yes	Yes	Yes	Yes	*Cost*

* *Without high-frequency serial communications*

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 26b DFT-BIST Device Test Requirements—Long Term

YEAR *TECHNOLOGY NODE*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*	*DRIVER*
DFT required to cap test application time "Logic BIST"	Yes	Yes	Yes	*Test Time/Cost*
Total "reduced function" pincount *	512–2400	512–3000	512–4000	*I/O*
DFT for noncontact parametrics	Yes	Yes	Yes	*Cost*
ATE high speed clock frequency (MHz)	7000	12000	18000	*On-chip Clock Rate*
ATE high speed clock [Accuracy + skew (ps)]	12	8	4	*On-chip Clock Rate*
ATE high speed clock jitter (ps peak-to-peak)	4	2	1	*On-chip Clock Rate*
High speed clock burst (number of pulses)	10	10	10	*Sequential Depth*
High speed clock burst maximum frequency (MHz)	7000	12000	18000	*On-chip Clock Rate*
DFT Required for Clocks	Yes	Yes	Yes	*Cost*
Mixed-signal video pin pairs	2	2	2	*SoC*
Mixed-signal RF pin pairs	2	2	2	*SOC*
DFT Required to aid ATE in meeting mixed-signal and/or decrease cost	Yes	Yes	Yes	*Cost*

* *Without high-frequency serial communications*

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

POTENTIAL SOLUTIONS

Major testing problems are appearing in all test areas because of steadily increasing pincounts, frequencies, number of logic gates, and the introduction of analog and memory in SoC devices. ATE manufacturers are struggling to provide equipment to meet these challenges. As mentioned in the beginning of the *Test* chapter, ATE costs are approaching $20M and wafer yields are beginning to fall because tester accuracy cannot be maintained at 5% of the test period as frequencies rise above 1 GHz.

A common theme in most of the testing tables is the increasing need for DFT and BIST to avoid the problems being introduced as ATE technology fails to keep up with shrinking IC feature sizes. In the 1970s, ATE manufactured with bipolar ECL technology were capable of testing at frequencies an order of magnitude higher than the devices under test that were fabricated with 5 μm CMOS technology. In 1999, ATE is struggling to test high pincount devices at 1 Gbit/s, while 180 nm IC off-chip data rates are poised to advance to much higher frequencies.

Potential solutions therefore lie in areas of R&D aimed at developing new DFT and BIST techniques for digital, memory, and analog circuits. Present indications are that these solutions will come from academia rather than from the ATE industry. Previous SIA Test Roadmaps have done a poor job at predicting when BIST will eventually replace traditional full-featured, at-speed test equipment. Therefore, the following Figure 12 attempts to show when it would be desirable for DFT and BIST to move into widespread use.

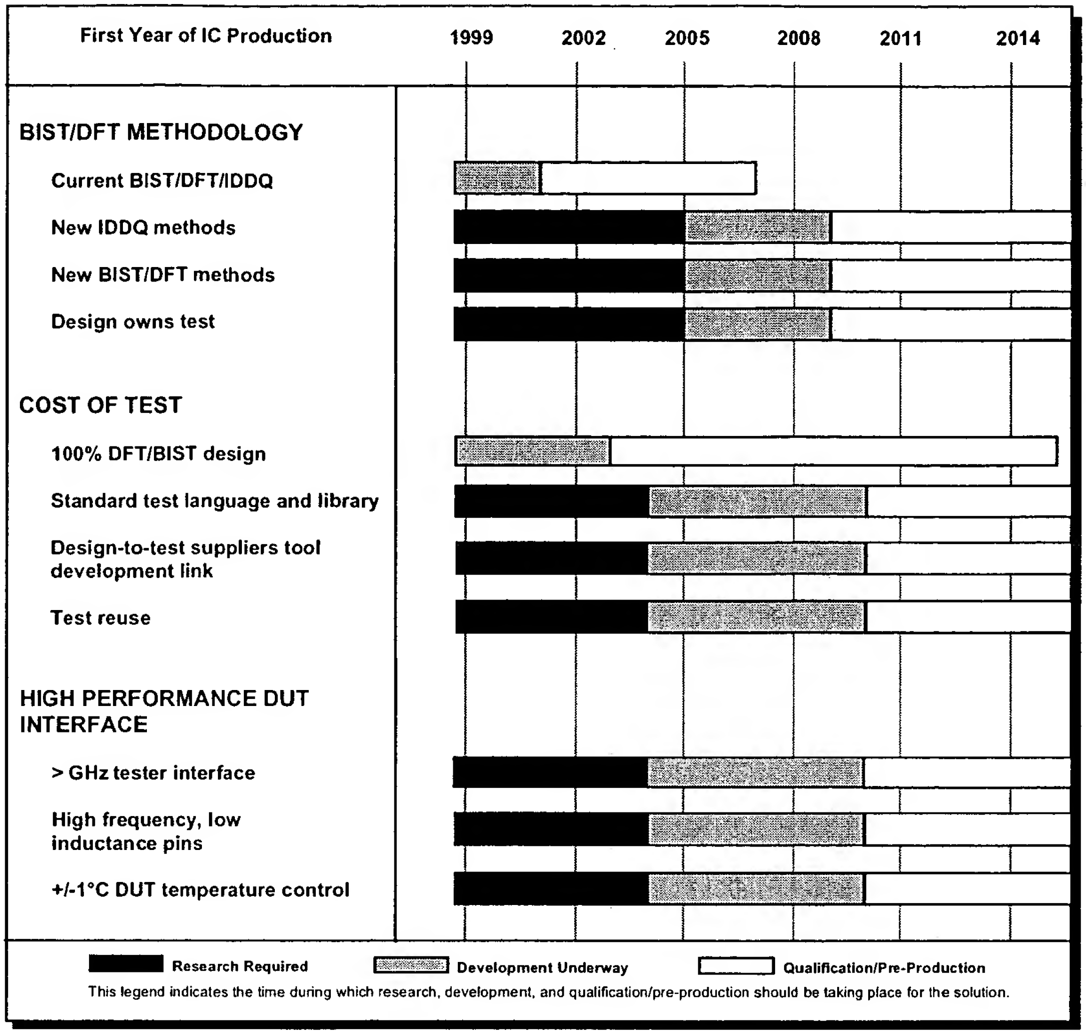

Figure 12 Test Potential Solutions

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS
1999 EDITION

PROCESS INTEGRATION, DEVICES, AND STRUCTURES

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PROCESS INTEGRATION, DEVICES, & STRUCTURES

SCOPE

The *Process Integration, Devices, & Structures (PIDS)* chapter addresses concepts that affect full process flow and reliability tradeoffs associated with new options. Physical and electrical design rules are included within PIDS, and address physical and electrical parameters such as physical dimensions, key active device electrical parameters, passive electrical parameters, and reliability criteria. Nominal targets as well as statistical tolerances are important. This scope has been broken into three subcategories described below. The overarching theme of this chapter is the need to include more embedded functions into the design of an IC, with simultaneous satisfaction of constraints of interconnection, power consumption, reliability, and device performance. This is the fundamental issue associated with a System-on-a-Chip (SoC) application that is the trend for the future devices. SoC issues become a larger crosscut problem that will be dealt with separately as a multidiscipline activity in a separate section.

MEMORY AND LOGIC

Digital memory and logic form the major portion of semiconductor device production. Microprocessors and ASIC devices lead the logic category, while memory encompasses DRAM, SRAM, and nonvolatile memory (NVM). Process integration optimizes the overall architecture of the full process. This includes the silicon active device as well as the on-chip interconnect hierarchies for power, clock, and signal distribution. The architectural tradeoffs between the devices and interconnect structures are driven by performance, density, and reliability requirements. Devices and structures refer to the active transistors, interconnect, and other structures required for logic and memory cell design. Memory cells, DRAM, SRAM and NVM, are applied to both commodity and embedded applications.

ANALOG, MIXED-SIGNAL, AND RADIO FREQUENCY (RF) DEVICES

The commodity driver applications for analog, mixed-signal and RF ICs are projected to remain in personal computing and communications. Analog refers to "pure" analog circuits such as operational amplifiers. Mixed-signal includes integrated circuits containing both digital and analog functions, such as analog-to-digital and digital signal processing circuits. RF refers to pure analog and mixed-signal integrated circuits operating above 800 MHz, such as for wireless communications and "radio on a chip." Certain analog IC technologies such as high voltage and power ICs are not specifically included, while others, such as microelectromechanical systems (MEMS), are included in the out years. Such devices must reuse and leverage the expertise gained from mainstream, digital CMOS technology to remain low-cost, and meet the demands for high performance and reliability.

RELIABILITY

Reliability is a critical aspect of process integration. Emerging technology nodes require the introduction of new materials and processes at a rate that exceeds current capabilities for gathering information and generating the usual database on new failure regimes and defects. Because process integration must be performed without the benefit of extended learning, it will be difficult to maintain current reliability levels. These issues place difficult challenges on testing and wafer level reliability (WLR). Packaging interface reliability is particularly vulnerable because of new materials and processes, form factors, tighter lead and bond spacing, severe environments, adhesion, and customer manufacturing capability issues.

DIFFICULT CHALLENGES

Table 27 Process Integration, Devices, and Structures Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
Meeting device performance targets with available gate stack materials	Production worthy high κ dielectrics and compatible gate materials will not be available.
Function integration at low V_{dd}	Crosstalk, substrate noise, and device performance difficult to optimize simultaneously at high clock rates and low V_{dd}.
Managing power, ground, signal, and clock on multilevel coupled interconnect	Despite the use of low κ dielectrics, interconnect scaling is increasing coupling capacitance, crosstalk and signal integrity issues. Power, clock, and ground distribution will consume an increasing fraction of available interconnect.
Management of increasing reliability risks with the rapid introduction of new technologies.	Inadequate identification and modeling of failure modes in new materials, new operating regions (such as tunneling) and new SoC technologies (such as MEMS)
Integration of precision passive elements	Maintaining high Q, low noise, and tolerances of discrete components.
FIVE DIFFICULT CHALLENGES <100 nm / BEYOND 2005	*SUMMARY OF ISSUES*
Overcoming fundamental scaling limits for current device structures	Switching drive, noise margin, material properties, and reliability will limit performance improvements from scaling
Integration choices for system-on-a-chip	Cost-effective process integration of many functions on a single chip.
Atomic level fluctuations and statistical process variations	Possible reduction of yield and performance below desired levels due to unacceptable statistical variations.
Design for manufacturability, reliability, and performance.	Inadequate smart design tools that incorporate integration challenges in process control, proximity effects, reliability, performance, and others
Low-power, low-voltage, high-performance, and reliable nonvolatile memory element	NVM program and erase require voltages that are incompatible with highly scaled low-voltage devices

DESCRIPTION OF PROCESS INTEGRATION, DEVICES, AND STRUCTURES DIFFICULT CHALLENGES

1. *Meeting device performance targets with available gate stack materials*—High κ gate dielectrics will be required to avoid the excessive tunneling currents of scaled SiO_2 or oxynitrides. Production worthy high κ dielectrics and compatible gate materials will not be available. High conductivity gates with low/no depletion are needed to meet performance requirements.

2. *Function integration at low V_{dd}*—Future systems-on-a-chip (SoCs) will require integration of logic, analog, and memory on the same chip at low-power supply voltages. Each of these technologies faces its own particular problems at low V_{dd}. In logic technology, the challenge is to balance the competing requirements of high-performance and low standby power. Analog circuits will face major problems of headroom and signal-to-noise. Flash memory requires higher programming voltages on-chip. Integration of these technologies will be a major challenge.

3. *Managing power, ground, signal, and clock on multilevel coupled interconnect*—Crosstalk and increased parasitic RC delay are becoming limiting factors in scaled interconnect systems. Incorporating low κ dielectrics will help, but not eliminate these problems. With distribution of power, ground, and clock consuming an increasing fraction of the available interconnect, new interconnect architectures are needed. The interconnect issues are inter-related, and can only be solved by careful integration of new materials, process, architecture, and design tools.
4. *Management of increasing reliability risks with the rapid introduction of new technologies*—Reliability knowledge and capabilities are not keeping pace with the introduction of new materials, new operating regions and SoC, resulting in an increasing risk of problems.
5. *Integration of precision passive elements*—Maintaining high Q passive elements will become increasingly difficult with increasing values of Q and operations at lower voltages.
6. *Overcoming fundamental scaling limits for current device structures*—Switching drive, noise margin, material properties, and reliability will limit performance improvements from scaling. The fundamental limits in the MOS structures are becoming more pronounced due to quantum effects and atomic level effects, causing the increase in performance to be limited.
7. *Integration choices for system-on-a-chip*—The choices of which embedded technologies to include on a chip will be limited by the cost-effectiveness of the embedded technologies for a particular application. The introduction of more complicated additional functions will be more difficult to achieve as the process compatibility and requirements of each embedded feature become more difficult to satisfy simultaneously on a single chip.
8. *Atomic level fluctuations and statistical process variations*—For advanced device structures/architectures, statistical process and dimensional variations will be a more significant barrier to achieving high-performance and yield. While the absolute control of processes and alignment is improving, the percentage variation must not be allowed to increase. Statistical variation of the dopant atoms in the channel region will limit threshold voltage control. To address these issues, novel device structures such as inherently self-aligned or adaptive transistors, or nonlithographically defined structures, will be required.
9. *Design for manufacturability, reliability, and performance*—Increased complexity includes integration of multi-V_t devices, active devices with high gain and stable saturation characteristics, high κ and high quality dielectrics for DRAM and nonvolatile memory, and high quality passive devices (high Q inductors and capacitors).
10. *Low-power, low-voltage, high-performance, and reliable nonvolatile memory element*—The nonvolatile memory element currently requires higher voltages than the scaled technologies allow. New structures or storage techniques will be required to achieve the function of a nonvolatile memory.

TECHNOLOGY REQUIREMENTS

The technology requirements tables reflect the needs of high-performance products (Tables 28–30). Physical gate lengths, gate dielectrics, and junction depths are all being aggressively scaled to meet these requirements. To support the smaller physical gate lengths and to keep the chip dynamic power dissipation within acceptable limits, power supply voltages are also decreasing. It will be a significant challenge to maintain constant drive current as the power supply voltage is reduced. New device structures will be required at some point in the future in order to maintain the projected scaling trends. The off-state leakage current is also increasing to meet the drive current and performance targets. With the higher off-state leakage currents, innovative circuit and system design techniques will be required in order to keep the static power dissipation to an acceptable level. The higher leakage current will also present challenges for defect screening.

The gate dielectric requirements for these transistors quickly reaches a thickness where tunneling currents will be significant and the current SiO_2 based dielectrics can no longer be scaled. Significant effort and focus

must be placed on developing alternate dielectric materials and gate stacks. These will probably be required by the 100 nm technology node in order to extend the scaling limits of current devices.

For the shallow S/D extension junction requirements, the need will depend on the drain engineering that is used. With pocket implants, it is possible to use deeper junctions. Short wire pitch requirements depend on the application. Memory cells will need a short wire pitch that is ~2x the minimum half pitch, whereas logic will require ~3x. The metal system must be optimized to minimize RC delay and meet the electromigration and stress migration requirements. ESD protection coupled with high speed, scaled I/Os present a challenge in device optimization.

Projections for DRAM cell size scaling quickly reach the point where current approaches cannot meet the requirements. This will drive a change in material, cell design, and memory architecture. Data retention and soft error specs will be extremely difficult to achieve in these smaller cells.

Future systems on a chip will require the integration of various logic, memory, analog, and mixed-signal functions at low power supply voltages in order to provide improved system performance. Cost-effective integration of these functions will drive process innovation for future technology. For these highly integrated systems, new testing methodologies will be needed to overcome the testing complexity. Crosstalk and signal integrity problems have been pushed by scaling of the metal system into a regime where technology alone cannot provide the solution. Intelligent design tools will be a requirement.

MEMORY AND LOGIC

Table 28a Memory and Logic Technology Requirements—Near Term

	YEAR *TECHNOLOGY NODE*	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*	*DRIVER*
1	*DRAM ½ Pitch (nm)*	*180*	*165*	*150*	*130*	*120*	*110*	*100*	
2	*MPU Gate Length (nm)*	*140*	*120*	*100*	*85*	*80*	*70*	*65*	
3	*MPU / ASIC ½ (nm)*	*230*	*210*	*180*	*160*	*145*	*130*	*115*	
4	*ASIC Gate Length (nm)*	*180*	*165*	*150*	*130*	*120*	*110*	*100*	
5	Minimum logic V_{dd} (V) (desktop)	1.5–1.8	1.5–1.8	1.2–1.5	1.2–1.5	1.2–1.5	0.9–1.2	0.9–1.2	*M GATE*
6	T_{ox} equivalent (nm)	1.9–2.5	1.9–2.5	1.5–1.9	1.5–1.9	1.5–1.9	1.2–1.5	1.0–1.5	*M GATE*
7	Nominal I_{on} at 25 °C (µA/µm) [NMOS/PMOS] high-performance	750/350	750/350	750/350	750/350	750/350	750/350	750/350	*M GATE*
8	Maximum I_{off} at 25 °C (nA/µm) (For minimum L device) high performance	5	7	8	10	13	16	20	*M GATE*
9	Gate delay metric CV/I (ps) high-performance	11	9.4	8.6	7.3	6.9	6.1	5.7	
10	Percent static power reduction necessary due to innovative circuit/system design	0	33	48	55	71	77	81	*M GATE* *M & A ½*
11	Nominal I_{on} at 25 °C (µA/µm) [NMOS/PMOS] low power	490/230	490/230	490/230	490/230	490/230	490/230	490/230	*A GATE*
12	Maximum I_{off} at 25 °C (pA/µm) (For minimum L device) low power	5	7	8	10	13	16	20	*A GATE*
13	Gate delay metric CV/I (ps) low power	18	16	13	11.2	10.7	8.8	8.2	
14	Percent static power reduction necessary due to innovative circuit/system design	0	36	55	65	80	85	88	*A GATE* *M & A ½*
15	V_T 3σ variation (±mV) (For minimum L device)	50	50	42	42	42	33	33	*M GATE*
16	S/D extension junction depth, nominal (µm)	0.045–0.07	0.04 – 0.065	0.04–0.06	0.03–0.05	0.03–0.048	0.028–0.044	0.025–0.04	*M GATE*

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 28a Memory and Logic Technology Requirements—Near Term (continued)

	YEAR *TECHNOLOGY NODE*	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*	*DRIVER*
1	*DRAM ½ Pitch (nm)*	*180*	*165*	*150*	*130*	*120*	*110*	*100*	
2	*MPU Gate Length (nm)*	*140*	*120*	*100*	*85*	*80*	*70*	*65*	
3	*MPU / ASIC ½ (nm)*	*230*	*210*	*180*	*160*	*145*	*130*	*115*	
4	*ASIC Gate Length (nm)*	*180*	*165*	*150*	*130*	*120*	*110*	*100*	
17	Gate sheet resistance (Ω/sq) at minimum dimension	**4–6**	**4–6**	**4–6**	**4–6**	**4–6**	**4–6**	**4–6**	*M Gate*
18	Interconnect levels	**6–7**	**6–7**	**7**	**7–8**	**8**	**8**	**8–9**	*M & A ½*
19	Short wire pitch (µm)	**0.36–0.46**	**0.33–0.42**	**0.30–0.36**	**0.26–0.32**	**0.24–0.29**	**0.22–0.26**	**0.2–0.23**	*M & A ½*
20	Maximum wire length Lm (µm)	**2243**	**2036**	**1828**	**1621**	**1468**	**1315**	**1162**	*M & A ½*
21	DRAM cell size (µm²)	**0.26**	**0.22**	**0.18**	**0.10**	**0.08**	**0.065**	**0.044**	*D ½*
22	DRAM cell dielectric T_{ox} equivalent (nm)	**3**	**2.40**	**1.80**	**0.95**	**0.80**	**0.65**	**0.45**	
23	Dram retention time (ms)	**250**	**250**	**250**	**250**	**250**	**250**	**250–500**	
24	DRAM soft error rate (fits)	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	
25	Nonvolatile data retention	**10**	**10**	**10**	**10**	**10**	**10**	**10**	
26	NOR cell size (µm²)	**0.34**	**0.29**	**0.24**	**0.17**	**0.15**	**0.13**	**0.1**	*M & A ½*
27	+/- V_{pp}	**8–10**	**8–10**	**8–9.5**	**8–9.5**	**8–9.5**	**7–9**	**7–9**	
28	Tunnel oxide (nm)	**8–10**	**8–10**	**8.5–9.5**	**8.5–9.5**	**8.5–9.5**	**8–9**	**8–9**	
29	NVM endurance (erase/write cycles)	**100K**	**100K**	**100K**	**100K**	**100K**	**100K**	**100K**	
30	ESD protection voltage (V/µm)	**7.5**	**7.5**	**10.5**	**10.5**	**10.5**	**12**	**12**	
31	(V/µm²)	**2.5**	**2.5**	**3.0**	**3.0**	**3.0**	**3.5–4.0**	**3.5–4.0**	

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 28b Memory and Logic Technology Requirements—Long Term

	YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
[1]	*DRAM ½ Pitch (nm)*	70	50	35	
[2]	*MPU Gate Length (nm)*	45	32	22	
[3]	*MPU / ASIC ½ Pitch (nm)*	80	55	40	
[4]	*ASIC Gate Length (nm)*	70	50	35	
[5]	Minimum logic V_{dd} (V) (desktop)	0.6–0.9	0.5–0.6	0.3–0.6	M Gate
[6]	T_{ox} equivalent (nm)	0.8–1.2	0.6–0.8	0.5–0.6	M Gate
[7]	Nominal I_{on} at 25 °C (µA/µm) [NMOS/PMOS] high performance	750/350	750/350	750/350	M Gate
[8]	Maximum I_{off} at 25 °C (nA/µm) (For minimum L device) high-performance	40	80	160	M Gate
[9]	Gate delay metric CV/I (ps) high-performance	3.7	2.6	2.4	
[10]	Percent static power reduction necessary due to innovative circuit/system design	91	97	98	M Gate M & A ½
[11]	Nominal I_{on} at 25 °C (µA/µm) [NMOS/PMOS] low power	490/230	490/230	490/230	A Gate
[12]	Maximum I_{off} at 25 °C (pA/µm) (For minimum L device) low power	40	80	160	A Gate
[13]	Gate delay metric CV/I (ps) low power	5.6	4.5	3.7	
[14]	Percent static power reduction necessary due to innovative circuit/system design	95	98	99	A Gate M & A ½
[15]	V_T 3s variation (±mV) (For minimum L device)	25	17	17	M Gate
[16]	S/D extension junction depth, nominal (µm)	0.02–0.028	0.013–0.02	0.01–0.014	M Gate
[17]	Gate sheet resistance (Ω/sq) at minimum dimension	4–6	4–6	4–6	M Gate
[18]	Interconnect levels	9	9–10	10	M & A ½
[19]	Short wire pitch (µm)	0.14–0.21	0.10–0.15	0.07–0.11	M & A ½
[20]	Maximum wire length Lm (µm)	697	325	201	M & A ½
[21]	DRAM cell size (µm²)	0.018	0.0075	0.0031	D ½
[22]	Cell dielectric T_{ox} equivalent (nm)	0.15	0.06	0.043	
[23]	Minimum refresh time (ms)	250–500	250–500	250–500	
[24]	Soft error rate (fits)	1000	1000	1000	
[25]	Nonvolatile data retention	10	10	0.1–10	
[26]	NOR cell size (µm²)	0.05	0.025	0.012	M & A ½
[27]	+/- V_{pp}	7–8.5	6.5–8.5		
[28]	Tunnel oxide (nm)	7.5–8.5	2–8	2–7	
[29]	NVM endurance (erase/write cycles)	100K	0.1–1M	0.1–10M	
[30]	ESD protection voltage (V/µm)	13.5	15	17.5	
[31]	(V/µm²)	4.5–5.0	5.5–6.0	7.5–10	

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Notes for Table 28a and b Memory and Logic Requirements

General Notes:

[A] *The power supply voltage control is ±10%.*

[B] *Control of L_{gate} is ±10% and ±20% for L_{eff}*

[C] *The total series resistance of the S/D is expected to be <10% of the channel "ON" resistance, $R_{on}=V_{dd}/I_{on}D$. Flash products will not make use of a technology node at the time it is introduced for microprocessor or DRAM usage.*

Explanatory Notes for each row of Table 28a and b:

[1] *From ORTC table*

[2] *From ORTC table*

[3] *From ORTC table*

[4] *From ORTC table*

[5] *Power supply voltage is based on controlling the active power dissipation (see linked spreadsheet) and keeping the field in the gate dielectric at reasonable levels per reliability concerns. Generally, the higher values in the range will be used for high-performance applications, while the lower values in the range will be used for low-power applications.*

[6] *This is the equivalent effective physical SiO_2 thickness. (Note that the electrically determined oxide thickness from C-V measurements would be larger than the thickness in this line because of polysilicon depletion and quantum effects.) Generally, as with V_{dd}, the higher values in the range will be used for high-performance applications, while the lower values in the range will be used for low-power applications. For the 180 through the 110 nm nodes, the range of equivalent T_{ox} is chosen to keep $V_{dd}/T_{ox} \leq 8$ MV/cm because of oxide reliability concerns, where V_{dd}/T_{ox} is a metric for the electric field in the oxide. At the 100 nm technology node, there is a distinct likelihood that high κ materials other than SiO_2 or oxynitride will be used for the gate dielectric. For such materials, the gate leakage current is much smaller than for oxide dielectric with the same equivalent Tox, allowing smaller Tox and hence higher I_{on} for the high κ case. Also, the $V_{dd}/T_{ox} \leq 8$ MV/cm requirement may not hold for the high κ materials, and hence from a reliability point of view, T_{ox} can be scaled further for these materials. Thus, at the 100 nm node, the wide range of 1.0–1.5 nm for equivalent T_{ox} comprehends the uncertainty of what dielectric material will be used, with the high end of the range appropriate for SiO_2 or oxynitride and the very bottom end of the range appropriate for high κ materials. Beyond the 100 node, the use of high κ material for the gate dielectric becomes much more likely, and the $V_{dd}/T_{ox} \leq 8$ MV/cm requirement is no longer followed*

[7] *The device I_{on} value is expected to remain relatively constant for succeeding technology generations.*

[8] *The device I_{off} value is projected to increase with successive technology generations to maintain I_{on} constant per Line 7. I_{off} is measured with $V_s=V_g=V_{substrate}=0$ and $V_d=V_{dd}$. I_{off} is the difference between the drain current and the gate (leakage) current (I_{off} is the sum of the subthreshold current [the current in the source lead] and the junction leakage current [the current in the substrate lead]). The requirements on the gate leakage current are listed in the Front End Processes (FEP) chapter in Table 34.*

[9] *Gate delay metric for high-performance devices is calculated using the simple CV/I ratio and assuming that the channel width scales with the channel length. The MPU gate length is used for the L. The highest value of V_{dd} is used in this analysis along with the thickest gate dielectric.*

[10] *For each technology node, maximum system-imposed limits for total chip leakage current, $I_{L,SYS}$, were estimated by assuming a static power dissipation limit of 10% of the maximum heat-sink limit, and dividing this static power dissipation by V_{dd}. Given the projected device I_{off} value from Line 8, the total projected static leakage current for the chip was calculated based on the total number of transistors and an assumed W/L ratio of 3. This projected chip static leakage current was increased by a factor of 100 to account for the leakage current increase due to device self heating (T=100°C). If this projected T=100°C chip static leakage current value is greater than $I_{L,SYS}$, then the excess percentage of static power dissipation is listed in Line 9. This excess must be eliminated through innovative circuit or system design techniques such as using dynamic or multi-V_t techniques to reduce the effective I_{off} of the chip or by turning off sections of the chip temporarily. System values of the heat-sink dissipation limit, the power-supply voltage, chip size and transistor density were obtained from the ORTC tables.*

[11] *For successive technology generations, the device I_{on} value is expected to remain relatively constant. The low-power device performance is a calculated percentage of the high-performance I_{on} value; this calculated value takes into account the loss in current drive due to the higher required threshold voltage necessary in order to satisfy more stringent I_{off} requirements.*

[12] *The device I_{off} value is set to three orders of magnitude less than the I_{off} for the high-performance chips (Line 8), and is similarly projected to increase with succeeding technology generations. I_{off} is the difference between the drain current and the gate (leakage) current (I_{off} is the sum of the subthreshold current [the current in the source lead] and the junction leakage current [the current in the substrate lead]). The requirements on the gate leakage current are listed in the Front End Processes chapter in Table 34.*

[13] *Gate delay metric for the low-power devices is calculated using the simple CV/I ratio and assuming that the channel width scales with the channel length. The MPU gate length is used for the L. The lowest value of V_{dd} is used in this analysis along with the thinnest gate dielectric.*

[14] *For each technology node, maximum system-imposed limits for total chip leakage current, $I_{L,SYS}$, were estimated by assuming a static power dissipation limit of 10% of the maximum chip power dissipation, and dividing this static power dissipation by V_{dd}. A reasonable value for the maximum dissipation for high density, battery-operated chips is 100 µW, in order to preserve battery life. Given the projected device I_{off} value from Line 11, the total projected static leakage current for the chip was calculated based on the total number of transistors and an assumed W/L ratio of 3. If this projected chip static leakage current value is greater than $I_{L,SYS}$, then the excess percentage of static power dissipation is listed in Line 12. This excess must be eliminated through innovative circuit or system design techniques such as using dynamic or multi-V_t techniques to reduce the effective I_{off} of the chip or by turning off sections of the chip temporarily.*

[15] *The V_t 3-sigma variation was scaled proportionately with the reduction in the midrange power supply voltage.*

[16] *A range of junction depths can be used depending on the drain and channel engineering used (such as pocket implants versus shallow drain extensions).*

[17] *Difficult to obtain gate sheet resistance targets with silicide at 70 nm and beyond.*

[18] *The number of interconnect levels is driven by high-performance microprocessor.*

[19] *The short wire pitch is equal to two times the half pitch.*

[20] *For the metal layers with the smallest pitch, this is the calculated value of the maximum wire length for the propagation delay to be $0.9*f_{max,\ local}$, where $f_{max,\ local}$ is the maximum local frequency from the ORTC tables. The gates are three-input NAND gates, with a Wn/L ratio of 5. (The formula used in calculating the delay as a function of maximum wire length is in P.D. Fisher, et al.[4]) Also refer to the linked spreadsheet.*

[4] P. D. Fisher, et al., "The Test of Time," *IEEE Circuits and Devices Magazine*, vol. 14, pp. 37–44 (March 1998).

[21] *The cell size is driven by the values for DRAM capacity (bits per chip) and chip size, as discussed in more detail in the Front End Processes chapter Table 34b. The capacity and chip size numbers used by FEP are from the Overall Roadmap Technology Characteristics (ORTC) Tables 1a and 1b, and reflect the "generation at introduction" option. (This is for the DRAM chip that is just being introduced and sampled, having the highest DRAM capacity and most aggressive but still quite large chip size. Note that the "Generation at production" option in the ORTC tables has one quarter the DRAM capacity of the generation at introduction option, and correspondingly smaller chip size that allows the chip price to be affordable.) Since the FEP DRAM capacity and chip size numbers are quite aggressive, the cell size must also be scaled very aggressively. The difficulty will lie in reducing the value of the cell size factor, a, where a = cell size/F2 and F is the DRAM half pitch. The required values for a are 8 for the 180 nm node, 6 for the 130 nm node, and 4.4 for the 100 nm node. a = 8 is probably achievable with current techniques, but a =6 will require innovative solutions, as indicated by the yellow coloring of the 130 nm node for this line, while a=4.4 has no known solution, as indicated by the red coloring of the 100 nm node and beyond.*

[22] *Cell dielectric T_{ox} equivalent thickness is driven by the values for DRAM capacity (bits per chip) and chip size, as discussed in more detail in the Front End Processes chapter, Table 34b. The capacity and chip size numbers used by FEP are from the Overall Roadmap Technology Characteristics (ORTC) Tables 1a and 1b, and reflect the "generation at introduction" option. (This is for the DRAM chip that is just being introduced and sampled, having the highest DRAM capacity and most aggressive but still quite large chip size. Note that the "generation at production" option in the ORTC tables has one quarter the DRAM capacity of the Generation at introduction option, and correspondingly smaller chip size that allows the chip price to be affordable.) Since the FEP DRAM capacity and chip size numbers are quite aggressive, the equivalent T_{ox} must also be scaled very aggressively. For the 180 nm–150 nm nodes, the dielectric is based on ONO/Ta_2O_5. For the 130 nm node and beyond, breakthroughs are needed to utilize MIM structures and eventually BST, while for the 70 nm node and beyond, there are no known solutions. The actual T_{ox} equivalent requirement for each node depends on factors such as area enhancement (by height and 3D structures), film leakage, and contact formation. Trench capacitors may have different requirements for the cell dielectric material, but the trends should be valid..*

[23] *Retention time is the minimum time without refreshing a row that the data from memory is still sensed correctly at 85°C. This is the measure of the combined interaction of device leakage, signal strength, and the sense amplifier circuit's sensitivity. This requirement can vary with operating frequency and temperature, and also depending on the application specifics.*

[24] *Soft error: This is a typical FIT rate and can vary with cycle time and other quality/reliability testing conditions.*

[25] *Retention requirements will remain at ten years in the near term, but future alternative technologies will exploit retention-endurance tradeoffs.*

[26] *The need for high electric fields will complicate scaling and eventually force use of alternative NVM technology.*

[27] *The meaning of V_{pp} has become uncertain because it is no longer an external supply. In this table it is intended to indicate the highest voltage relative to ground seen in the cell array.*

[28] *Tunnel oxides must be thin enough to allow ease of program/erase, but thick enough to assure retention. Scaling difficulties will force consideration of alternative cell structures.*

[29] *Endurance of 100K cycles is a minimum need, and in emerging nodes the possibility of higher endurance and lower retention will be explored.*

[30] *ESD V/µm in terms of NMOS capability per micron width. Particularly critical in NMOS ESD circuits and self-protected circuits.*

[31] *ESD V/μm^2 in terms of protection circuit effectiveness per unit area of the protection circuit including guard ring.*

ANALOG, MIXED-SIGNAL, AND RF

Table 29a Analog, Mixed-signal, and RF Technology Requirements—Near Term

[1]	YEAR TECHNOLOGY NODE		1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
	DRAM ½ Pitch (nm)		180	165	150	130	120	110	100	D
	MPU Gate Length (nm)		140	120	100	85	80	70	65	M Gate
	MPU/ASIC ½ Pitch (nm)		230	210	180	160	145	130	115	M & A
	ASIC Gate Length (nm)		180	165	150	130	120	110	100	A Gate
[2]	Minimum Digital Supply Voltage (V)		1.8–1.5		1.5–1.2			1.2–0.9		M Gate
[3]	Minimum Analog Supply Voltage (V)		3.3–2.5	2.5–1.8						
[4]	RF Frequency (GHz)		0.9–2.5	0.9–10						
[5]	Analog Frequency (GHz)		<0.1	0.1–5						
[6]	RF Transistor	Current (μA)	100	100	100	100	75	75	75	M Gate
[7]		f_{max} (GHz)	25	28	32	35	40	45	50	
[8]		f_τ (GHz)	20	20	25	30	30	35	40	
[9]		Noise figure (dB)	1.5	1.5	1.5	1.5	1.2	1.2	1.2	
[10]		1/f Noise (V^2-μm^2)	1×10^{-11}	1×10^{-11}	1×10^{-11}	5×10^{-12}	5×10^{-12}	5×10^{-12}	1×10^{-10}	
[11]	Analog Transistor	Current (μA)	75	70	65	60	55	50	50	
[12]		1/f Noise (V^2-μm^2)	1×10^{-11}	1×10^{-11}	1×10^{-11}	5×10^{-12}	5×10^{-12}	5×10^{-12}	2×10^{-10}	
[13]		Gate oxide leakage (A/cm^2)	1×10^{-12}	1×10^{-12}	1×10^{-12}	1×10^{-10}	1×10^{-10}	1×10^{-10}	1×10^{-10}	
[14]		Current matching (Δ% ±3σ)	≤1	≤1	≤1	≤1	≤1	≤1	≤1	
[15]	RF Coupling Capacitor	Density ($fF/\mu m^2$)	1	1.2	1.4	1.5	1.7	1.9	2	
[16]		Q	≥15	≥18	≥22	≥25	≥27	≥29	≥30	
[17]	Filter Capacitor	Density ($fF/\mu m^2$)	2.5	2.8	3.2	3.5	3.7	3.8	4	
[18]		Matching (Δ% ±3σ)	≤0.1	≤0.1	≤0.1	≤0.1	≤0.1	≤0.1	≤0.1	
[19]	RF Bypass Capacitor	Density ($fF/\mu m^2$)	5	6	7	7.5	8	9	10	
[20]		Linearity (ppm/V)	≤1000	≤1000	≤1000	≤1000	≤1000	≤1000	≤1000	
[21]		Q	≥15	≥18	≥22	≥25	≥27	≥29	≥30	
[22]	Analog Capacitor	Density ($fF/\mu m^2$)	1	1	1	1.5	1.5	1.5	2	
[23]		Linearity (ppm/V)	≤100	≤100	≤100	≤100	≤100	≤100	≤100	
[24]		Leakage ($_pA/_pF$–V)	≤0.001	≤0.001	≤0.001	≤0.001	≤0.001	≤0.001	≤0.001	
[25]		Matching (Δ% ±3σ)	≤0.1	≤0.1	≤0.1	≤0.1	≤0.1	≤0.1	≤0.1	
[26]	RF Resonator	Q	<50	<50	<50	50–1000				
[27]	Analog Resistor	Matching (Δ% ±3σ)	≤1	≤1	≤1	≤0.1	≤0.1	≤0.1	≤0.1	
[28]		1/f Noise (A^2-μm^2)	1×10^{-18}	1×10^{-18}	1×10^{-18}	1×10^{-18}	1×10^{-18}	1×10^{-18}	1×10^{-18}	
[29]		TC (ppm/°C)	≤100	≤100	≤100	≤10	≤10	≤10	≤10	
[30]	Inductor	Q	≥15	≥15	≥25	≥25	≥25	≥25	≥30	
[31]	Signal Isolation	S_{21} (dB)	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-120	
[32]	Benchmark Circuits	Gain (dB)	≥20	≥20	≥20	≥20	≥20	≥20	≥20	
[33]		IIP3 (dBm)	-4	-4	-4	-3	-3	-3	-2.5	
[34]		Noise figure (dB)	1.5	1.5	1.5	1.3	1.3	1.3	1.2	
[35]		Noise (dB)	4	4	4	3.5	3.5	3.5	3	
[36]		Resolution (Bits)	8–14			8–14				

Table 29b Analog, Mixed-signal, and RF Technology Requirements—Long Term

[1]	YEAR / TECHNOLOGY NODE		2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
	DRAM ½ Pitch (nm)		70	50	35	D
	MPU Gate Length (nm)		45	32	22	M Gate
	MPU / ASIC ½ Pitch (nm)		80	55	40	M & A
	ASIC Gate Length (nm)		70	50	35	A Gate
[2]	Minimum Digital Supply Voltage (V)		0.9–0.6	0.6–0.5	0.5–0.3	M Gate
[3]	Minimum Analog Supply Voltage (V)		1.8–1.5		1.5	
[4]	RF Frequency (GHz)		0.9–10	0.9–100		
[5]	Analog Frequency (GHz)		0.1–5	0.1–10		
[6]	RF Transistor	Current (μA)	50	50	50	M Gate
[7]		f_{max} (GHz)	60	150	175	
[8]		f_T (GHz)	50	120	140	
[9]		Noise figure (dB)	≤1	≤1	≤1	
[10]		1/f Noise (V^2-μm^2)	5×10^{-11}	2×10^{-11}	1×10^{-11}	
[11]	Analog Transistor	Current (μA)	40	30	20	
[12]		1/f Noise (V^2-μm^2)	1×10^{-10}	1×10^{-10}	5×10^{-11}	
[13]		Gate oxide leakage (A/cm^2)	1×10^{-08}	1×10^{-08}	1×10^{-05}	
[14]		Current matching (Δ% ±3σ)	≤1	≤1	≤1	
[15]	RF Coupling Capacitor	Density ($fF/\mu m^2$)	3	4	6	
[16]		Q	≥35	≥40	≥40	
[17]	Filter Capacitor	Density ($fF/\mu m^2$)	5	7	10	
[18]		Matching (Δ% ±3σ)	≤0.1	≤0.1	≤0.1	
[19]	RF Bypass Capacitor	Density ($fF/\mu m^2$)	15	20	30	
[20]		Linearity (ppm/V)	≤1000	≤1000	≤1000	
[21]		Q	≥35	≥40	≥40	
[22]	Analog Capacitor	Density ($fF/\mu m^2$)	3	4	6	
[23]		Linearity (ppm/V)	≤100	≤50	≤50	
[24]		Leakage ($_pA/_pF$–V)	≤0.001	≤0.001	≤0.001	
[25]		Matching (Δ% ±3σ)	≤0.1	≤0.1	≤0.1	
[26]	RF Resonator	Q	50–1000		≥1000	
[27]	Analog Resistor	Matching (Δ% ±3σ)	≤0.1	≤0.1	≤0.01	
[28]		1/f noise (A^2-μm^2)	1×10^{-18}	1×10^{-18}	1×10^{-18}	
[29]		TC (ppm/°C)	≤10	≤10	≤1	
[30]	Inductor	Q	≥50	≥75	≥75	
[31]	Signal Isolation	S_{21} (dB)	≤-120	≤-120	≤-120	
[32]	Benchmark Circuits	Gain (dB)	≥20	≥20	≥20	
[33]		IIP3 (dBm)	-1.5	-1	-1	
[34]		Noise figure (dB)	1.0	1.0	1.0	
[35]		Noise (dB)	2.5	2	2	
[36]		Resolution (Bits)	8–14		≥24	

Solutions Exist (white) *Solutions Being Pursued* (shaded) *No Known Solutions* (dark)

Notes for Table 29a and bAnalog, Mixed-signal, and RF Requirements

Explanatory Notes for each row of Tables 29

[1] Year of first digital product for a given technology generation. Lithographic drivers for key technologies at each node are indicated. Year of first analog, RF, and mixed-signal product at the same technology may lag by one generation.

[2] Digital (logic V_{dd}) supply voltage, driven by MPU gate length (M Gate), is repeated here for reference.

[3] Analog supply voltage is expected to lag digital by two or more generations. Additional voltage headroom is needed to avoid excessive power dissipation under reduced signal swing conditions. Analog CMOS designs may use thick gate oxide and low V_t techniques. The analog power supply reduction trend may lag digital backward compatibility trend for I/O such that a common thick gate oxide solution is not feasible.

[4] RF applications will focus on the 0.9–2.5 GHz, 5–6 GHz, 17–20 GHz, 40–45 GHz, and 60–65 GHz frequency spectrums. Design of applications at the lower frequencies will continue throughout the duration of the roadmap (lower frequency bands are not "obsoleted" and will continue to be used). Higher frequency bands will drive performance requirements.

[5] General purpose analog frequency (such as DSP, audio/video, ADC) trend is in parallel with RF. Very clean, jitter-free, clock frequency generation is required. Transistors: It is expected that speed × power characteristics favor use of bipolar for we < 180 nm. MOS speed × power may be favorable relative to bipolar at L_{eff} > 180 nm. Bipolar device assumed through 110 nm (see Potential Solutions Figure 14) followed by MOS device.

[6] Absolute current (independent of device geometry) at which these key RF transistor parameters are measured.

[7] Assumes a "rule of thumb" of approximately 10× the transmit/receive frequency.

[8] Assumes that ft generally follows the progression of f_{max}.

[9] Measured at the specified current (Row 5) and at the application transmit/receive frequency (Row 4).

[10] Bipolar device assumed through 110 nm (see Potential Solutions Figure 14) followed by MOS device. Assume SPICE model for MOS device: $SVG=Kf/(C_{ox}^2 \times W \times L \times f)$. Values scaled assuming t_{ox}^2 relationship. 1/f spectral density is normalized to active device area=1 μm^2, frequency=1Hz. RF MOS device assumed to be realized with the thinnest gate oxide and shortest L_{eff} available at a given node. For this reason, the minimum MPU gate length (M Gate) is indicated as a driver for this device. Although the effects are acute at baseband, 1/f noise can be "mixed up" to RF if present in RF devices. The effect is prominent in MOS devices due to carrier recombination in traps at the insulator-semiconductor interface (surface effect).

[11] Absolute current (independent of device geometry) at which these key analog transistor parameters are measured.

[12] Bipolar device assumed through 110 nm (see Potential Solutions Figure 14) followed by MOS device. Assume SPICE model for MOS device: $SVG=Kf/(C_{ox}^2 \times W \times L \times f)$. Values scaled assuming t_{ox}^2 relationship. 1/f spectral density is normalized to active device area=1 μm^2, frequency=1Hz. Analog MOS device assumed to use the thicker or analog gate oxide available at a given node. The effect is prominent in MOS devices due to carrier recombination in traps at the insulator-semiconductor interface (surface effect). Vertical devices (bipolar) or sub-surface devices (JFETs) are superior in this regard.

[13] Maximum leakage is the same as that for digital CMOS but lagging two generations in gate thickness (see row 3). Analog power supply constrains minimum gate oxide thickness (and therefore leakage). T_{ox}=5 nm (180–150 nm nodes); T_{ox}=4 nm (130–100 nm nodes); T_{ox}=3.5 nm (70–50 nm nodes); T_{ox}=3 nm (35 nm node).

[14] Matching specification assumes "near neighbor" devices at minimum practical separation. Careful layout and photolithographic uniformity are required.

[15] RF coupling capacitors are not expected to drive density. Linearity is not driven by this capacitor.

[16] *Q is the most important parameter for this type of capacitor. Low series R and low parasitics are key.*

[17] *Analog filter implementations will drive density to 7 fF/μm². As digital filter solutions dominate beyond 2003, bypass capacitor applications will drive density. As digital content increases, chip size decreases, and capacitors occupy a larger percentage of a chip. Choice of implementation is driven by complexity/chip size tradeoff (cost). microelectromechanical systems (MEMS) implementation for filter applications may be favorable at density ≥7 fF/μm². Voltage linearity and leakage are not driven by this capacitor.*

[18] *Matching important for this capacitor. Specified at a value of 1 pF.*

[19] *As digital filter solutions dominate beyond 2003, bypass capacitor applications will drive density. High κ dielectrics may be cost-effective as chip size decreases in the 5–15 year timeframe. Density is driven by low frequency requirements and chip size considerations.*

[20] *Voltage linearity not driven by this capacitor.*

[21] *Q is important for this capacitor to provide bypass response at high frequency. Massively parallel, parasitic implementations are expected to dominate for the next five years.*

[22] *Analog capacitors do not drive density.*

[23] *Voltage linearity is driven by switched capacitor applications. Low series R is key.*

[24] *Leakage is driven by feedback capacitor applications where a long time constant is required. Requirement is relaxed with increasing analog clock frequency. Highest quality dielectric is suggested.*

[25] *Matching is key for analog capacitors. Specified at a value of 1 pF.*

[26] *Q is important for this resonator. Low RF parasitic structures such as MEMS polysilicon structures are long-term solutions (see Potential Solutions Figure 14).*

[27] *Matching is important for the analog resistor. Careful layout and photolithographic uniformity are required. Minimum dimensions assumed to be larger than minimum technology dimensions.*

[28] *1/f noise requirement is most important for the analog resistor. It is assumed that low 1/f solutions other than polysilicon coincide with high Q RF resistor solutions.*

[29] *Temperature coefficient is important for the analog resistor. Low TC films or TC canceling techniques may be utilized. 1/f spectral density is normalized to resistor area=1 μm², frequency=1 Hz.*

[30] *Q is most important for the inductor. Low series R implementations such as thick copper is assumed for the next five years. CMOS trend toward increasing substrate doping conflicts with inductor integration. Solutions that mitigate the CMOS conflict and maintain Q are assumed.*

[31] *Signal isolation is best defined as the transmission efficiency (S21 in dB) between a noise source and a noise sensor. Transient sensitivity (in V peak-to-peak) is also an important measure of signal isolation but is not quantified due to its dependence on layout and package. System partitioning, metal interconnect scheme, substrate resistivity, and package design have significant impact on the signal isolation performance. Final result is dependent on application and design tradeoffs.*

[32] *Gain for low-noise amplifier and mixer benchmark circuits*

[33] *IIP3 for low-noise amplifier and mixer benchmark circuits*

[34] *Noise figure for a low-noise amplifier benchmark circuit*

[35] *Noise for a mixer benchmark circuit*

[36] *Resolution for A/D, D/A benchmark circuits required for audio/video applications*

Several trends have been identified for analog, RF and mixed-signal requirements that will lead to higher levels of integration with logic: raw speed of the logic process will enable more signal processing in the digital realm and the implementation of some RF functions; use of dual-gate oxides for higher voltage logic I/O's will support analog requirements for signal headroom; continued focus on 1/f noise, capacitor density and component matching will be required for power and area efficient design.

Modularity of process features will be desirable in order to adapt the technology to specific SoC architectures. Optimization of the logic process to meet analog transistor specifications may add process complexity, but will be required to achieve mixed-signal integration goals. CMOS will continue to be the technology of choice except for applications where Si or SiGe BiCMOS offers a clear performance or area advantage in high-speed circuits.

RELIABILITY

Table 30a Reliability Technology Requirements—Near Term

	YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
Customer Reliability Expectations (at 85° C Junction Temperature)								
[1]	Early failures (ppm) (First 4000 operating hours)	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000
[2]	Long term reliability (5–10 Years) (FITs = failures in 1E9 hours)	10–100	10–100	10–100	10–100	10–100	10–100	10–100
[3]	Soft error rate (FITs)	1000	1000	1000	1000	1000	1000	1000
[4]	Relative failure rate per transistor (normalized to 180 nm)	1	1	1	.62	.62	.62	.34
[5]	Relative failure rate per m of Interconnect (normalized to 180 nm)	1	1	1	.51	.51	.51	.34
[6]	System-on-a-Chip reliability prediction	Logic and Memory			MicroMachine			Micro Optics
[7]	Failure analysis cycle time (days)	1–12	1–12	1–12	1–10	1–10	1–10	1–10

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Note: Reliability requirement includes chip and package failures. Additional parameters (such as temperature cycling and humidity) need to be specified for package reliability.

Table 30b Reliability Technology Requirements—Long Term

	YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
Customer Reliability Expectations (at 85° C Junction Temperature)				
[1]	Early failures (ppm) (First 4000 operating hours)	50–2000	50–2000	50–2000
[2]	Long term reliability (FITs = Failures in 1E9 hours) (5–10 Years)	10–100	10–100	10–100
[3]	Soft error rate (FITs)	1000	1000	1000
[4]	Relative failure rate per transistor (normalized to 180 nm)	.16	.07	.03
[5]	Relative failure rate per m of interconnect (normalized to 180 nm)	.18	.10	
[6]	System-on-a-Chip reliability prediction		Micro Biological	
[7]	Failure analysis cycle time (days)	1–10	1–10	1–10

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Notes for Table 30a and b Reliability Requirements

[1, 2, 3, 5]	*Reliability requirements vary with application. For many mainstream customers it will be sufficient to hold current reliability levels steady during this period of rapid technological change. However, other customers would like reliability levels to improve. Degradation of current reliability levels is not acceptable.*
[1]	*Early failures are generally associated with defects.*
[3, 4]	*Inverse of number of transistors per generation (3) or meters of interconnect per generation (4). For the reliability levels of the chip to remain constant (1,2) the failure rate per transistor or per meter of interconnect must be reduced.*
[6]	*Need to develop the capability to predict the reliability of advanced technologies then will be integrated onto advanced Systems-on-a-Chip. Dates when technologies will be inserted are approximate.*
[7]	*The time to complete the determination of the cause of a yield, field or design failure.*

Chip reliability levels need to be maintained while the technology undergoes massive changes. (Note that this requires significant improvement in the reliability per transistor and the reliability per meter of interconnect.) The environment, life time and reliability levels vary from application to application. Applications that require higher reliability levels, harsher environments and/or longer lifetimes are more difficult than the mainstream office and mobile applications. In addition, as System-on-a-Chip evolves to integrating more and more new technologies (such as MEMS, optoelectronics) on a single chip, there is a need to manage not only the reliability of these new technologies but also any reliability interactions between the various technologies. Defect screening may be required to meet the reliability requirements, especially during the first year of production when yields are ramping up. Defect screening will be required to meet the reliability requirements during the first year of production when yields are at 60%. Finally, failure analysis cycle time improvements are required to support rapid yield learning and design debugging. For more details, see the *SEMATECH Reliability Supplement to the ITRS*, SEMATECH Document #99093824A-TR.[5]

[5] SEMATECH. *Sematech Reliability Supplement to the ITRS*, 99093824A-TR. Austin, TX:SEMATECH, 1999.

POTENTIAL SOLUTIONS

MEMORY AND LOGIC

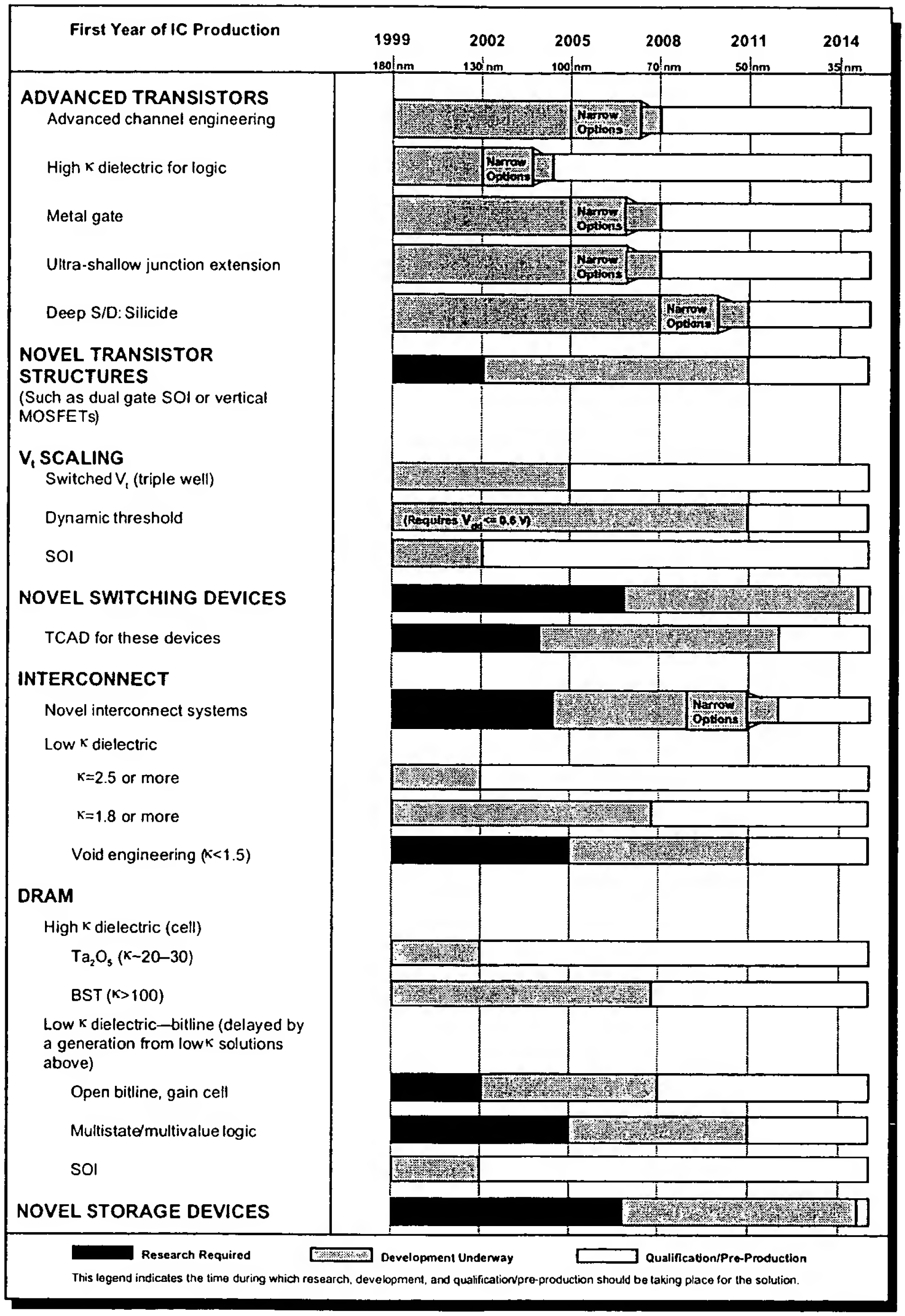

Figure 13 Memory and Logic Potential Solutions

There will be a number of problems in scaling the basic MOSFET structures, particularly for the 100 nm technology node and beyond. The most pressing of these is with the gate stack, the combination of gate dielectric and electrode. The reason for this problem is the thin oxide thickness required for 110 nm and beyond technology generations. For such thin oxides, the gate leakage current due to direct tunneling would become unacceptably large. Use of alternate gate dielectrics with higher relative dielectric constant (κ) than silicon dioxide is the leading projected solution to reduce the gate leakage current to more tolerable levels. However, the time to develop and implement such dielectrics in production is exceedingly short, since the 110 nm node is scheduled for first production by 2004. This is the highest risk problem in the front end. Along with high κ gate dielectrics, dual metal for the gate electrodes is a potential solution to eliminate depletion effects in polysilicon gates and the problem of boron penetration from P^+ polysilicon. Also, metal electrodes sharply reduce the gate resistance and avoid the problem that occurs with silicided polysilicon of increasing sheet resistance for very narrow gates. Ultra-shallow source/drain (S/D) extension junctions will be required, and techniques such as plasma assisted implantation, projection gas immersion laser doping, and ultra-low energy (< 0.5keV) implants are projected solutions for fabricating these junctions. In the deep S/D contact, the requirement of low sheet resistance and contact resistance and shallow junction depth will become increasingly difficult to meet without such innovations as raised S/D or epitaxial Si/Ge. Finally, to maintain the on current and deal with short-channel effects, advanced channel engineering techniques such as highly optimized halo implants and the use of high mobility silicon/germanium epitaxial layers are envisioned. Refer to Figure 13 for the Memory and Logic potential solutions.

Even with innovative scaling solutions as discussed above, it will be quite difficult with technologies at the 100 nm node and beyond to simultaneously meet the requirements for I_{on}, I_{off}, and limited overall chip power dissipation. This is due to the sharp scaling of V_{dd}, while the threshold voltage, V_t, must remain relatively constant to keep I_{off} within tolerable limits. Using multiple V_ts on the chip, or switched V_t through well bias (which requires triple well for bulk CMOS), or dynamic V_t, where the V_t is changed by the gate bias, could alleviate these problems. (Dynamic V_t requires that $V_{dd} \leq 0.6$ V to avoid excessive junction leakage due to forward biasing of the source/substrate junction.) Also, SOI technology, with its high-performance at low V_{dd} and its low parasitic capacitance, could be an important solution. Eventually, for the 50 nm node or beyond, such novel structures as dual gate SOI or vertical MOSFETS may be needed. Even further out, novel switching devices such as quantum dot or single electron transistors, are possible solutions. More accurate, comprehensive, and easy to use TCAD and modeling tools are needed to develop and implement the above-mentioned solutions in a cost-effective, timely manner.

For interconnect, as the technology is scaled and the speed increases, the number of metal levels and the density of the wiring increases and reduction of the parasitic resistance and capacitance becomes critical. Copper is being implemented in current technology by some companies because of its relatively low resistivity and its high lifetime against electromigration. Eventually, copper is expected to replace aluminum as the mainstream metallization for ICs. Low dielectric constant (κ) materials are also being implemented for the interlevel and intralevel dielectric to reduce the capacitance, and it is expected that newer materials with lower κ will be utilized for later technology generations. Eventually, "void" structures such as air gap, void-based materials, etc., may be implemented. It is expected that the combination of copper and low κ dielectrics will suffice for many technology generations. In the long run, however, beyond the 50 nm technology node, highly innovative solutions such as optical interconnect, liquid nitrogen cooled conductors, may be utilized to overcome the inherent speed and power limitations of copper and low κ dielectrics.

For DRAMs, improvements in density, cost, speed, and noise immunity with scaling are critical. As with the gate dielectric, high κ dielectrics are expected to be implemented to increase the capacitance of the storage nodes. Also, similar low κ dielectrics to those in logic IC interconnects will be implemented to lower the

bitline capacitance, but probably delayed by a generation compared to implementation in the high-performance logic ICs. This delay is due mainly to cost considerations versus sensing noise margin. Longer-range solutions include novel array architectures (such as open bitline), gain cells, multi-state and multi-value logic, and the use of SOI. Eventually, novel storage devices such as ferroelectric RAMs (FeRAMs) may be utilized.

Chips of the future are expected to become increasingly complex and high density, and will increasingly mix logic, memory, analog, and others, leading eventually to the system-on-a-chip. To design such chips, much improved CAD and modeling tools will be needed to deal with issues such as signal crosstalk, efficiently using the sheer number of transistors on a chip, effectively applying technological solutions such as switched or dynamic V_t, etc. The need is particularly acute in the interconnect area, where innovative architectures are needed to meet the difficult power, speed, and noise requirements for future technology nodes.

ANALOG, MIXED-SIGNAL, AND RF

Potential solutions for analog are those that are different, or in addition, to those for memory and logic. Successful analog technologies will leverage the base digital platform while integrating value-added features and functions. Key ingredients to successful analog integration are the addition of precision high Q passive elements, adequate signal isolation, and compatible active devices. Refer to Figure 14.

As the speed-power product of CMOS improves, the technology will replace BiCMOS and bipolar implementations. This trend is driven first by increased integration of baseband and IF functions at 180 nm. Integration of RF and IF in CMOS follows. Portable wireless products lead the drive for low power (battery life). Active devices fabricated in SOI will be key in achieving low parasitic capacitance (low current).

The power supply trend for analog design is expected to lag that of digital by two or more generations until 35 nm where it levels off at 1.5 V. A combination of unique gate oxide thickness, multiple threshold, and DC-DC conversion will be utilized to support the analog requirements. Solutions in active threshold regulation and/or design architecture will be required to extend the trend for lower analog supply voltage. Ultimately, full-digital implementations in CMOS will replace most analog designs.

The effect of 1/f noise is more prominent in MOS devices relative to bipolar devices. Low-noise structures such as sub-surface devices (JFET) may be desirable long term solutions.

Matching requirements are severe for analog and exceed those for digital. Precise active and passive device matching will be achieved through fabrication techniques such as optical proximity correction and low D_t processes. Differential circuit design techniques and active compensation will be utilized for matching control.

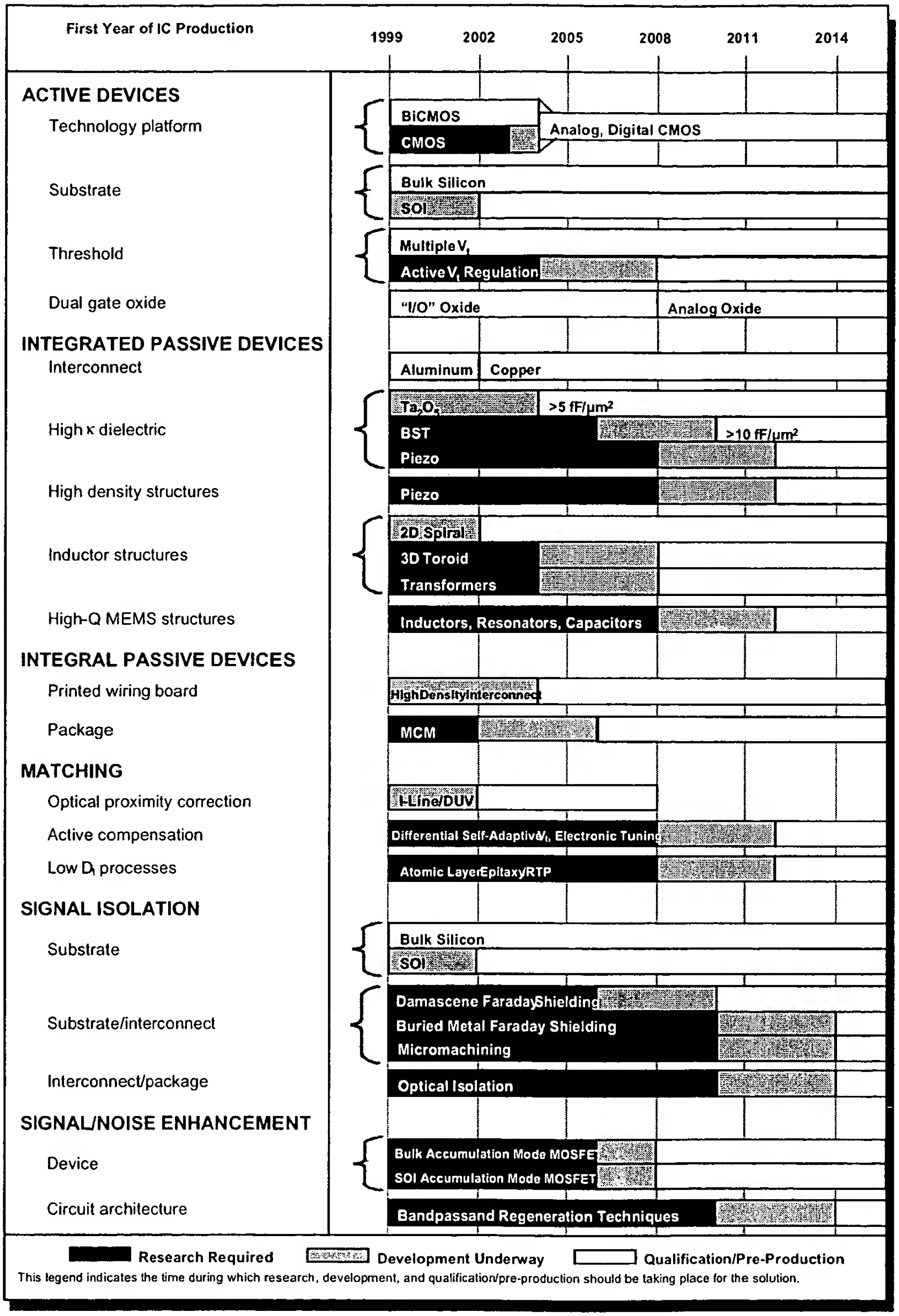

Figure 14 Analog, Mixed-signal, and RF Potential Solutions

The trend of integrating discrete, board-level, passive elements to the chip-level will continue. Solutions for achieving discrete-equivalent precision on-chip will be expected. Very low resistance metal interconnects are required for high Q integrated passives. New high κ dielectrics are needed to reduce integrated capacitor area. Alternatively, some passives may be integrated into the printed wiring board or package as a method of cost reduction/simplification. The need for low-loss, high Q inductors may justify use of 3D or micromachined structures.

Protection of noise sensitive analog circuits from "noisy" digital circuits will become increasingly difficult as the frequency of operation rises. Signal isolation is managed through a combination of substrate, interconnect, and package solutions. Near term, circuit blocks may be protected with oxide isolation and guard rings. Integrated shielding structures are required for protection of circuits and interconnects. Innovative optical and micromachining techniques may be employed as solutions in the future. Novel device structures and design architectures may be employed to enhance circuit signal/noise.

Any cost-effective solution addressing these problems must be compatible with the mainstream CMOS technology of the time

RELIABILITY

The most effective way to meet requirements is to have a complete built-in reliability solution available at the start of the development of each new technology node. This would enable finding the optimum reliability/performance/power choice and would enable designing a manufacturing process that can consistently have high reliability yields. However, to achieve these results requires that many years (historically a decade) before the start of production for a new technology node R&D is conducted on characterizing failure modes, deriving validated, predictive models and developing design for reliability and reliability TCAD tools. Unfortunately, the capability to fully support built-in reliability is not currently available. Under the status quo, the reliability technology base gap will grow. The penalty will be an increasing risk of reliability problems and a reduced ability to push performance, cost and time-to-market.

The Reliability Potential Solutions shown in Figure 15 will not be available when needed. For reliability capabilities to catch up requires a substantial increase in reliability research-development-application and cleverness in acquiring the needed capabilities in much less than the historic decade-like time scales. Work is needed on rapid characterization techniques, validated models and design tools for each failure mechanism. The impact of new materials like Cu, low κ and alternate gate dielectrics need particular attention. Breakthroughs may be needed to develop design for reliability tools that can provide a high fidelity simulation of a large fraction of an IC in a reasonable time. For more details, see the *SEMATECH Reliability Supplement to the ITRS*, SEMATECH Document #99093824A-TR. [5]

Achieving aggressive technology learning curves will require evolutionary and revolutionary advances in failure analysis capabilities. New capabilities are required to handle smaller killer defect sizes, subtle timing defects, and backside analysis (from the back through the silicon for flip chip and dense interconnect). Due to increasing chip complexity, the time to localize faults is growing and is dominating failure analysis time. Automated analysis techniques are required to reduce failure analysis times.

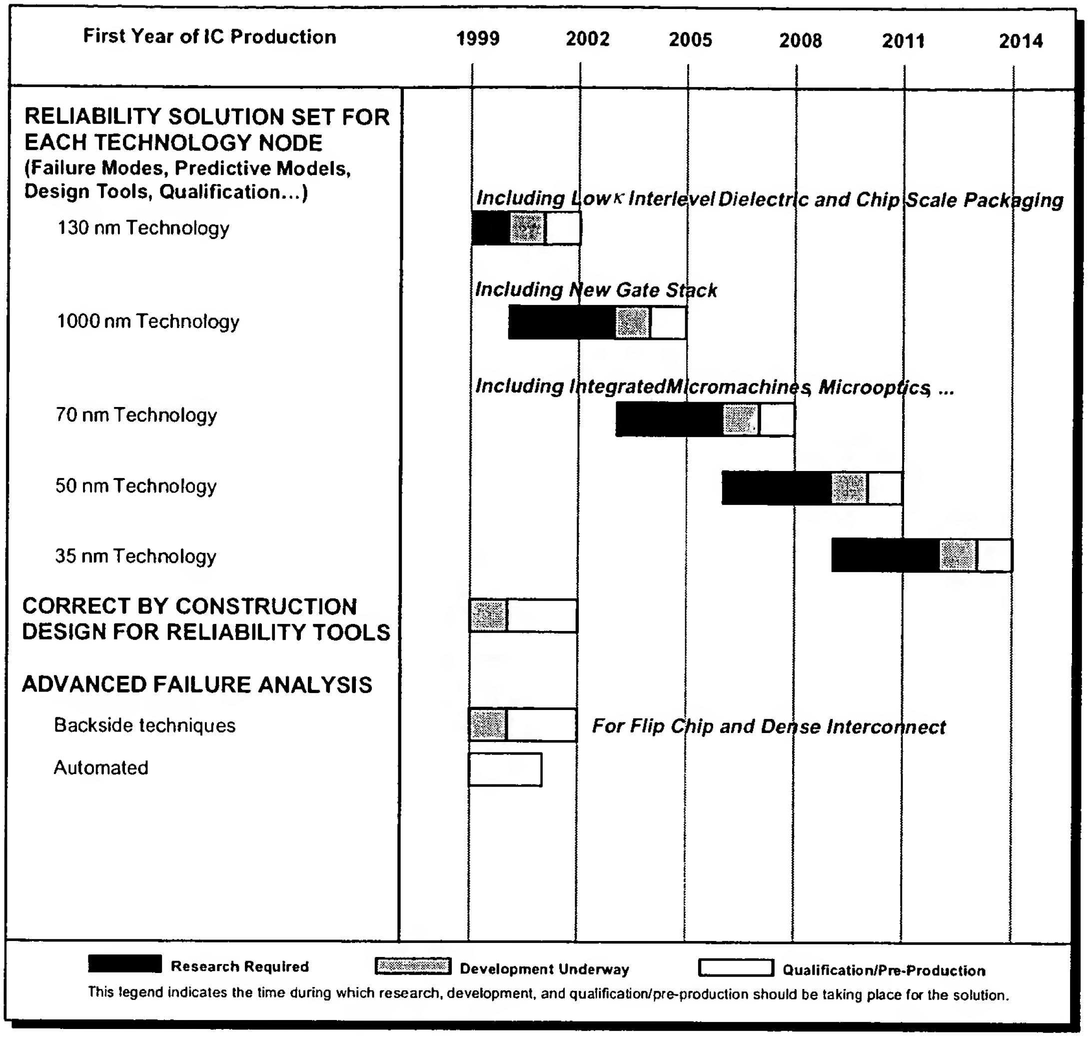

Figure 15 Reliability Potential Solutions

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS
1999 EDITION

FRONT END PROCESSES

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FRONT END PROCESSES

SCOPE

The Front End Processes (FEP) Roadmap was developed with a focus on high performance transistor and DRAM storage capacitor structures appropriate for both memory and logic product types. The intent of this roadmap is to define comprehensive requirements and potential integrated solutions for the key technology areas in the front-end-of-line (FEOL) wafer fabrication processing of integrated circuits. Hence, the Roadmap includes the tools, materials, and processes utilized from the starting silicon wafer through the silicidation process. These specific technology areas are covered: Starting Materials, Surface Preparation, Thermal/Thin Films and Doping, and Front End Plasma Etch.

A presentation of scaling-driven technology requirements and potential solutions is provided for each technology area. The targets and trends shown in the requirements tables are model-based unless otherwise noted. Potential solutions are known examples of possible solutions, however, they are not to be considered the only approaches; innovative, novel solutions are sought.

Related topics for FEP are presented in other sections of the ITRS. The tool-related issues for plasma etch and chemical mechanical polish (CMP) for trench isolation are delineated in the Interconnect chapter rather than in this FEP chapter because of their overlap with back-end-of-line (BEOL) tool issues. The FEP roadmap includes the processing issues as well as future requirements for plasma etch and CMP processing related to FEOL device fabrication. The crosscut needs of FEP are covered in the following sections: Defect Reduction; Metrology; Environment, Safety, & Health; and Modeling & Simulation.

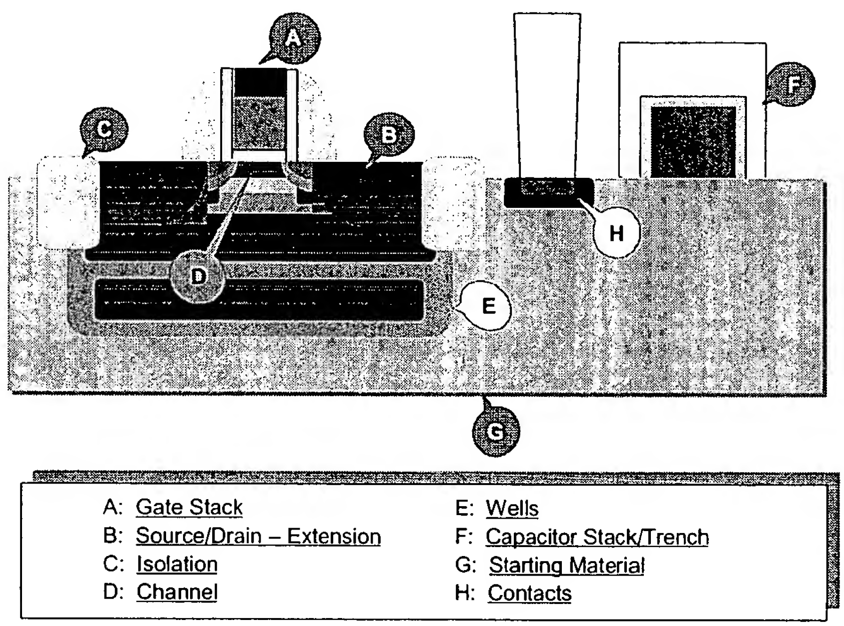

Figure 16 CMOS Transistor, Contact, and DRAM Structure

DIFFICULT CHALLENGES

THE GRAND CHALLENGE—MOVING BEYOND THE SILICON DIOXIDE ERA

Device scaling has been the primary means by which the semiconductor industry has achieved the unprecedented gains in productivity and performance quantified by Moore's Law. These gains have historically been paced by the development of new optical lithography tools, masks and photoresist materials. Now, a *new challenge* has appeared on the horizon that will require considerable resources to overcome, which if not addressed could result in a *showstopper*, to this historical progression. The challenge is the replacement of the traditional silicon dioxide/dual-doped polysilicon gate stack process, which has been the mainstay of CMOS device manufacturing since its inception. The new CMOS gate stack process will require the cost-effective, low temperature integration of nanometer-scale high κ dielectric gate insulators, with dual metal gate electrodes. The anticipated need for the manufacturing deployment of this new process is *no later than five years.* History has shown that changes of this magnitude normally require ten years or more to implement.

At the present time, there is much reason for optimism that this new process can be developed and the research community has responded well to the challenge. As a result, many promising candidate high κ dielectric and metal gate electrode materials have been identified and some preliminary prototype field effect transistors have been produced. However, production deployment requires the comprehension and solution of many difficult challenges that will require extensive resourcing to achieve production readiness. These include

a) the narrowing of dielectric layer choices and selection of final candidate(s);

b) the narrowing of gate electrode material choices and selection of final candidates;

c) the development of the metrology tools to characterize the process;

d) the development of the test equipment and protocols to characterize the electrical and reliability characteristics of the dielectric layer and its interfaces to silicon and gate electrode;

e) the development of the manufacturing equipment with ultra-high levels of ambient control required to reliably, reproducibly, and cost-effectively achieve the atom-by-atom control mandated by the gate dielectric stack and its interfaces with the device silicon on one side and the gate electrodes on the other;

f) the identification, understanding, and elimination of transistor performance and reliability problems that are likely to arise; and

g) the CMOS integration of these disparate materials and unit process into a cost-effective, reliable manufacturing process.

The grand challenge is not the eventual solution to these problems, but the marshalling of the appropriate industry and university resources required to meet the ITRS timeline.

Another consequence of continued device scaling is the difficult challenge associated with the production of abruptly doped ultra-shallow junctions having dopant concentrations in excess of equilibrium limits. New techniques and tools are required to meet this challenge. The integration of these techniques with the aforementioned gate stack poses special difficulties resulting from the anticipated temperature limits imposed by the high κ gate stack process. In addition, the continued scaling of device junctions will probably require that device structures migrate into some type of elevated contact architecture that must also be integrated with the high κ dual metal gate stack.

Towards the end of the current roadmap period, it may be envisaged that the MOSFET structure, as it is currently embodied, will no longer achieve the transistor performance dictated by the ITRS. Therefore, new device structures will be required when traditional CMOS scaling fails. However, these new structures will have the same or more stringent requirements for high κ dielectrics and conducting materials in order to

confine charge and provide current conduction without loss. Inventive new device architectures and concepts are required to address these end-of-roadmap needs.

The use of DRAMs has proliferated because of extraordinary reductions in cost per bit, in part achieved by the ability to scale the size of the DRAM storage cell at a rate that is greater than the square of the DRAM half-pitch dimension. This has resulted in a historical doubling of on-chip bit density every two years. Such aggressive scaling has been accomplished through the utilization of inventive storage cell configurations that make efficient use of chip area. Throughout this period, the storage cell capacitor dielectric has remained silicon oxide or a nitride derivative. However, further aggressive scaling will require that the limited dielectric constant afforded by these materials has resulted in the need to replace these dielectrics with a material of much higher dielectric constant. Changes in capacitor electrodes will also be required to effect this change. It is unlikely that the high κ and electrode materials chosen for this application will be the same as those chosen for the MOSFET gate dielectric because, aside from the common need for high dielectric constant, the other requirements are different. As a result, it is likely that a new fabrication process for either the present stack or trench capacitor structures will be required. *This new fabrication process poses problems of equivalent complexity and scope as those associated with the future CMOS gate stack*, and the timeline for manufacturing deployment are very similar. Therefore, it is anticipated that industry resources of equivalent scope will be required to address this conversion.

The nature of these challenges are detailed in Table 31 as well as in the text, tables, and figures in the following portions of this chapter.

Table 31 Front End Process Difficult Challenges

BEFORE 2005, LOGIC GATE LENGTH > 65 nm	*ISSUES*
Nitride Derivatives and High κ Gate Stacks	Effective oxide thickness ~/>1.2 nm for nitride derivatives, ~/< 1.2 nm for high κ Achieve optimal channel mobility >95% of SiO_2 Minimize gate leakage mechanisms to achieve ~/<1A/cm^2 for high-performance logic and ~/<0.001 A/cm^2 for system LSI Control Boron penetration. Minimize gate electrode depletion, e.g., polysilicon depletion Chemical compatibility of dual metal with appropriate work functions
DRAM Storage Cells (Stack and Trench Capacitors)	Implementation of Ta_2O_5, BST, etc., with associated compatible electrode materials Capacitor structures that meet (DRAM ½ Pitch)^2 scaling Trench and stack capacitor scaling to <100 nm
Ultra-Shallow Junctions (USJ) with Standard Processing	Achievement of lateral and depth abruptness Achievement of low series resistance, <10% of channel R_s Annealing technology to achieve ~/<300Ω/□ at ~/<30 nm X_j
L_{eff} Control	Etch CD control and selectivity Sidewall etch control Microloading effects of dense/isolated lines Halo/pocket implant optimization Overall thermal cycle control
Metrology	Physical, electrical and chemical measurement and characterization of gate dielectric, electrodes, USJ, etc.

Table 31 Front End Process Difficult Challenges (continued)

2005 AND AFTER, LOGIC GATE LENGTH ≤ 65 nm	*ISSUES*
Ultra High κ Gate Stack	Effective oxide thickness <0.9 nm Chemical compatibility of dual metal with appropriate work functions Acceptable channel mobility Thermal budget and dielectric stability CD Control Gate Leakage ~/<1A/cm^2 for high performance logic, ~/<0.001 A/cm^2 for system LSI Cost-effective CMOS integration
Memory Storage Cell	Will an alternate storage cell supplant conventional memory? Ultra high κ capacitor dielectric (Epi BST) Are trench and stack capacitor structures viable at or below 70 nm while meeting (DRAM ½ Pitch)^2 scaling?
Alternate and Ultra-scaled Transistor Structures	CMOS structure: raised S/D, replacement gate process flow, CD control, CMOS integration, and others New device structures beyond planar CMOS: pillar, wraparound gate, and others.
Integration of Silicon Compatible Materials	CoO of large wafers (>300 mm): epi, SOI, Si:Ge Development of compatible high κ dielectric materials Development of compatible dual metal electrodes Development of material compatible cleaning processes
Metrology	Physical, chemical and electrical measurement and characterization of new dielectric, electrodes, and ultra-shallow, ultra-abrupt, dopant distributions

TECHNOLOGY REQUIREMENTS AND POTENTIAL SOLUTIONS

STARTING MATERIALS

The selection of starting materials at present generally involves choosing either Czochralski (Cz) polished or epitaxial silicon wafers. For 130 nm and smaller geometries, silicon-on-insulator (SOI) materials appear to be poised to become more than a niche technology. Other starting material alternatives include hydrogen heat-treated polished wafers to improve near-surface characteristics and the growth of specially prepared low grown-in defect crystals. Memory circuits are commonly manufactured on lower cost Cz polished wafers, while logic ICs are generally manufactured on higher cost epitaxial wafers because of their greater robustness (e.g., gate dielectric integrity) during IC fabrication and latch-up suppression capability, although the latter may not be as critical with the implementation of shallow trench isolation (STI). The reduction of the epitaxial-to-polished wafer price ratio favors continued use of epitaxial wafers for logic applications. The wide variety of potential starting materials, including SOI, is likely to continue into the foreseeable future and is addressed in the potential solutions in Figure 17.

Tables 32a and 32b lists target values of critical characteristics of wafers immediately after removal from the shipping box. These characteristics include general wafer properties plus specific parameters appropriate to polished, epitaxial, and SOI wafers. The values have been selected to ensure that each parameter contributes no more than 1% to the chip yield loss. The values in the table are derived from model-based analysis, taking into account critical dimension (CD), number of bits or transistors per chip, wafer size, for example. These values are only as reliable as the underlying models, which are far from complete.

Parameter values determined in this way do not take into account the distribution of parameter values resulting from manufacturing variations. Two distributions are commonly found in wafer technology. Parameters distributed symmetrically around a central (mean) value (such as thickness) can be described by

the familiar normal distribution. Zero-bounded parameters (such as flatness, particle density, and surface metal concentrations) can usually be approximated by a log-normal distribution, in which the logarithms of the parameter values are normally distributed. The latter distribution is highly asymmetric with long tails at the upper end of the distribution.

Table 32a Starting Materials Technology Requirements—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	Driver
DRAM ½ PITCH (nm)	180	165	150	130	120	110	100	D ½
MPU GATE LENGTH (nm)	140	120	100	85	80	70	65	M
*General Characteristics * [A,B]*								
Wafer diameter (mm) **	200	300 ***	300	300	300	300	300	M
Edge exclusion (mm)	2	1	1	1	1	1	1	D ½, M
Front surface particle size (nm), latex sphere equivalent [C]	≥ 90	≥ 82.5	≥ 75	≥ 65	≥ 60	≥ 55	≥ 50	D ½
Particles (cm^{-2}) [D]	≤ 0.13	≤ 0.12	≤ 0.12	≤ 0.14	≤ 0.13	≤ 0.12	≤ 0.10	D ½
Particles (#/wf)	≤ 38	≤ 84	≤ 80	≤ 95	≤ 89	≤ 84	≤ 72	D ½
Critical surface metals (at/cm^2) [E]	≤ 1.8×10^{10}	≤ 1.4×10^{10}	≤ 1.2×10^{10}	≤ 8.8×10^{9}	≤ 6.8×10^{9}	≤ 5.8×10^{9}	≤ 4.9×10^{9}	D ½, M
Site flatness (nm) [F]	≤ 180	≤ 165	≤ 150	≤ 130	≤ 120	≤ 110	≤ 100	D ½
Oxygen (center point value ± 2.0 ppma) (ASTM '79) [G]	19–31	18–31	18–31	18–31	18–31	18–31	18–31	D ½, M
*Polished Wafer **								
Total Allowable Front Surface Light Scattering Defect Density is The Sum of Crystal Originated Pits (COPs) and Particles (see General Characteristics)								
Front surface COPs size (nm), latex sphere equivalent [C]	≥ 90	≥ 82.5	≥ 75	≥ 65	≥ 60	≥ 55	≥ 50	D ½
COPs (cm^{-2}) [H]	≤ 0.13	≤ 0.12	≤ 0.12	≤ 0.14	≤ 0.13	≤ 0.12	≤ 0.10	D ½
COPs (#/wf)	≤ 38	≤ 84	≤ 80	≤ 95	≤ 89	≤ 84	≤ 72	D ½
Back surface particle size (DRAM), latex sphere equivalent (nm) [I]	≥ 667	≥ 617	≥ 567	≥ 500	≥ 467	≥ 433	≥ 400	D ½
Particles (DRAM) (#/cm^2) [J]	≤ 0.63	≤ 0.61	≤ 0.58	≤ 0.55	≤ 0.53	≤ 0.50	≤ 0.48	D ½
Particles (DRAM) (#/wf)	≤ 191	≤ 423	≤ 403	≤ 384	≤ 367	≤ 352	≤ 336	D ½
Total bulk Fe (at/cm^3) [K]	≤ 1×10^{10}	< 1×10^{10}	< 1×10^{10}	< 1×10^{10}	< 1×10^{10}	< 1×10^{10}	< 1×10^{10}	D ½, M
Oxidation stacking faults (OSF) (DRAM) (cm^{-2}) [L]	≤ 4.4	≤ 3.9	≤ 3.4	≤ 2.8	≤ 2.5	≤ 2.2	≤ 1.9	D ½
Oxidation stacking faults (OSF) (MPU) (cm^{-2}) [L]	≤ 3.1	≤ 2.5	≤ 1.9	≤ 1.5	≤ 1.4	≤ 1.1	≤ 1.0	M
Recombination lifetime (µs) [M], see also [N]	≥ 305	≥ 350	≥ 350	≥ 350	≥ 350	≥ 350	≥ 350	D ½

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 32a Starting Materials Technology Requirements—Near Term (continued)

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	Driver
DRAM ½ PITCH (nm)	180	165	150	130	120	110	100	D ½
MPU GATE LENGTH (nm)	140	120	100	85	80	70	65	M
Epitaxial Wafer *								
Total Allowable Front Surface Defect Density is The Sum of Epitaxial Large Area Defects, Epitaxial Stacking Faults and Particles (see General Characteristics) [O]								
Minimum layer thickness (DRAM) (μm) (± % tolerance) [P]	3–4 (±4%)	3–4 (±4%)	3–4 (±4%)	2–3 (±4%)	2–3 (±4%)	2–3 (±4%)	2–3 (± 3%)	D ½
Minimum layer thickness (MPU) (μm) (± % tolerance) [P]	1.5–2 (±4%)	1.5–2 (±4%)	1.5–2 (±4%)	1.5–2 (±4%)	1.5–2 (±4%)	1.5–2 (±4%)	1–1.5 (± 3%)	M
Layer large area defects (DRAM) (cm^{-2}) [Q]	≤ 0.008	≤ 0.007	≤ 0.007	≤ 0.007	≤ 0.006	≤ 0.006	≤ 0.006	D ½
Layer large area defects (MPU) (cm^{-2}) [Q]	≤ 0.006	≤ 0.006	≤ 0.006	≤ 0.006	≤ 0.006	≤ 0.006	≤ 0.006	M
Layer stacking faults (DRAM) (cm^{-2}) [R]	≤ 0.015	≤ 0.015	≤ 0.014	≤ 0.013	≤ 0.013	≤ 0.012	≤ 0.012	D ½
Layer stacking faults (MPU) (cm^{-2}) [R]	≤ 0.012	≤ 0.012	≤ 0.012	≤ 0.012	≤ 0.012	≤ 0.012	≤ 0.012	M
Silicon-On-Insulator Wafer *								
Silicon final device layer thickness (tolerance ± 5%) (nm) [S]	30–200	30–200	30–200	30–200	30–200	20–100	20–100	M
Buried oxide (BOX) thickness (tolerance ± 5%) (nm) [T]	≤ 200	≤ 200	≤ 200	≤ 200	≤ 200	≤ 100	≤ 100	M
D_{BOX}, BOX defects (DRAM) (cm^{-2}) [U]	≤ 0.106	≤ 0.100	≤ 0.096	≤ 0.091	≤ 0.085	≤ 0.080	≤ 0.069	D ½
D_{BOX}, BOX defects (MPU) (cm^{-2}) [U]	≤ 0.359	≤ 0.346	≤ 0.352	≤ 0.344	≤ 0.275	≤ 0.254	≤ 0.208	M
D_{INC}, inclusions (DRAM) (cm^{-2}) [V]	≤ 0.127	≤ 0.120	≤ 0.115	≤ 0.109	≤ 0.102	≤ 0.096	≤ 0.082	D ½
D_{INC}, inclusions (MPU) (cm^{-2}) [V]	≤ 0.431	≤ 0.415	≤ 0.422	≤ 0.413	≤ 0.330	≤ 0.305	≤ 0.250	M
D_{TD}, threading dislocations (DRAM,MPU) (cm^{-2}) [W]	≤ 2×10^6	≤ 2×10^6	≤ 2×10^6	≤ 2×10^6	≤ 2×10^6	≤ 2×10^6	≤ 2×10^6	D ½, M

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

* *Parameters define limit values; independent predictors of yield, mathematically or empirically modeled at 99% limit values rarely coincide for more than one parameter. A given wafer will generally not exhibit more than one limit value "at a time;" other parameter values most likely near median value, thereby ensuring total yield for all parameters is at least 99%.*

** *Significant gaps in metrology and wafer manufacturing equipment need to be closed on 200 mm, especially for the 180 nm and 130 nm nodes, inasmuch as 300 mm is being delayed and 200 mm will still be prevalent at the 130 nm node.*

*** *Numerical values are for 300 mm, although 200 mm will be the dominant wafer diameter.*

Table 32b Starting Materials Technology Requirements—Long Term

YEAR / TECHNOLOGY NODE	2008 / 70 nm	2011 / 50 nm	2014 / 35 nm	DRIVER
DRAM ½ PITCH (nm)	70	50	35	D ½
MPU GATE LENGTH (nm)	45	32	22	M
*General Characteristics * [A,B]*				
Wafer diameter (mm)	300	300	450	M
Edge exclusion (mm)	1	1	1	D ½, M
Front surface particle size (nm), latex sphere equivalent [C]	≥ 35	≥ 25	≥ 17.5	D ½
Particles (cm^{-2}) [D]	≤ 0.10	≤ 0.10	≤ 0.10	D ½
Particles (#/wf)	≤ 73	≤ 72	≤ 165	D ½
Critical surface metals (at/cm^2) [E]	$\leq 4.2\times10^9$	$\leq 3.6\times10^9$	$\leq 3.4\times10^9$	D ½, M
Site flatness (nm) [F]	≤ 70	≤ 50	≤ 35	D ½
Oxygen (center point value ± 2.0 ppma) (ASTM '79) [G]	18–31	18–31	18–31	D ½, M
*Polished Wafer **				
Total Allowable Front Surface Light Scattering Defect Density is The Sum of Crystal Originated Pits (COPs) and Particles (see General Characteristics)				
Front surface COPs size (nm), latex sphere equivalent [C]	≥ 35	≥ 25	≥ 18	D ½
COPs (cm^{-2}) [H]	≤ 0.10	≤ 0.10	≤ 0.10	D ½
COPs (#/wf)	≤ 73	≤ 72	≤ 165	D ½
Back surface particle size (DRAM), latex sphere equivalent (nm) [I]	≥ 300	≥ 233	≥ 184	D ½
Particles (DRAM) ($\#/cm^2$) [J]	≤ 0.42	≤ 0.37	≤ 0.32	D ½
Particles (DRAM) (#/wf)	≤ 294	≤ 255	≤ 504	D ½
Total bulk Fe (at/cm^3) [K]	$< 1\times10^{10}$	$< 1\times10^{10}$	$< 1\times10^{10}$	D ½
Oxidation stacking faults (OSF) (DRAM) (cm^{-2}) [L]	≤ 1.1	≤ 0.7	≤ 0.4	D ½
Oxidation stacking faults (OSF) (MPU) (cm^{-2}) [L]	≤ 0.6	≤ 0.4	≤ 0.2	M
Recombination lifetime (μs) [M] [N]	≥ 350	≥ 350	≥ 400	D ½
*Epitaxial Wafer **				
Total Allowable Front Surface Defect Density is the Sum of Epitaxial Large Area Defects, Epitaxial Stacking Faults and Particles (see General Characteristics) [O]				
Minimum layer thickness (DRAM) (μm) (± % tolerance) [P]	2–3 (±3%)	2–3 (±3%)	2–3 (±3%)	D ½
Minimum layer thickness (MPU) (μm) (± % tolerance) [P]	1–1.5 (±3%)	1–1.5 (±3%)	1–1.5 (±3%)	M
Layer large area defects (DRAM)(cm^{-2}) [Q]	≤ 0.005	≤ 0.004	≤ 0.004	D ½
Layer large area defects (MPU)(cm^{-2}) [Q]	≤ 0.006	≤ 0.006	≤ 0.006	M
Layer stacking faults (DRAM) (cm^{-2}) [R]	≤ 0.010	≤ 0.009	≤ 0.008	D ½
Layer stacking faults (MPU) (cm^{-2}) [R]	≤ 0.012	≤ 0.012	≤ 0.012	M

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 32b Starting Materials Technology Requirements—Long Term (continued)

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
DRAM ½ PITCH (nm)	70	50	35	D ½
MPU GATE LENGTH (nm)	45	32	22	M
*Silicon-On-Insulator Wafer**				
Silicon final device layer thickness (tolerance ± 5%) (nm) [S]	20–100	20–100	20–100	M
Buried oxide (BOX) thickness (tolerance ± 5%) (nm) [T]	≤ 70	≤ 50	≤ 50	M
D_{BOX}, BOX defects (DRAM) (cm^{-2}) [U]	≤ 0.061	≤ 0.060	≤ 0.052	D ½
D_{BOX}, BOX defects (MPU) (cm^{-2}) [U]	≤ 0.154	≤ 0.107	≤ 0.080	M
D_{INC}, inclusions (DRAM) (cm^{-2}) [V]	≤ 0.073	≤ 0.072	≤ 0.063	D ½
D_{INC}, inclusions (MPU) (cm^{-2}) [V]	≤ 0.184	≤ 0.129	≤ 0.096	M
D_{TD}, threading dislocations (DRAM,MPU) (cm^{-2}) [W]	≤ 2×10^6	≤ 2×10^6	≤ 2×10^6	D ½, M

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

** Parameters define limit values; independent predictors of yield, mathematically or empirically modeled at 99%. limit values rarely coincide for more than one parameter. A given wafer will generally not exhibit more than one limit value "at a time;" other parameter values most likely near median value, thereby ensuring total yield for all parameters is at least 99%.*

Notes for Table 32a and b Starting Materials Requirements

[A] Organics/polymers modeled approximately 0.1 of a monolayer, ≤ 1×10^{14} C at/cm^2.

[B] Front-surface microroughness ≤ 0.10 nm (RMS) for all CD generations; instrumentation choice, target values, and spatial frequency range (scan size) are selected based on application. Power spectral density analysis is recommended to utilize full accessible range of instruments.

[C] Front surface particle or crystal originated pit (COP) size = $K_1(CD)$; $K_1 = 0.5$.

[D] Front-surface particles modeled for 99% yield by $Y = \exp[-D_P R_P T A (CD)^2]$ [6], $R_P = 0.2$, T = # of transistors or bits/chip per technology generation, and A is the DRAM cell area factor, a function of the technology generation. Assuming a pre-gate cleaning efficiency of 50% for particles in Surface Preparation, the particle values are accordingly increased by a factor 2. This results in a number twice that listed in the Surface Preparation values in Table 33. The analogous A value for MPUs is not available, so the MPU particles are taken equal to the DRAM values.

[E] Metals empirically modeled for 99% yield by $Y = \exp[-D_M R_M T A (CD)^2]$ [6], $R_M = 0.2$, T = # of transistors or bits/chip per technology generation and A is the DRAM cell area factor, a function of the technology generation, with $D_M = K_2 (M)^3 \exp[-To/0.7]$, $K_2 = 1.854 \times 10^{29}$ cm^4, To equivalent oxide thickness (corrected for quantum mechanical and poly depletion effects), in nm per technology generation (based on MIS DRAM device structure.) The experimental data resulting in this model is based on and extends the precursor publication. [7] Assuming a pre-gate cleaning efficiency of 50% for metals in Surface Preparation, the metal values are accordingly increased by a factor 2. This results in a number twice that listed in the Surface

[6] W. Maly, H.T. Heineken, and F. Agricola, "A Simple New Yield Mode," *Semiconductor International*, number 7, 1994, pages 148–154.

[7] W.B. Henley, L. Jastrzebski and N.F. Haddad, "The Effects of Iron Contamination on Thin Oxide Breakdown-Experimental and Modeling," *MRS 262*, (1992) pages 993–998.

Preparation values in Table 33. The value listed is the limit for each of the following metals: Ca, Co, Cu, Cr, Fe, K, Mo, Mn, Na, and Ni.

[F] *The metric for site flatness should be matched to the type of exposure equipment used in leading edge applications. For the 180 nm technology node, full-field steppers with square fields (nominally 22 × 22 mm) will be utilized and SFQR is the appropriate metric. For the 130 nm technology node to the end of optical lithography, scanners will be utilized with rectangular fields (nominally 25 mm × 32 mm) and SFSR is the appropriate metric. In either case, the metric value is approximately equal to the CD for dense lines (DRAM half pitch). Partial sites should be included. Note that flatness metrology requires sufficient spatial resolution to capture topological features relevant for each technology node. Warp should be less than 50 µm for all technology generations.*

[G] *Range of center-point value based on IC requirements. ± tolerance is minimum-maximum range about center-point value. Bulk Micro Defects (BMD) for internally gettered or no internally gettered polished wafer > $1 \times 10^8/cm^3$ or < $1 \times 10^7/cm^3$, respectively, after IC processing. The IOC '88 oxygen concentration value is obtained by multiplying the ASTM value by 0.65.*

[H] *COPs modeled for 99% yield by $Y = \exp[-D_C R_C T A (CD)^2]$ [6], $R_C = 0.1$, T = # of transistors or bits/chip per technology generation and A is the DRAM cell area factor, a function of the technology generation. The analogous A value for MPUs is not available, so the MPU COPs are taken equal to the DRAM values.*

[I] *The front-surface height elevation, H, due to a back-surface particle of size, D, under a back-surface film of thickness, T, and a wafer thickness, W, may be expressed as $[(xD + xT + W) - (T + W)]$, which may be reduced to $[(xD) - (1-x)T]$, where x = 0.6 is the compression of the particle and back-surface film due to the pressure of the chuck on the wafer. Assuming a front-surface elevation of 2(CD) results in a 100% lithographic printing failure, the back-surface particle size is expressed as:*
$D = [(2/0.6)(CD) + (0.4/0.6)(T)]$, where CD and T are expressed in nm. In this table, T is set equal to 100 nm.

[J] *Back-surface particles modeled for 99% yield by $Y = \exp[-D_P R_P A_{EFF}]$ (1), $R_P = 1.0$ and $A_{EFF} = A_{CHIP} \times 0.03 \times 0.8$, where 0.03 corresponds to only 3% of the chip area touches the chuck and 0.8 corresponds to only 80% of the effective chip area is degraded by effects of the back-surface particle on the front-surface de-focus effect. Assuming a pre-gate cleaning efficiency of 50% for particles in Surface Preparation, the particle values are accordingly increased by a factor 2.*

[K] *Fe consistent with τ_r (see [M]); other bulk metals also important. Bulk Fe concentration (at/cm³) cannot be converted to surface concentration (at/cm²) via wafer thickness.*

[L] *OSF density empirically modeled by $K_3 (CD)^{1.42}$; CD in nm; $K_3 = 2.75 \times 10^{-3}$, [8] test at 1100°C, 1 hour steam, strip oxide/etch; n-type material more difficult to control OSF.*

[M] *Recombination lifetime, $\tau_r \geq 2(L^2)/D_n$, where L = minority-carrier diffusion length and D_n = minority-carrier diffusion coefficient at 27°C) [9]. The diffusion length is taken equal to the wafer thickness and a safety factor of 2 is used. Appropriate technique(s) to control, stabilize and passivate surface effects required, depending on the technique (such as SPV, PCD) No oxygen precipitation in sample and resistivity of 5–20 Ω-cm recommended.*

[N] *Generation lifetime, $\tau_g = n_i/G$, [10] where n_i = intrinsic concentration [11,12] and G is the generation rate per unit volume and per unit time $\tau_g = (n_i q W)(I_{limit}/A_{CR})^{-1} \geq 50\ \mu s$ ensures DRAM junction leakage current $I_{limit} \leq 10^{-16}$ A/bit at 27°C ($\leq 10^{-13}$ A/bit at*

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[8] M. Kamoshida, "Trends of Silicon Wafer Specifications vs. Design Rules in ULSI Device Fabrication. Particles, Flatness and Impurity Distribution Deviations." *DENKA KAGAKU*, number 3, 1995, pages 194–204.

[9] W. Shockley. *Electrons and Holes in Semiconductors*. Princeton: D. Van Nostrand Co., Inc. 1950, page 69.

[10] D.K. Schroder. *Semiconductor Material and Device Characterization*, 2nd edition. New York:John Wiley & Sons, 1998, page 428.

[11]. M.A. Green, "Intrinsic Concentration, Effective Densities of States, and Effective Mass in Silicon," *Journal of Applied Physics*, volume 67, 1990, pages 2944–2954.

[12] A.B. Sproul and M.A. Green, "Improved Value for the Silicon Intrinsic Carrier Concentration from 275 to 375 K," *Journal of Applied Physics*, volume 70, 1991, pages 846–854.

100° C) for $A_{CRI} = 2.5\ \mu m^2$ [13]*, and $W = 0.5\ \mu m$; I_{limit} scales with CD generation. Assumes subthreshold device leakage, gate dielectric leakage, and diffusion current less than junction leakage current at 100°C.*

[O] *Other epitaxial defects such as hillocks and mounds should also be accounted for, but an appropriate yield model is not available.*

[P] *Range of target value refers to the center point measurement with tolerance to indicate within-wafer maximum positive or negative % deviation from the center value. Data applicable for p/p^-, p/p^+ and p/p^{++}. Flat zone modeled as 0.8 epi thickness.*

[Q] *Large area epitaxial defects modeled at 99% yield where $Y = \exp[-D_{LAD} R_{LAD} A_{CHIP}]$ (1), where $R_{LAD} = 1$ and A_{CHIP} applies to DRAM and MPU as appropriate.*

[R] *Epitaxial stacking faults modeled at 99% yield where $Y = \exp[-D_{SF} R_{SF} A_{CHIP}]$ (1), where $R_{SF} = 0.5$ and A_{CHIP} applies to DRAM and MPU as appropriate.*

[S] *Range of target value refers to the centerpoint measurement with tolerance to indicate within-wafer maximum positive or negative % deviation from the center value. The final device silicon is less than incoming material due to consumption during device fabrication. Currently listed values are applicable for both partially- and fully-depleted films and are the best available data at the present time. For fully depleted films, the silicon and buried oxide (BOX) thicknesses may be equally partitioned.*

[T] *Range of target value refers to the center point measurement with tolerance to indicate within-wafer maximum positive or negative % deviation from the center value. Currently listed values are applicable for both partially- and fully-depleted films and are the best available data at the present time. Top silicon-BOX interface charge $<10^{11}/cm^2$. For fully depleted films, the silicon and buried oxide (BOX) thicknesses may be equally partitioned.*

[U] *BOX defects with yield of 99%; $Y = \exp[-D_{BOX} R_{BOX} T \beta (CD)^2 \delta]$ (1), D_{BOX} = BOX defect density (mainly pinholes), $R_{BOX} = 0.2$ (best present estimate), $\beta = 1$ for DRAM and 10 for MPU; $\delta = 6$ units (gate, source, and drain [includes LDD extension])*

[V] *Inclusions defects with yield of 99%; $Y = \exp[-D_{INC} R_{INC} T \beta (CD)^2 \delta]$,* [1] *$D_{INC}$ = inclusion defect density, $R_{INC} = 1$ (best present estimate), $\beta = 1$ for DRAM and 10 for MPU; $\delta = 1$ unit (gate). Test is done using HF etchant* [14,15,16] *to decorate defects and subsequent optical counting. Sources of inclusions can include COPs, metal silicides, or local SiO_2 islands in the top silicon layer. These inclusions may also be detected by localized light scattering (LLS) measurements)* [15, 16, 17]*.*

[W] *Yields comparable to bulk devices have been achieved with threading dislocations, D_{TD}, of $2 \times 10^6/cm^2$. Kill ratios are not sufficiently known for reliable calculations; experimental yield/D_{TD} correlation data must be obtained. Downward trends in D_{TD} for future technology generations are expected.*

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[13] A.F. Tasch and L.H. Parker, "Memory Cell and Technology Issues for 64- and 256-Mbit One-Transistor Cell MOS DRAMs," *Proceedings of IEEE*, volume 77, 1989, pages 374–388.

[14] Y. Omura, S. Nakashima, K. Izumi, and T. Ishii, "0.1-um-Gate, Ultrathin-Film CMOS Devices Using SIMOX Substrate with 80-nm-Thick Buried Oxide Layer," *IEDM Technical Digest*, 1991, pages 675–678.

[15] D.K. Sadana, J. Lasky, H.J. Hovel, K. Petrillo and P. Roitman. "Nano-Defects in Commercial Bonded SOI and SIMOX," 1994 *IEEE International SOI Conference Proceedings*, Nantucket Island, MA (1994) pages 111–1112.

[16] W. P. Maszara, R. Dockerty, C.F.H. Gondran, and P.K. Vasudev, "SOI Materials for Mainstream CMOS Technology," Silicon-On-Insulator Technology and Devices VIII, X. Cristoloveanu, P.L.F. Hemment, K. Izumi and S. Wilson editors, PV 97-23, *The Electrochemical Society Proceeding Series*, Pennington, NJ (1997), pages 15–26.

[17] H. Aga, M. Nakano and K. Mitani, "Study of HF Defects in Thin Bonded SOI Dependent on Original Wafers," *Extended Abstracts of the 1998 International Conference on Solid State Devices and Materials*, Hiroshima (1998), pages 304–305.

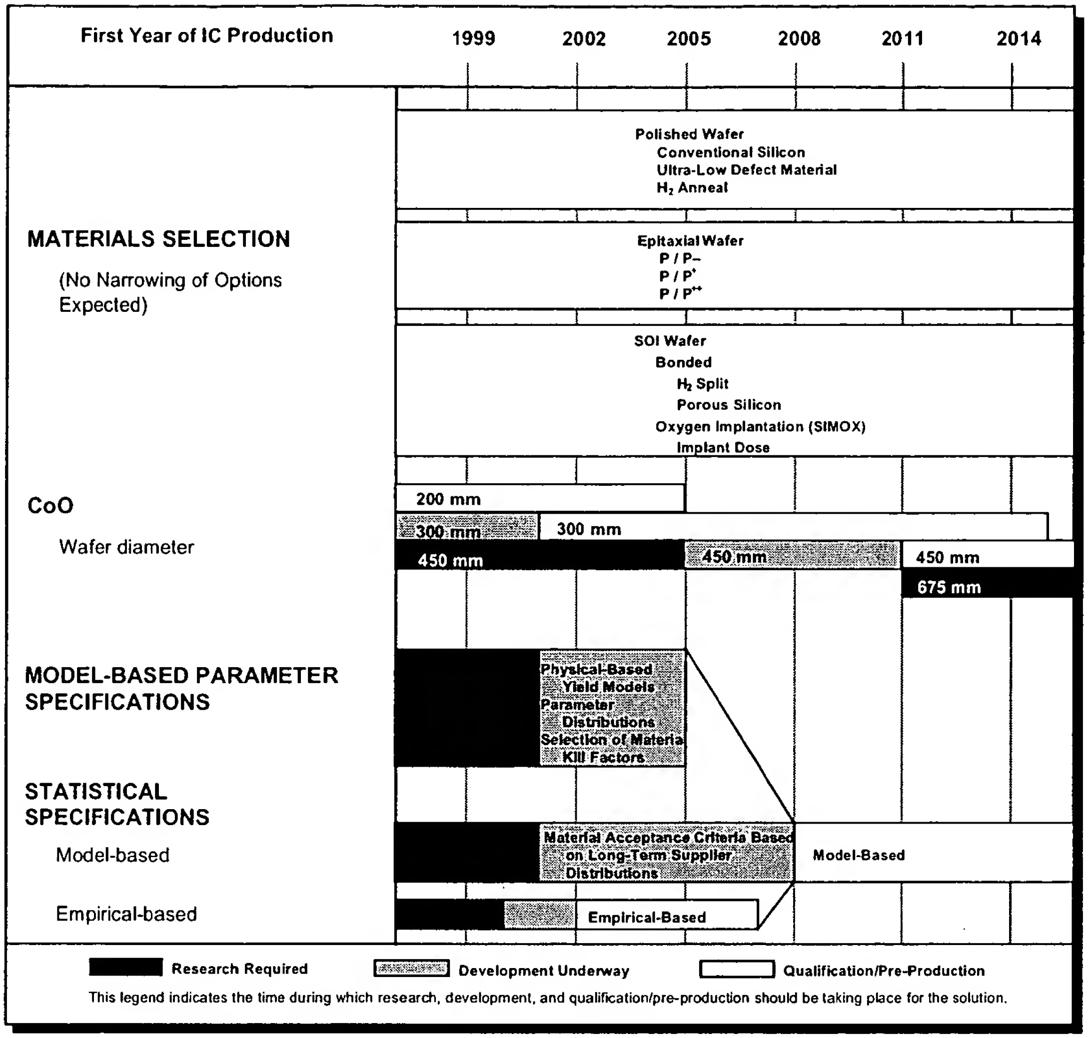

Figure 17 Starting Materials Potential Solutions

The ideal methodology to control overall material-contributed yield loss would be to partition loss allocations by defect types so that an overall IC fabrication yield loss due to the starting material does not exceed 1%. The yield loss for a particular defect is equal to the integral of the product of (1) the probability of failure due to a given value of the parameter (as established by the appropriate yield model) and (2) the fraction of wafers having that value (as established by the log-normal distribution function). With this approach, one can determine acceptable product distributions, which can then be utilized as materials acceptance criteria. Rather than a table of allowable parameter limits, this methodology would tailor fit specifications to product distributions demonstrated by individual suppliers.

Before such an approach can be realized, three advances are necessary. First, current yield models need to be validated for most parameters. Second, supplier distributions for parameters have to be established. Third, materials acceptance practices must be modified to allow for acceptance based on these supplier product distributions rather than small sample testing by the IC manufacturer. These issues are also

addressed in the potential solutions in Figure 17. In the meantime, yield models based on the best available information are used and parameters are assigned a limit based on a 99% yield requirement for that parameter. It is further assumed that any individual wafer will not contribute significantly to the yield loss for any parameters except for the specific parameter being considered. This empirical approximation has been shown to result in values nearly equal to the limit values obtained from the ideal methodology for modeled parameter distributions.

In the future, as the acceptable values for many parameters approach detection or resolution limits, enhanced cooperation between wafer suppliers and IC manufacturers will be essential in establishing and maintaining acceptable product distributions. Further development of IC yield models in relation to material characteristics is required, so that the ideal methodology described above can be implemented to establish acceptable product distributions. It is essential to balance the "best wafer possible" against the CoO opportunity of not driving silicon requirements to the detection limit, but instead to some less stringent value consistent with achieving high IC yield. Therefore, the surface metal and particle trends for starting wafers are less stringent than the pre-gate values listed in Surface Preparation (see Tables 33a and 33b) because it is assumed that a minimum cleaning efficiency of 50% takes place during the early IC processing steps. Both the chemical nature of the surface produced by the wafer supplier (hydrophobic versus hydrophilic) and the wafer-carrier interaction during shipment are important in controlling the subsequent adsorption of impurities and particles on the wafer surface.

The physical structure of the wafer surface has emerged as a critical concern. Both polished and epitaxial wafers exhibit defects that must be controlled to achieve high IC yields. Critical polished wafer defects include both surface chemical residues, such as organics and particles, and grown-in microdefects, such as "crystal-originated pits" (COPs). Structural defects, such as epitaxial stacking faults and other large area defects, must be controlled on epitaxial wafers. Material requirements are expressed in terms of specific types of surface defects. The removal and prevention of surface defects is a current state-of-the-art challenge for silicon wafer technology. The development of laser scanning and other instrumentation to count, size, and determine the composition and morphology of these defects is a critical metrology challenge. It is important to note that the total defect count is the sum of the various constituents. For example, both particles and COPs must be taken into account when considering the total surface defect density on polished wafers. This section does not consider either the availability or effectiveness of methods to monitor and distinguish these defects.

Additionally, the back surface of the wafer is increasingly being polished to reduce particle contamination, improve wafer flatness, and increase wafer strength. The polished back surface more readily exhibits microscopic contamination and handling scratches; ironically, a cleaner surface may actually appear to be dirtier. More stringent robotic handler standards may be required to ensure conformance with the implicit back-surface cleanliness requirements. Flatness degradation due to the presence of back-surface particles, which were previously hidden within the back-surface roughness, must be considered. Many external gettering techniques may also degrade the quality of the polished back surface and, in the case of non-uniformities in deposited-film-based external gettering, may degrade the wafer flatness. Such external gettering techniques may be inappropriate.

Polished wafer—As device geometries continue to shrink, ultra-low material defects and surface micro-property variations are becoming more important. The formation of uncontrolled SiO_x precipitates is likely to result in excessive device leakage current, necessitating greater attention to internal gettering in polished wafers. The magnitude and uniformity requirements will impose stringent bulk defect control to achieve homogeneous internal gettering capabilities.

The dependence of gate dielectric integrity—and the resulting D_0—on the crystal growth parameters and the related role of point defects and agglomerates have been extensively documented. This parameter has served effectively as a measure of material quality for several device generations. However, for device structures with equivalent oxide thicknesses described in Tables 34a and 34b, this parameter does not appear to relate to device yield and performance. Therefore, D_0 has been deleted from Tables 32a and 32b as

a target parameter. It should be noted, however, that with the potential onset of gate dielectric materials with dielectric constants significantly larger than SiO_2, these materials may require different pre- and post-gate surface preparation cleans.

Epitaxial wafer—The improved gate dielectric integrity in epitaxial material is due to the lack of residual polishing micro-damage and grown-in micro-defects (COPs), both of which appear in polished wafers. However, the presence of extended area defects and epitaxial stacking faults can also degrade the gate dielectric integrity so these defects must also be carefully controlled. For present applications, p/p^+ and p/p^{++} continue to be the mainstream epitaxial structures. For epitaxial layer resistivity greater than a few Ω-cm, a back-surface seal may be required for the p/p^{++} structures. The potential utilization of an implanted ground plane (high dose buried layer) on a polished wafer to prevent latch up and to getter impurities, rather than an epitaxial p/p^+ structure, is also receiving attention, although the control of COPs will be required in polished wafers. The utilization of p/p^- is also receiving attention for advanced IC applications, although this material configuration does not exhibit the solubility-enhanced iron gettering capability of heavily boron doped substrates. This deficiency, however, may be offset by the benefit of reduced system capacitance as compared to heavily doped substrates.

In the absence of solubility-enhanced gettering, the role of oxygen may have to be reassessed. It is well known that oxygen precipitates more slowly in p^- as compared with p^+ and p^{++} material. Because the appropriate oxygen concentration significantly depends on the IC thermal process sequence to be employed, many factors must be considered in the selection of the optimal oxygen concentration, especially in the case where the shallow trench isolation (STI) is greater than the epitaxial layer thickness.

Silicon-on-insulator wafer—SOI obviates the concern about latch-up while offering the potential for high speed, low-power applications, soft-error immunity, fewer process steps, smaller chip size, and utilization of the previous generation's factory equipment to achieve the required number of chips per wafer. Different SOI approaches may be necessary to service different IC applications. Evaluation of the various SOI wafer fabrication techniques by material characterization and identification of the relationships between defects and SOI properties, defect control by gettering and the impact of defects on subsequent device properties, such as transconductance, buried-oxide breakdown voltage, and leakage current, is essential. Some bulk IC designs can be transferred directly to SOI substrates. However, process and mask redesign may further improve performance and reduce chip size inasmuch as unique device configurations may be required in many cases. In any case, even if SOI does not extend the device scaling trend of the IC industry compared to conventional silicon materials, the benefits of high speed, low-power consumption, and reduced soft errors may motivate its use for certain applications at any given technology node.

Large diameter wafer—The conversion to 300 mm diameter wafers, beginning slowly in 1999 with peak conversion anticipated about 2002–2003, is necessary to achieve the required economy of scale for large volume IC manufacturing. International cooperation and standardization of wafers, carriers, and factory protocol continue to be critical for achieving this conversion in a cost-effective and timely manner. Business issues are the primary migration concern as it appears that the engineering issues associated with cost-effective 300 mm crystal growth and wafer gravitational stresses can be addressed. Projections of wafer diameter beyond 300 mm suggest that 450 mm may be the next appropriate size. However, the acceleration of technology generations and related economic factors may cause the introduction of 450 mm wafers to occur later than is currently projected. Continuation of the present wafer-diameter trend would require the implementation of research in 2011 to drive the introduction of 675 mm wafers in about 2020. These wafers are projected to be approximately 1 mm thick, but significant gravitational stress and related equipment platform issues are anticipated with these wafers.

Continuation of past wafer diameter trends is illustrated in the potential solutions in Figure 17; nevertheless, it is far from clear that 450 mm or 675 mm diameter wafers will be economically viable. The engineering issues associated with these diameters also appear to be enormous. A paradigm shift in the preparation of cost-effective silicon substrates may be required to mitigate the escalating costs associated with conventional silicon substrate materials. One possible approach is the introduction of cost-effective

SOI wafers. Another approach is the fabrication of silicon materials on an appropriate substrate so that it is not necessary to remove half or more of the bulk silicon wafer to conform to IC package dimensions.

SURFACE PREPARATION

Surface preparation processes have been relatively long-lived. Research and development in this area have focused largely on maximizing the quality of the gate dielectric. Changes have been made, for example, to improve particle performance, reduce surface roughening or eliminate watermarks left by drying. The dielectric material has remained silicon dioxide throughout, making fundamental changes in front-end chemistries unnecessary. Back end of line (BEOL) processes have been similarly stable owing to long-term use of aluminum as a wiring material and SiO_2 as an interlayer dielectric. In the future, materials changes are expected in both the FEOL and BEOL. Fundamental changes to surface preparation processes will likely be required.

In the FEOL, new gate dielectrics are being adopted. Initially, materials (silicon nitride, nitrided oxides) may be compatible with existing surface preparation processes. Higher κ materials will follow, but are not yet well defined. In any case, control of interfaces will be increasingly important. Some materials that have been suggested will require new cleaning chemistries. Along with new dielectrics, new gate electrode materials are anticipated. Metal gates may not be compatible with the aqueous chemistries that have been dominant in the FEOL. Solvent based processes similar to those found in the BEOL may be needed, though for ESH reasons it will be desirable to find alternatives.

BEOL surface preparation processes must be compatible with copper and low κ dielectrics. For example effective post-CMP cleans and resist removal processes are needed for Cu and low κ materials. Further, it will be necessary to minimize backside Cu contamination levels, which may require additional backside cleans. Increasing numbers of wiring levels make these processes continually more important. The number of surface preparation steps in the BEOL often exceeds the number in the FEOL. Tables 33a and 33b summarizes the technology requirements for surface preparation.

Surface preparation challenges and potential solutions are shown in Figure 18. Wet chemical cleaning technologies are favored because many inherent properties of aqueous solutions facilitate the removal of metals (high solubility in liquid chemistries) and particles (zeta-potential control, shear stress and efficient energy transfer by megasonics). Hence, wet chemical surface preparation methods will likely continue to find wide application in the foreseeable future. Gas phase cleaning technologies have not been widely used to date, partly due to CoO issues and the absence of technical necessity. Their more urgent need may arise, however, to provide interfacial control for advanced gates and/or interconnect layers. Gas phase chemistries can more easily penetrate high aspect ratio structures such as vias and capacitor trenches, but an effective, non-damaging particle removal process is still needed.

Surface preparation technology overlaps many technology thrusts. Reduced chemical use, chemical and water recycling, and alternative process technologies offer ESH and CoO benefits. Dilute chemistries have become more common in recent years, and this trend will continue. Ozonated water processes show much promise as replacements for sulfuric acid based resist strips and cleans. Efforts in deionized (DI) water usage reduction and recycling should continue. Additional CoO benefits can be realized by footprint reduction, fluid flow optimization through modeling, and *in situ* sensor-based process control. In general, increased use of *in situ* monitoring may be required for 300 mm due to the high costs of monitor wafers and of any degradation in product quality.

Surface preparation and defect reduction technology are likewise closely coupled. Low wafer defect levels required after surface preparation depend on appropriate purity levels in chemicals and DI water. To minimize CoO, however, aggressive purity targets should be adopted only where a technological justification exists. In all areas of surface preparation, a balance must be achieved between process and defect performance, cost, and environmental issues.

Table 33a Surface Preparation Technology Requirements—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
Front End of Line [A]								
DRAM critical area (cm^2) [B]	0.32	0.32	0.68	0.68	0.68	1.6	1.6	D ½
Logic critical area (cm^2) [C]	0.1	0.1	0.13	0.13	0.13	0.19	0.19	M
DRAM GOI D_0 (cm^{-2}) [D]	0.03	0.03	0.01	0.01	0.01	0.01	0.01	D ½
Logic GOI D_0 (cm^{-2}) [D]	0.1	0.1	0.08	0.08	0.08	0.05	0.05	M
Light scatterers, front side [E]								
DRAM (cm^{-2})	0.064	0.06	0.058	0.068	0.064	0.06	0.051	D ½
Logic (cm^{-2})	0.064	0.06	0.058	0.068	0.064	0.06	0.051	M
Particle size (nm)	90	82.5	75	65	60	55	50	D ½
Light scatterers, back side (cm^{-2}) [F]	0.315	0.325	0.290	0.275	0.265	0.250	0.240	D ½
Particle size (nm) [F]	500	450	400	333	300	267	233	D ½
Critical surface metals [G]	$\leq 9\times10^9$	$\leq 7\times10^9$	$\leq 6\times10^9$	$\leq 4.4\times10^9$	$\leq 3.4\times10^9$	$\leq 2.9\times10^9$	$\leq 2.5\times10^9$	D ½
Mobile ions (atoms/cm^2) [H]	4.25×10^{10}	4.25×10^{10}	4.70×10^{10}	4.70×10^{10}	4.70×10^{10}	4.68×10^{10}	4.7×10^{10}	M and D ½
Organics/polymers (C atoms/cm^2) [J]	7.3×10^{13}	6.6×10^{13}	6.0×10^{13}	5.3×10^{13}	4.9×10^{13}	4.5×10^{13}	4.1×10^{13}	M and D ½
Surface oxygen (O atoms/cm^2) [K]	$<1\times10^{14}$	$<1\times10^{14}$	$<1\times10^{14}$	$<1\times10^{14}$	$<1\times10^{14}$	$<1\times10^{14}$	$<1\times10^{12}$	M and D ½
Surface roughness (nm) [L]	0.15	0.14	0.13	0.12	0.12	0.1	0.1	M and D ½
DRAM water marks (/cm^2) [M]	2.50×10^{-3}	2.27×10^{-3}	2.03×10^{-3}	1.80×10^{-3}	1.63×10^{-3}	1.45×10^{-3}	1.28×10^{-3}	D ½
Logic water marks (/cm^2) [M]	2.79×10^{-3}	2.64×10^{-3}	2.49×10^{-3}	2.34×10^{-3}	2.20×10^{-3}	2.07×10^{-3}	1.93×10^{-3}	M
Back End of Line [N]								
Particles (cm^{-2}) [O]	0.064	0.06	0.058	0.068	0.064	0.06	0.051	D ½
Particle size (nm)	180	165	150	130	120	110	100	D ½
Corrosion resistance (years) [P]	>10	>10	>10	>10	>10	>10	>10	D ½
Surface oxygen (O atoms/cm^2) [K]	$<1\times10^{14}$	$<1\times10^{14}$	$<1\times10^{14}$	$<1\times10^{14}$	$<1\times10^{14}$	$<1\times10^{14}$	$<1\times10^{12}$	D ½

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 33b Surface Preparation Technology Requirements—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
Front End of Line [A]				
DRAM critical area (cm^2) [B]	3.14	6.4	6.4	D ½
Logic critical area (cm^2) [C]	0.24	0.43	0.43	M
DRAM GOI D_0 (cm^{-2}) [D]	0.003	0.002	0.002	D ½
Logic GOI D_0 (cm^{-2}) [D]	0.042	0.023	0.023	M
Light scatterers, front side [E]				
DRAM (cm^{-2})	0.052	0.052	0.052	D ½
Logic (cm^{-2})	0.052	0.052	0.052	M
Particle size (nm)	35	25	18	D ½
Light scatterers, back side [F]	0.210	0.185	0.160	D ½
Particle size (nm) [F]	133	67	17	D ½
Critical surface metals (at/cm^2) [G]	$\le 2.1\times10^9$	$\le 1.8\times10^9$	$\le 1.7\times10^9$	D ½
Mobile ions (atoms/cm^2) [H]	4.4×10^{10}	4.5×10^{10}	6.0×10^{10}	M and D ½
Organics/polymers (C atoms/cm^2) [J]	2.8×10^{13}	2.0×10^{13}	1.4×10^{13}	M and D ½
Surface oxygen (O atoms/cm^2) [K]	$<1\times10^{12}$	$<1\times10^{12}$	$<1\times10^{12}$	M and D ½
Surface roughness (nm) [L]	0.08	0.08	0.08	M and D ½
DRAM water marks (/cm^2) [M]	9.02×10^{-4}	4.51×10^{-4}	6.39×10^{-4}	D ½
Logic water marks (/cm^2) [M]	1.63×10^{-3}	1.35×10^{-3}	1.12×10^{-3}	M
Back End of Line [N]				
Particles (cm^{-2}) [O]	0.052	0.052	0.052	D ½
Particle size (nm)	70	50	36	D ½
Corrosion resistance (years) [P[	>10	>10	>10	D ½
Surface oxygen (O atoms/cm^2) [K]	$<1\times10^{12}$	$<1\times10^{12}$	$<1\times10^{12}$	D ½

Solutions Exist ☐ *Solutions Being Pursued* ☐ *No Known Solutions* ■

Notes for Tables 33a and b Surface Preparation Requirements

[A] *Starting wafer up to deposition of the pre-metal dielectric*

[B] *Bits/chip multiplied by the critical dimension squared*

[C] *Transistors/chip multiplied by 10 × the critical dimension squared*

[D] *Based on the model $Y = 1/(1 + AD)$, using an acceptable yield of 99% and the critical areas given for DRAM and logic nodes. Electrical measurement of D_0 should follow ASTM F 1771-97 and the revised EIAJ/JEDEC Standard 35-1, using appropriate sample sizes and capacitor areas.*

[E] *Particles modeled for 99% yield by $Y = \exp[-D_pR_p\, T\, b\, (CD)^2\, d]$, $R_p = 0.2$, T = # of transistors or bits/chip per technology generation, b = width/length CD ratio = 1 for DRAM and 10 for MPU, d = 1 unit (1) in previous models. In the current model, a = bd, where "a" is the DRAM cell area factor, a function of the technology generation. The analogous MPU model is not available, so the MPU particles are taken as equal to the DRAM values. (see backup Excel workbook, "Particles")*

[F] *Modeled as in Table 32, except with kill ratio of 0.2. Values are therefore ½ those for Starting Materials. (see backup Excel workbook "Particles")*

[G] *Metals empirically modeled for 99% yield by* $Y = \exp[-D_M R_M T A (CD)^2]$.[6] $R_M = 0.2$, *T = # of transistors or bits/chip per technology generation and A is the DRAM cell area factor, a function of the technology generation, with* $D_M = K_2 (M)^3 \exp[-To/0.7]$, $K_2 = 1.854 \times 10^{29}$ cm^4. *To equivalent oxide thickness (corrected for quantum mechanical and poly depletion effects), in nm per technology generation (based on MIS DRAM device structure.) The experimental data resulting in this model is based on and extends the precursor publication)*[7]. *Assuming a pre-gate cleaning efficiency of 50% for metals in Surface Preparation, the metal values are accordingly increased by a factor 2. This results in a number twice that listed in the Surface Preparation values in Table 33. The value listed is the limit for each of the following metals: Ca, Co, Cu, Cr, Fe, K, Mo, Mn, Na, and Ni.*

[H] *Based on* $Nm = 1/q \times C_{gate} \times DV$, *where* C_{gate} *is computed for maximum effective gate dielectric thickness and DV is the allowable threshold voltage variability for this node. It is assumed that 10% of allowable shift is attributable to nm.*

[J] *Measured after critical clean including pre-gate, pre-poly, pre-metal, pre-silicide, pre-contact, and pre-trench fill. (See backup Excel workbook, "Organics").*

[K] *As determined by SIMS depth profiling through the tungsten silicide film into the polysilicon layer. (see backup Excel workbook, "Surface Oxygen").*

[L] *Surface roughness measured using tapping mode AFM on a 2 µm×2 µm scan area. Measured prior to oxidation on EPI substrates. Target values are for* SiO_2 *gate dielectric. (see backup Excel workbook, "Surface Roughness").*

[M] *Water marks defectivity levels were calculated using the yield model of Y= 1/(1+AD) where Y is yield, A is the chip area and D is the defect density. This approach assumes that one physical defect (water mark) results in one failed die. Y in all cases is .99. (see backup Excel workbook, "Watermarks").*

[N] *Poly-silicide metal dielectric deposition through passivation*

[O] *BEOL target is the same defect density as FEOL. However, the critical particle size is equal to CD rather than CD/2. (See backup Excel workbook, "Particles").*

[P] *Based on accelerated testing at 100% relative humidity. (See backup Excel workbook, "Corrosion Resistance").*

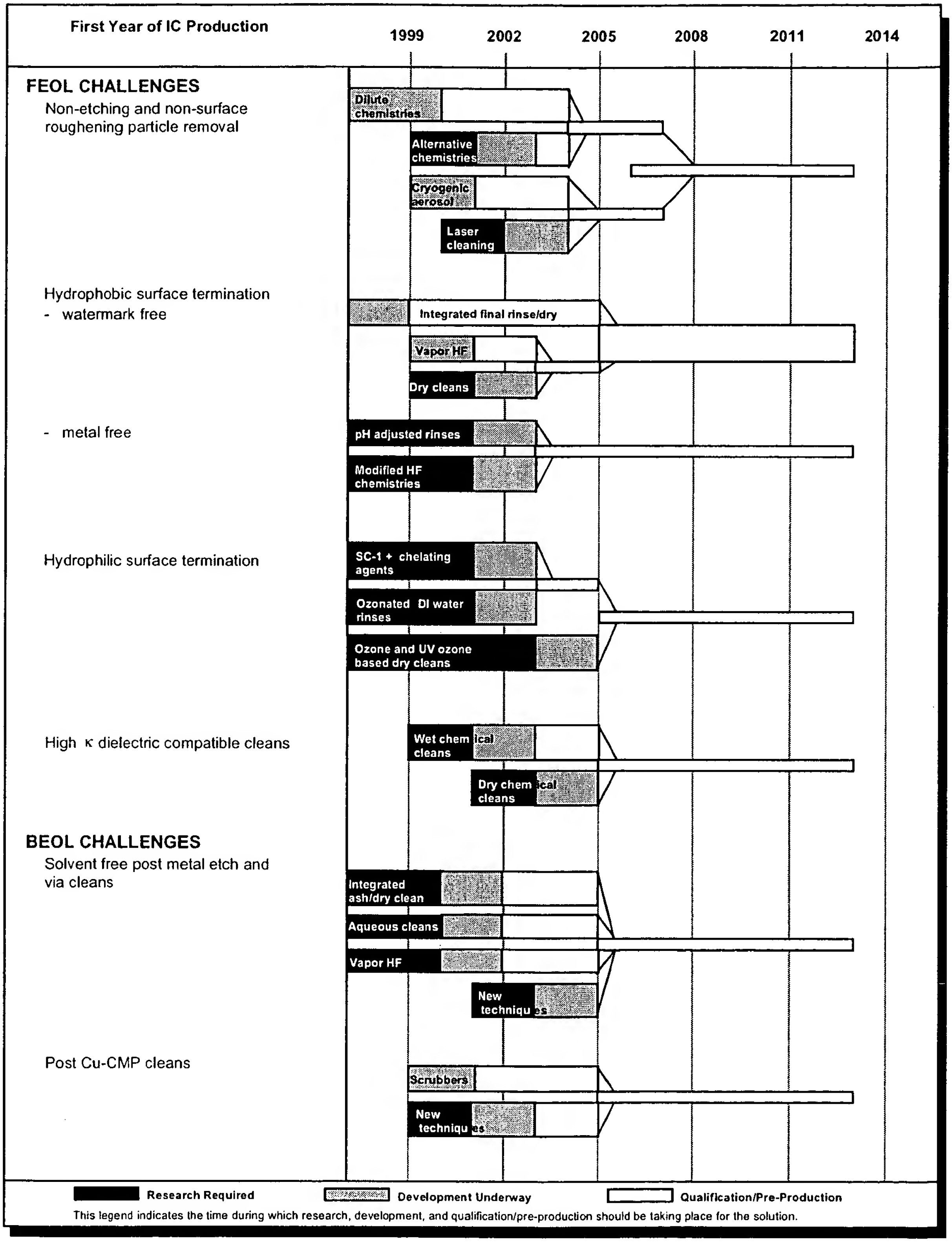

Figure 18 Surface Preparation Potential Solutions

THERMAL/THIN FILMS AND DOPING

Front end processing requires the growth and deposition of high quality, uniform, defect-free films. These films may be insulators, silicon, or conductors. The precision doping of the underlying substrate and deposited layers is normally required. In addition to reduced thermal budgets required by device scaling, several other difficult challenges have been identified for this area including the growth or deposition of reliable very thin gate dielectric layers; the identification and development of alternate high dielectric constant layers and suitable interface layers for both gate and DRAM capacitor applications; the formation of and making contact to ultra-shallow device junctions; and the development of alternate, depletion-free, low-resistivity gate materials. Other important challenges include the achievement of abrupt channel doping profiles, defect management for minimum post implant leakage in small thermal budget environments, sidewall spacer formation. Drive current limits by high channel doping levels may ultimately require the development of new device structures. CMOS-compatible innovative solutions are needed in all of these areas. Underlying all these concerns is the inevitable rise of leakage currents associated with threshold scaling, gate dielectric tunneling, and junction leakage.

THERMAL/THIN-FILMS

The gate dielectric has emerged as one of the most difficult challenges for future device scaling. Requirements summarized in Tables 34a and 34b indicate an oxide equivalent thickness progressing to substantially less than 1 nm. Tunneling currents preclude the use of SiO_2 dielectric layers below approximately 1.5 nm thickness where tunneling currents larger than 1 A/cm^2 are predicted. Since tunneling currents will scale exponentially with further thickness reductions, phase-out of this dielectric material is needed *as early as the 100 nm node.* No suitable alternative high dielectric constant material and interface layer has been identified with the stability and interface characteristics to serve as a gate dielectric. Years of research and development are required to identify and qualify a suitable alternative material. Similar problems are anticipated with the DRAM storage capacitor dielectric at an earlier technology node. The near-term gate dielectric solution requires the fabrication and use of ultra-thin silicon oxide, oxynitride films, or silicon nitride films. The latter film shows attractive boron diffusion penetration resistance and a moderately higher dielectric constant value of 7. Near term solutions will impose severe restraints on surface preparation, pre-and post-process ambient control, silicon compatible materials development (such as gate electrodes and contacts), and post processing thermal budgets.

Improved thickness control and uniformity will be essential to achieve V_t control for large diameter wafers. Sensitivity to post-gate process induced damage associated with ion implant and plasma etching is expected to increase especially as it relates to leakage associated with gate perimeter. Intermediate and long-term solutions require the identification of materials with a higher dielectric constant (>10 suggested for intermediate term and >20 for long term) with other electrical characteristics (such as stability and interface state densities) and reliability approaching that of high quality gate SiO_2. A major problem with a material other than SiO_2 is the probability that a very thin SiO_2 layer will still be required at the channel and/or gate electrode interface to preserve interface state characteristics and channel mobility. This would severely degrade any benefits that accrue from the use of the high κ dielectric. The presence of a single molecular layer of Si-O bonding to bridge between the silicon substrate and a high κ material is expected to present a physical limit to scaling of effective dielectric thickness below 0.3 nm.

Another challenge is the achievement of acceptably low electrical leakage. To fill these needs, the high κ dielectric must have a band gap of 4–5 eV with a barrier height of >1 eV to limit thermionic emission and Fowler-Nordheim tunneling. In addition, the candidate dielectric material must have negligible trap densities to suppress Frenkle-Poole tunneling. Finally, the material must have excellent diffusion barrier properties to prevent gate electrode material or gate electrode dopant contamination of the transistor channel.

Table 34a Thermal/Thin Films, Gate Etch, and Doping Technology Requirements—Near Term

YEAR / TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
MPU Gate Length (nm)	140	120	100	85	80	70	65	M
Equivalent physical oxide thickness T_{ox} (nm) [A]	1.9–2.5	1.9–2.5	1.5–1.9	1.5–1.9	1.5–1.9	1.2–1.5	1.0–1.5	M
Gate dielectric leakage at 100°C (nA/μm) high-performance [B]	5	7	8	10	13	16	20	M
Gate dielectric leakage at 100°C (pA/μm) low power [B]	5	7	8	10	13	16	20	M
Thickness control EOT (% 3σ) [C]	<± 4	<± 4	<± 4	<± 4	<± 4	<± 4	<± 4	M
Leffective control	≤ 20%	≤ 20%	≤ 20%	≤ 20%	≤ 20%	≤ 20%	≤ 20%	M
L_{gate} 3σ variation (nm) (dense and isolated lines) [D]	14	12	10	8.5	8	7	6.5	M
CD bias between dense and isolated lines [E]	≤ 15%	≤ 15%	≤ 15%	≤ 15%	≤ 15%	≤ 15%	≤ 15%	M
Minimum measurable gate dielectric remaining (post gate etch clean) [F]	>0	>0	>0	>0	>0	>0	>0	M
Sidewall spacer thickness (nm) extension structure [G]	72–144	65–130	59–108	52–104	48–96	44–88	40–80	M
Sidewall spacer thickness (nm) elevated contact [H]	—	—	—	—	—	—	20–40	M
Sidewall spacer thickness (nm) single drain [I]	—	—	—	—	—	—	—	M
Sidewall spacer thickness control (nm, 3σ)	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%	M
Gate electrode sheet Rs (Ω/•) [J]	4–6	4–6	4–6	4–6	4–6	4–6	4–6	M
Gate electrode thickness [K]	140	120	100	85	80	70	65	M
Gate electrode resistivity (μΩ-cm) [L]	70	60	50	43	40	35	33	M
Active poly doping to achieve 10% GOx depletion [M]	2.2×10^{20}	2.2×10^{20}	3.1×10^{20}	3.1×10^{20}	3.1×10^{20}	3.9×10^{20}	4.6×10^{20}	M
Silicide thickness (nm) [N]	55	45	40	34	32	28	25	M
Contact silicide sheet Rs (Ω/□) [O]	2.7	3.3	3.8	4.4	4.7	5.4	6.0	M
Contact maximum resistivity (Ω-cm²) [P]	$< 3.0\times10^{-7}$	$< 2.5\times10^{-7}$	$< 2.0\times10^{-7}$	$<1.7\times10^{-7}$	$<1.6\times10^{-7}$	$<1.1\times10^{-7}$	$<1.0\times10^{-7}$	M
Maximum silicon consumption (nm) [Q]	36–70	32–60	26–50	22–43	20–40	18–36	16–33	M
Contact Xj (nm) [R]	75–145	65–125	55–105	45–90	43–85	38–75	35–70	M
Drain extension Xj (nm) [S]	42–70	36–60	30–50	25–43	24–40	20–35	20–33	M
Drain extension sheet resistance (Ω/□)	350–800	310–760	280–730	250–700	240–675	220–650	200–625	M
Lateral abruptness for source extension (nm/decade) [T]	4.8	4.1	3.4	2.9	2.7	2.4	2.2	M
Extension lateral abruptness (nm/decade) [U]	14	12	10	8.5	8	7	6.5	M
Potential: dopant variation—Position (nm)	15	10	10	<10	<8	<8	<7	M
Potential: dopant variation—Dose	<10% (Halo)	<10% (Halo)	<9% (Halo)	<8%	<7%	<6%	<5%	M
Channel concentration for W depletion $<1/4L_{eff}$ (cm^{-3}) [V]	2.0×10^{18}	2.3×10^{18}	2.7×10^{18}	3.0×10^{18}	3.3×10^{18}	3.7×10^{18}	4.0×10^{18}	M
Uniform channel concentration (cm^{-3}), for V_t=0.4 [W]	0.8–1.5×10^{18}	0.8–1.5×10^{18}	1.5–2.5×10^{18}	1.5–2.5×10^{18}	1.5–2.5×10^{18}	2.5–4.0×10^{18}	2.5–6.0×10^{18}	M
Retrograde Channel Depth (nm) [X]	< 21–35	< 18–30	< 15–25	< 12–22	<12–20	< 10–18	< 10–17	M

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Table 34b Thermal/Thin Films, Gate Etch, and Doping Technology Requirements for Logic—Long Term Needs

YEAR / TECHNOLOGY NODE	2008 / 70 nm	2011 / 50 nm	2014 / 35 nm	DRIVER
MPU Gate Length (nm)	45	32	22	M
Equivalent physical oxide thickness T_{ox} (nm) [A]	0.8–1.2	0.6–0.8	0.5–0.6	M
Gate dielectric leakage at 100°C (nA/μm) high-performance [B]	40	80	160	M
Gate dielectric leakage at 100°C (pA/μm) low power [B]	40	80	160	M
Thickness control EOT (% 3σ) [C]	<± 4	<± 4	<± 4	M
Leffective control	≤ 20%	≤ 20%	≤ 20%	M
L_{gate} 3σ variation (nm) (dense and isolated lines) [D]	5	3.2	2.2	M
CD bias between dense and isolated lines [E]	≤ 15%	≤ 15%	≤ 15%	M
Minimum measurable gate dielectric remaining (post gate etch clean) [F]	>0	>0	>0	M
Sidewall spacer thickness (nm) extension structure [G]	28–56	20–40	14–28	M
Sidewall spacer thickness (nm) elevated contact [H]	14–28	10–20	7–14	M
Sidewall spacer thickness (nm) single drain [I]	7.5–15	5–10	3.7–7.5	M
Sidewall spacer thickness control (nm, 3σ)	≤ 10%	≤ 10%	≤ 10%	M
Gate electrode sheet Rs (Ω/□) [J]	4–6	4–6	4–6	M
Gate electrode thickness [K]	45	32	22	M
Gate electrode resistivity (μΩ-cm) [L]	23	16	11	M
Active poly doping to achieve 10% Gox depletion [M]	5.4×10^{20}	7.3×10^{20}	1.2×10^{21}	M
Silicide thickness (nm) [N]	20	15	12	M
Contact silicide sheet Rs (Ω/□) [O]	7.5	10.0	12.5	M
Contact maximum resistivity (Ω-cm^2) [P]	$< 5.0\times10^{-8}$	$< 2.5\times10^{-8}$	$< 1.5\times10^{-8}$	M
Maximum silicon consumption (nm) [Q]	14–26	10–19	7–17	M
Contact Xj (nm) [R]	30–55	20–40	15–35	M
Drain extension Xj (nm) [S]	16–26	11–19	8–13	M
Drain extension sheet resistance (Ω/□)	150–525	120–450	100–400	M
Lateral abruptness for source extension (nm/decade) [T]	1.25	0.8	0.5	M
Extension lateral abruptness (nm/decade) [U]	4.5	3.2	2.2	M
Potential: dopant variation—position (nm)	<5	<4	<3	M
Potential: dopant variation—dose	5.0×10^{-2}	3.0×10^{-2}	2.0×10^{-2}	M
Channel concentration for Wdepletion $<1/4L_{eff}$ (cm^{-3}) [V]	8.0×10^{18}	1.4×10^{19}	3×10^{19}	M
Uniform.. channel conc. (cm^{-3}), for V_t=0.4 [W]	$4.0–9.0\times10^{18}$	$0.9–1.5\times10^{19}$	$1.5–2.5\times10^{19}$	M
Retrograde channel depth (nm/decade) [X]	< 8–13	< 5–10	< 4–8	M

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Notes for Table 34a and b Thermal / Thin Films, Gate Etch, and Doping Requirements

[A] *This number represents the effective thickness of the dielectric alone, at the maximum operating frequency of the technology, without substrate or electrode effects, and is determined through an electrical measurement of capacitance corrected for substrate and electrode effects.*

[B] *The gate leakage, specified at 100°C, is taken to be less than or equal to 1% of the transistor off-state leakage at that temperature. This leakage is the same as the Process Integration chapter specifies (Table 28) off-state leakage (excluding the gate leakage component) at room temperature since the device subthreshold leakage and junction leakage components of leakage are expected to increase by a factor of 100x between room temperature and 100°C. This gate leakage is measured on the minimum nominal device, and the specification is taken to apply to all transistor bias configurations, that is, both when $V_g = V_s = 0$ and $V_d = V_{dd}$ as well as when $V_s = V_d \approx 0$ and $V_g = V_{dd}$.*

[C] *See reference.* [18]

[D] *The technical challenges related to etch are device structure dependent. A conventional MOS structure is assumed. If other integration schemes, such as the replacement gate, become the preferred approach, the details outlined in this table will have to be updated.*

[E] *The 10% CD budget is a combined number for lithography, etch, and metrology. No effort is being made to partition the contribution from each. It is believed that both lithography and etch will have to work together to achieve this CD control target.*

[F] *The need is to have some remaining gate dielectric after the gate etch clean step. Since the dielectric material effectively reduces between technology nodes, the ability of the etch system to stop on that dielectric becomes more difficult. In addition, the metrology capability to measure or detect remaining gate dielectric material is suspect for very small thicknesses.*

[G] *Sidewall spacer thickness = 0.94 × MPU physical gate length (with a range of about ±33%) for a contacting junction that is 0.94 × MPU physical gate length. Validity established using response surface methodology in A. Srivastava and C.M. Osburn. "Response surface based optimization of 0.1 µm PMOSFETs with Ultra-Thin Gate Dielectrics."* [19]

[H] *Sidewall spacer thickness = = 0.46 × MPU physical gate length (with a range of about ±33%).*

[I] *Sidewall spacer thickness = ½ of average extension junction depth (with a range of ±33%): the number was chosen to allow for lateral diffusion of the extension junction beneath the spacer.*

[J] *Continuation of the historical trend*

[K] *Taken as MPU physical gate length from aspect ratio considerations*

[L] *From the sheet resistance and film thicknesses requirements (average); assumes metal gate electrode at and beyond 100nm node.*

[M] *Poly Activation from a spreadsheet model based on V_{dd} and gate oxide requirements*

[N] *Silicide thickness should be less than ½ of the center Contact Xj to avoid consumption-induced increase in contact resistivity.* [20]

[O] *Contact silicide sheet resistance: assumes 15 µΩ-cm silicide resistivity, such as $TiSi_2$ or $CoSi_2$*

[P] *Si/Silicide maximum resistivity: numbers based on specification of total parasitic resistance < 10% Rdevice (Vdd/Isat). Spreadsheet used to compute components of parasitic resistance.* [21]

[Q] *Silicon consumption assumes formation of cobalt disilicide having silicide thickness/silicon consumption ratios of 0.97.*

[R] *Contact Xj = 0.8×Isolated Line (nm) (with a range of ±33%); based on historical curves. All junction depths measured from x=0 at gate dielectric/silicon interface.*

[S] *Xj at Channel = 0.4×Isolated Line (with a range of about ±25%).*

[T] *S/D Abruptness based on a spreadsheet that emphasizes the spreading resistance impact on total series resistance.* [22]

[U] *Channel abruptness is in nm per decade dropoff in doping concentration = 0.1 * Isolated Line (nm) - based on Short Channel effect* [23]

[V] *Drain extension concentration for W depletion < ¼ Logic Half Pitch (Equation 5-57).* [24]

[W] *Uniform channel concentration for V_t = 0.4* [25]*. Neither quantum mechanical nor potential increase in short channel effects were used in this calculations. These effects do, however, tend to offset each other. The assumption of a constant threshold voltage of 0.4 V may not be consistent with the leakage current criteria. To reach the leakage current criteria may result in unacceptably large threshold voltages for the scaled power supplies resulting in severe performance degradation. In addition, high concentration channels could severely impact drain currents due to impurity scattering.*

[X] *The retrograde well profile must be less than 0.5 × the drain extension depth to improve short channel effects.* [26,27]

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[18] P. Zeitzoff and A. Tasch, "Modeling of Manufacturing Sensitivity and of Statistically Based Process Control Requirements for a 0.18 micron NMOS device," *Characterization and Metrology for ULSI Technology: 1998 International Conference*, D.G. Seiler, et al. eds., page 73.

[19] A. Srivastava and C.M. Osburn, "Response surface based optimization of 0.1 µm PMOSFETs with Ultra-Thin Gate Dielectrics," *SPIE Proc.*, vol. 3506, (1998), page 253.

[20] C.M. Osburn, J.Y. Tsai, and J. Sun, "Metal Silicides: Active Elements of ULSI Contacts," *J. Electronic Mater.*, vol. 25(11), (1996), page 1725.

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[22] K.K. Ng and W.T. Lynch, "Analysis of the Gate-voltage-dependent Series Resistance of MOSFETs," *IEEE Trans. Electron Dev.*, vol. ED-33, (1986), page 965.

[23] Y.Taur, "25 nm CMOS Design Considerations," *IEDM 1998, Technical Digest*, IEEE, Dec. 1998, pages 789–792.)

[24] B.G. Streetman. "Solid State Electronic Devices," 4th ed., ,. Englewood Cliffs, NJ:Prentice Hall , 1995, page 174.

[25] R. Muller and T. Kamins. *Device Electronics for Integrated Circuits.* New York, NY:John Wiley and Sons, Inc., 1977, page 324.

[26] S.Thompson, P.Packan, and M.Bohr. "Linear versus Saturated Drive Current: Tradeoffs in Super Steep Retrograde Well Engineering," *VLSI Technology Digest*, (1996), page 154.

[27] I.De and C.M. Osborn, "Impact of Super-steep-retrograde Channel Doping Profiles on the Performance of Scaled Devides," *IEEE Trans. Elec. Dev.*, vol. 46, no.8, (1999), page 1711.

The gate electrode also represents a major challenge for future scaling. Channel autodoping associated with boron out-diffusion and polysilicon depletion will eventually require the phase-out of dual-doped polysilicon gate material. A long-term solution such as low resistivity gate material(s) is not presently comprehended and years of research will be required to identify and qualify an alternative.

Work function, resistivity, and compatibility with CMOS technology are key parameters for the new candidate material. The latter requires that different gate materials be used for the PMOS and NMOS transistor gate electrodes to achieve acceptable threshold voltages; the former having a Fermi level near the silicon valence band, and the latter having a Fermi level near the conduction band. Sheet resistance considerations may ultimately require the use of cladded gate electrodes, where the dielectric interface layer is used to achieve the desired gate work function and the second layer is used to lower the overall gate sheet resistance. Alternatives are the use of SOI or dual-junction isolated transistors where a mid band-gap Fermi level may be used in conjunction with substrate or well biasing. Near term potential solutions to the gate electrode problem include improvements in the doped polycide gate stack or the use of Si-Ge gates. Boron penetration resistance of the gate dielectric (such as the use of silicon nitride) is of great importance as is the development of enhanced means of activating the doped polysilicon for achieving tighter control of the work function.

The incorporation of alternate interfacial layers, high κ dielectrics, and new gate electrode materials into CMOS configurations poses a significant integration challenge. The thermal stability of most of the candidate material systems is inadequate to allow typical junction formation annealing cycles to be used after gate formation. The use of these new materials may force either junction annealing temperatures to be dramatically lowered or a reversal in the sequence of gate stack and junction formation, such as the "replacement gate scheme." These schemes increase manufacturing complexity and may impact device performance and reliability by altering the gate to junction overlap. A preferred solution to the integration of two gate electrode metals is the use of a metal and a compound of the same metal, such as W and WN, so that a simple reaction might locally convert the metal into its compound. Otherwise, it may be necessary to utilize complex and multiple processes to fabricate both NMOS and PMOS devices.

Sidewall spacers are currently used to achieve isolation between the gate and source/drain regions, as well as to facilitate fabrication of self-aligned, drain-engineered dopant structures. The robustness of the sidewall spacer limits the gate and source/drain contacting structure and processes that can be used. Sidewall spacers have traditionally been formed from deposited oxides, thermal oxidation of polysilicon, deposited nitrides, and combinations of these. These processes will continue to be used at least until the time when elevated or raised source/drain structures are required, at which time the lack of a potential spacer solution will become acute. Single drain elevated structures will require sidewall thicknesses in the range of 5–10 nm and gate dielectric-like reliability and stability to manage parasitic series resistance. Below about 20 nm even the best thermal oxides are susceptible to defect formation when subjected to selective epitaxial silicon or silicide processes. Nitrides or oxynitrides may offer a better alternative than oxide; however, additional research is needed to find and qualify an acceptable sidewall spacer.

The key thermal/doping integration issues are maintaining shallow junction profiles, obtaining high dopant activation, ensuring thermal compatibility of materials, and controlling how these issues impact device electrical performance. A potential solutions roadmap for FEOL Thermal/Thin Films is given in Figure 19.

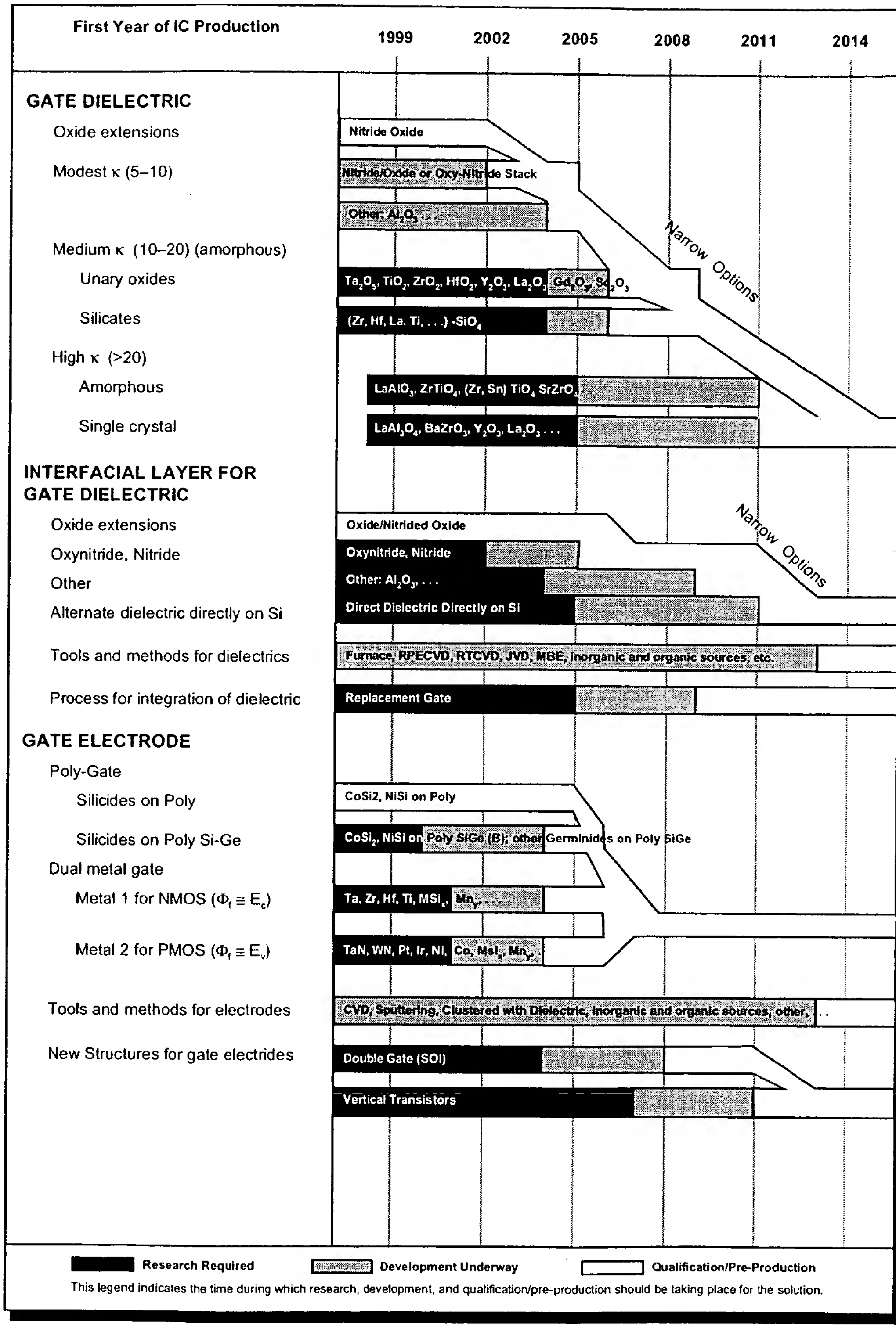


Figure 19 Thermal Thin Films Potential Solutions

DOPING TECHNOLOGY

The near-term difficult challenge facing doping technology is the extension of conventional methods used to fabricate ultra-shallow junctions into the deep submicron regime. Intrinsic within this challenge is simultaneously achieving both the depth of the scaled extension junction and the necessary lateral abruptness. The abruptness requirement is also expressed in the requirements for achieving a low series resistance, which is set to 10% of the derived channel resistance. The conflicting demands of producing highly doped, more shallow source/drain and drain extension junctions and contacting these with low sheet resistance contact material will also challenge the conventional salicide process. Several other difficult challenges have been identified involving the formation of and making contact to ultra-shallow device junctions. Underlying challenges include: activation technology to achieve 300 Ω/□ at <30 nm junction depths; stopping boron penetration of gate oxide; fabrication of low resistivity silicide contacts; 2D dopant profiling of ultra-shallow junctions; maintaining low particle levels at a meaningful size compared to the junctions; and placement of the layers (particularly the halo) with the necessary precision for the scaled devices.

Below the 70 nm node, the grand challenge is stated more simply as "Transistor Structure." Within this challenge is the issue that it is not presently known how to produce a doped layer, with activation above solid solubility, and using a restricted thermal budget. New transistor structures may be needed to achieve the transistor performance goals, yet these structures will need to be developed and qualified in time for production. These structures and processes will need to be temperature and process compatible with the high κ gate stack. For technologies less than 70 nm there is a similar set of underlying challenges: thermal process compatibility with the dielectric (activation versus high κ); formation of low resistance contacts; high conductivity extensions (200 Ω/□ at < 20 nm); engineering the extension to channel edge abruptness; and understanding metastable dopant activation. Underlying all these concerns is the inevitable rise of leakage currents associated with threshold scaling, gate dielectric tunneling, and junction tunneling.

EXTENSION

Scaling is expected to have a significant impact on processes used for doping drain extensions, channels, and channel edges. Drain extension doping levels are expected to increase, driven by the need to reduce both parasitic resistance and junction depth. Similarly, drain extension doping profiles, which with earlier technology nodes required lateral grading for minimum hot carrier damage, will need to become laterally abrupt to support low voltage operation. Sub-nanometer spatially resolved 2D metrology is needed to monitor the location and shape of both vertical and lateral dopant profiles in the extension region.

Potential doping solutions for these problems include ultra low energy ion implantation, plasma immersion ion implantation (PIII), and projection gas immersion laser doping (PGILD). A long-term solution is deposited doped layers (such as ALE).

CONTACT

The conventional means of shunting the contact regions with a self-aligned silicide will be challenged by the need to achieve low gate sheet resistivity while at the same time continuously minimizing silicon consumption in the source drain contact region. In addition, scaling of the contact area will result in unacceptable parasitic resistance if the specific contact resistivity of the silicon/silicide interface cannot be correspondingly reduced. An acceptable contact resistivity will require that the maximum concentration of activated dopant be achieved in the silicon at the silicide interface, and may also require that the metal/semiconductor barrier height be reduced. In the near term, the doping and contact shunting processes are becoming increasingly interdependent, resulting in a complex materials science problem for which innovative integrated CMOS-compatible solutions are required. Thus, the interim extension of conventional salicided source/drain structures will challenge process capability and manufacturability of incumbent methods for producing doped contact regions.

Contact shunting potential solutions include progressively scaling of the incumbent salicide process; selectively depositing titanium silicide; the siliciding of deposited sacrificial silicon; and the selective deposition of an alternate low resistivity contact metal. Ultimately, a robust contact process will require

development of innovative new device structures in which the source and drain contact regions are elevated with respect to the channel. However, current methods under investigation for producing elevated contact structures that may be needed for the sub-100 nm nodes are still in the research stage and are not yet production qualified.

POLY DOPING

The polysilicon gate electrode also represents a major challenge for near-term scaling. Both the effective increase in the gate dielectric thickness associated with depletion and the channel autodoping associated with boron out-diffusion from the p^+ polysilicon gate will eventually require the phase-out beyond the 70 nm technology node of the currently used dual-doped polysilicon gate material. Potential solutions are shown in Figure 20. Near term potential solutions to the gate electrode problem include improvements in the doped polycide gate stack. The boron penetration resistance of the gate dielectric is of great importance; this may favor silicon nitride as a gate dielectric solution. The development of enhanced means of activating the doped polysilicon for achieving tighter control of the work function is important and has possible solutions through materials engineering such as doping the silicon with germanium to increase the activation level of the boron dopant.

CHANNEL

To maintain acceptable off-state leakage with continually decreasing channel lengths will require that channel doping levels increase to offset the degradation in short channel effects for extremely small devices. Although both vertical and lateral channel engineering can be used to improve degradation due to these effects, it will not be possible to scale threshold voltage without a large increase in off-state leakage even with the aggressive scaling of gate oxide thickness. However, if the threshold voltage is not scaled, the device performance for low supply voltages will be extremely degraded due to the large reduction in gate drive. There is no simple solution to this problem since low off-state leakage is dictated by power constraints.

Retrograde channel doping is a form of vertical channel engineering. It is used to improve short channel effects and to increase surface channel mobility by creating a low surface channel concentration followed by a highly doped subsurface region. The low surface concentration increases surface channel mobility by minimizing channel impurity scattering while the highly doped subsurface region acts as a barrier against punchthrough. To be effective, the retrograde depth must be less than the source/drain extension (SDE) depth and should transition from a low to high concentration very quickly. As source/drain junction depths are scaled, the retrograde well depth and abruptness must also be scaled.

Lateral channel engineering is also used extensively to improve device performance. Typically, lateral engineering is accomplished by angled implants into the channel region following gate patterning. The lateral implants cause an increase in doping concentrations near the SDE regions. The resulting channel profile is device size dependent. Smaller devices have higher average channel doping levels. This can be used to tailor the relationship between threshold voltage and device size to improve device performance. For lateral channel engineering to be effective, the lateral profile must vary over the length of the channel. This will become extremely difficult as channel lengths continue to scale to the sub-50 nm regime.

The scaling of both the vertical and lateral channel profiles is extremely difficult due to diffusion effects that degrade the abruptness of the profiles. These profiles must be extremely localized to maximize the effect on device performance. Transient enhanced diffusivity (TED), high concentration diffusion effects (such as BED) and thermal diffusion must all be managed to produce the required channel profiles. The need for extremely abrupt, well-defined channel profiles may require the use of epitaxial deposition in conjunction with extremely low temperature processing. Even with this added capability, circuit designers may need to trade-off high off-state leakage versus markedly lower drive currents.

ISOLATION / WELL

Increased transistor densities will cause significantly reduced n^+/p^+ spacing, resulting in the need for improved inter-well isolation and control of parasitic circuit elements. Additionally, the increasing importance of achieving dynamic control of channel potential for both p^- and n-channel devices, as well as the increasing implementation of embedded memory arrays and system-on-chip designs will drive increasing

adaptation of additional isolation structures. High energy ion implantation techniques, aided by improved understanding of point defect kinetics and better TCAD modeling, offer potential solutions to these isolation doping needs.

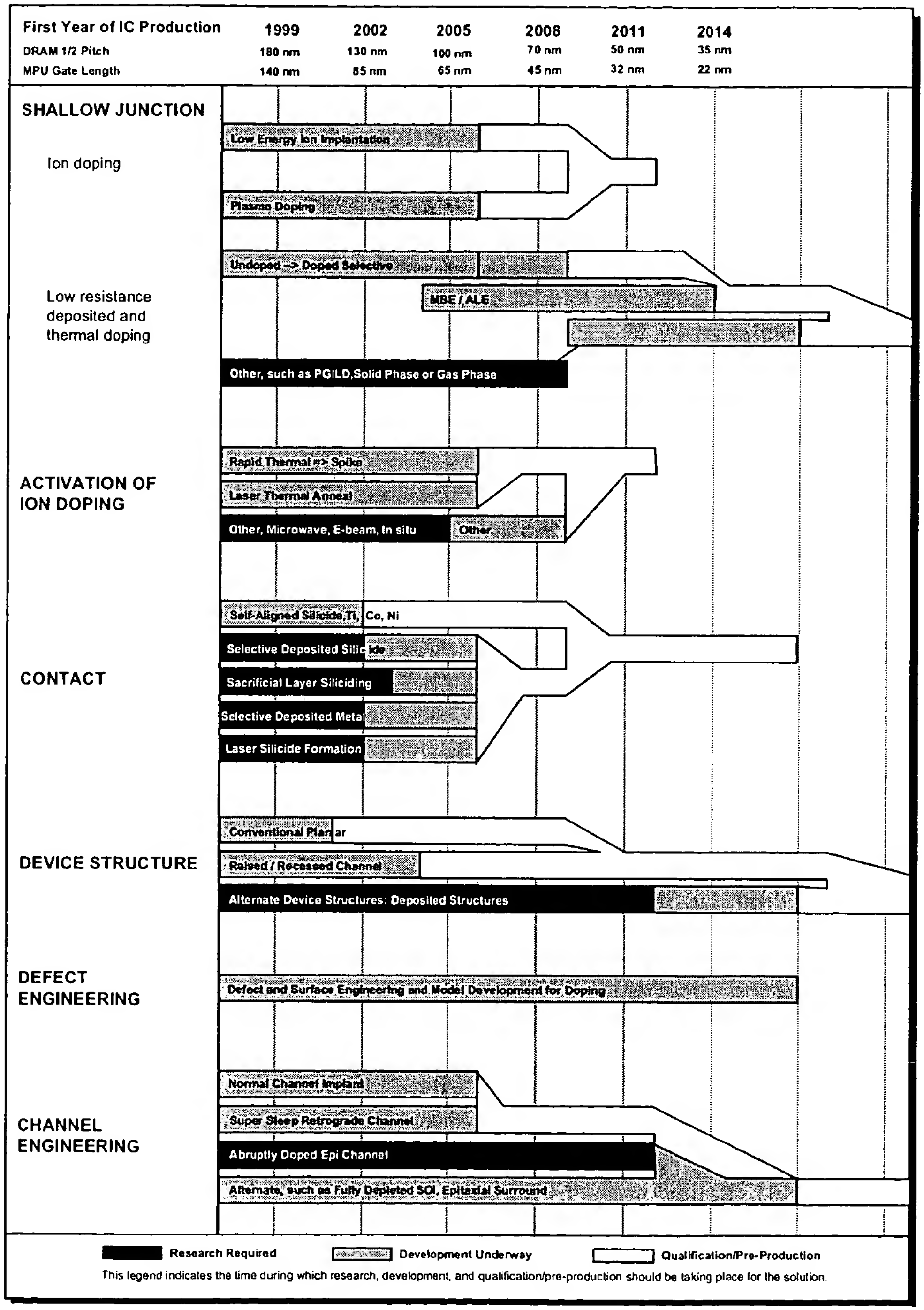


Figure 20 Doping Potential Solutions

FRONT END ETCH PROCESSING

Future challenges for etch processing are largely driven by decreasing critical dimensions (CDs) and new materials, notably metal gates, and deposited high κ dielectrics. The most challenging front end etch technical requirements are maintaining low bias and high uniformity of edge profile at continually larger wafer diameters and obtaining the required etch selectivity and etch profiles for the new materials. At the technology level where metal gates are introduced, new thinner photoresist materials with less etch resistance will be introduced. The simultaneous introduction of new gate stack materials, larger wafer diameters and new photoresists significantly compounds the difficulties associated with scaling alone. Close interaction between lithography and etch is key to achieving the CD control targets. Gate CD control requirements are provided in Tables 34a and 34b.

To preserve the CD of the etch mask, high etch selectivity is required between the mask material and the one or more underlying layers to be etched. If sufficient selectivity cannot be obtained with a photoresist mask then it may be necessary to transfer CD to a hard mask (which could also serve as an anti-reflective coating) and then use the hard mask to transfer the pattern to the underlying material. Such increase in process complexity will be necessary as the photoresist thickness is being reduced to be compatible with the decreased depth of focus in advanced lithography. Successfully transferring the pattern from the mask to the underlying material also requires the etch process to be extremely anisotropic to produce structures with near vertical sidewalls, especially for gate and sidewall spacer etch. In addition, microloading must be minimized to match etch rate and profile for both isolated and high aspect ratio dense structures.

As the linewidths shrink, the presence of line edge roughness (LER) is becoming increasingly important to CD control and the definition of CD itself. LER has its origin in both lithography and etch. The choice of gate material, photoresist composition and etch chemistry all contribute to the magnitude of such a linewidth uncertainty. To set a control target for this quantity, the impact of LER to device performance has to be understood. The associated measurement methodology and equipment will also have to be developed.

Decreasing linewidth with alternative gate dielectric material(s) also imposes strict front end etch requirements in the areas of defect density (etch block) and plasma damage. To meet future defect density requirements the plasma processes and etch tools must generate considerably fewer and smaller particles. Improvements will be required in the etch chemistries, the control of deposition in the etch chamber, and the cleaning procedures used for the etch chamber. Plasma etch tool design and plasma processing conditions must be developed that do not cause charging damage.

New materials present a challenge since several front end etch processes require extremely high selectivity between subsequently etched layers. For example, polysilicon gate etching requires high selectivity between the polysilicon gate electrode and the gate dielectric to allow an adequate over-etch of the polysilicon without etching into the silicon substrate. Measurement of the small remaining oxide thickness after gate etch clean processing is an area that is in need of development. In the future, high etch selectivity will be required between new lower resistivity metal gate electrodes and higher dielectric constant gate dielectrics. New etch chemistries and process conditions may be needed to etch these new materials with the required etch selectivity and feature profile. The unknown plasma damage susceptibility of these new gate dielectrics presents a new challenge to plasma etch process design.

Alternative gate dielectric materials will require development of multi-step etch processes where the majority of the bulk material is removed in a main etch step followed by completion in an over-etch step. It is highly desirable to be able to determine the amount of material remaining prior to completion of the main etch through the use of interferometry or a similar sensing technique so that a pre-emptive endpoint can be determined. To complete the processing, a highly selective non-damaging process is required.

Sidewall spacer width control presents another challenge to plasma etch. The spacer width and its sensitivity to over-etch is governed by the profile of the gate electrode, the thickness control and conformality of the space dielectric deposition as well as the anisotropy of spacer etch. An accurate assessment of the scalability of the sidewall spacer from an etch perspective is hindered by the limited process control data available. A non-destructive spacer width measurement metrology will have to be developed. Improved control of all the factors that can affect the spacer width, such as spacer dielectric deposition and etch endpoint detection, will be needed to ensure reproducibility.

Plasma damage will continue to be a major concern as reactors are designed for higher density processing to meet gate dielectrics scaling, and larger diameter wafer processing requirements. Furthermore, it is unknown if plasma charging damage can be avoided through the 70 nm technology node since the gate dielectric for that node is not yet defined. If plasma charging damage cannot be avoided in plasma etch tools then chemical downstream etching (CDE) or neutral stream etching must be pursued as an option. However, considerable research and development is required to build a large area chemical downstream etch tool that has sufficiently high directed neutral kinetic energy to satisfy the anistropic etch requirements of the future. Gate etch potential solutions are summarized in Figure 21. If CDE becomes the method of choice to minimize damage, then the source technology should be able to be integrated on a cluster platform either within a separate etch chamber or *in situ*.

The DRAM specific challenges for etch are in the formation of storage capacitors, especially the advanced high capacity stack capacitor structures. Such structures often employ new high κ dielectrics (such as Ta_2O_5, BST) and new metal electrodes such as materials (Pt, Ru, RuO_2). As in the case of advanced gate stacks, new etch chemistries will have to be developed. Profile control is not as stringent as in a transistor gate structure, but the 3D capacitor structure or much larger electrode thicknesses present high packing density defectivity control challenges. The other key area associated with stack capacitors is the formation of high aspect ratio contacts. To achieve high packing density, the expected size of the rectangular contact would be <0.1 µm and the aspect ratio would be >10. The development of a self-aligned high aspect ratio contact etch process and a sufficient post-etch cleaning method will be critical. The ability to maintain CD and selectivity control without etch stopping and damage to the shallow junctions will be key technical challenges.

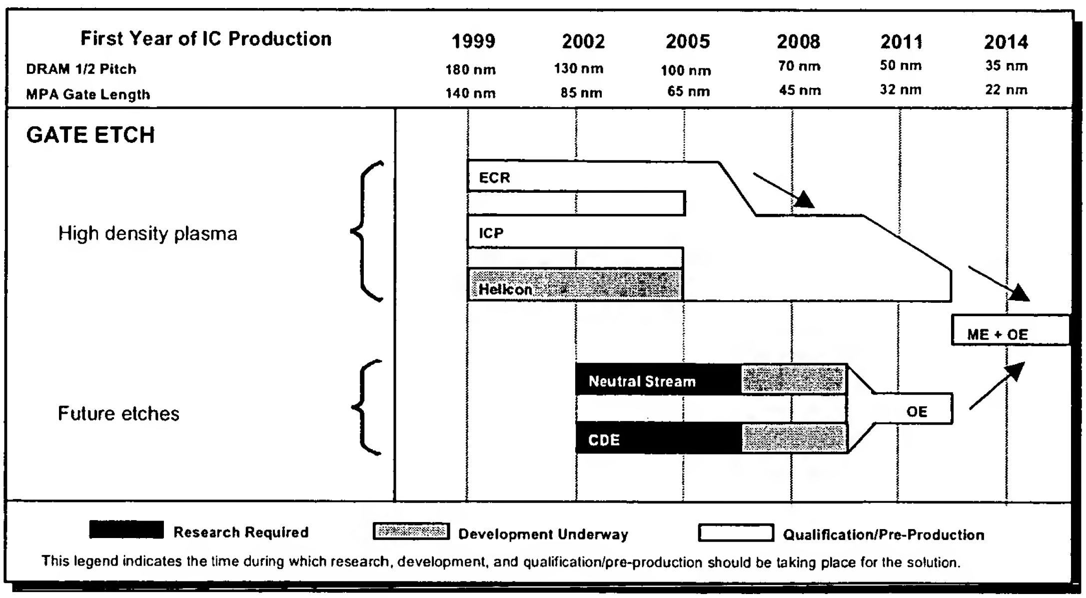


Figure 21 Front End Etch Potential Solutions

DRAM STACK CAPACITORS

In the giga-bit era, DRAM capacitor technology faces new challenges of introducing new storage capacitor dielectric and electrode materials. Table 35 summarizes the technology requirements for the DRAM stack capacitor. The cell size of DRAM is being scaled down faster than the general design rule and an area of at least $8F^2$ (F: Feature Size) will be realized at the 130 nm generation, which is the smallest cell size with a folded bit line architecture. Each of the target values in Table 35 is based on the assumption that a cell capacitance retains at least 25fF/cell to assure stable circuit function and sufficient soft-error immunity. Up to the mega-bit era, nitride/oxide dielectric films with a 3-dimensional polysilicon capacitor structures have

been used to keep the cell capacitance sufficiently high for sensing and noise immunity. For the 180 nm node, a poly-silicon bottom electrode and a 3D capacitor cell with high κ dielectric and metal counter-electrode is needed. Ta_2O_5 with a dielectric constant of 22 is a promising dielectric choice for this node. However, it is difficult to keep this cell capacitance value using these materials and structure beyond the 180 nm node. Thus, alternative high κ dielectrics are most likely to be introduced beyond this technology node. Ta_2O_5 is one of the most promising dielectrics with a dielectric constant of about 50.

Table 35 DRAM Stack Capacitor Films Technology Requirements

YEAR TECHNOLOGY NODE	*1999* *180 nm*	*2002* *130 nm*	*2005* *100 nm*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
DRAM capacity [A]	1G	(3G)	(8G)	(24G)	64G	(192G)
Cell area/chip size	69.6%	70.7%	71.7%	72.4%	72.9%	73.3%
Total cell area (cm^2)	2.8	3.3	3.8	4.5	5.2	6.3
DRAM chip size at introduction (cm^2)	4.0	4.6	5.3	6.3	7.1	8.6
Cell size factor "a" [B]	8.0	6.0	4.4	3.6	3.0	2.5
Cell size [μm^2] [C]	0.26	0.10	0.044	0.018	0.0075	0.0031
	=0.36×0.72	=0.26×0.39	=0.2×0.22	=0.14×0.13	=0.1×0.08	=0.07×0.04
Storage node size [μm^2] [D]	0.097	0.034	0.012	0.0039	0.0013	0.0003
	=0.18×0.54	=0.13×0.26	=0.1×0.12	=0.07×0.06	=0.05×0.03	=0.035×0.01
Capacitor - Structure - Dielectric material	Cylinder MIS Ta_2O_5	Pedestal MIM Ta_2O_5 [Note U]	Pedestal MIM BST	Pedestal MIM epi-BST	Pedestal MIM ???	Pedestal MIM ???
Dielectric constant	22	50 [Note U]	250	700	1500	1500
SN height H [μm]	0.95	0.84	0.71	0.42	0.28	0.35
Cylinder factor [E]	1.5	1.0	1.0	1.0	1.0	1.0
Roughness factor	1.0	1.0	1.0	1.0	1.0	1.0
Total capacitor area [μm^2]	2.20	0.69	0.32	0.11	0.04	0.031
Structural coefficient [F]	8.5	6.8	7.4	6.2	5.8	10.1
t_{eq} at 25fF [nm] [G]	3.0	0.95	0.45	0.15	0.060	0.043
t_{phy} at 25fF [nm] [H]	11.5	12.2	28.7	27.2	23.0	16.4
A/R of SN (OUT) for cell plate deposition [I]	6.0	8.0	16.7	26.9	68.8	162.7
HAC diameter [μm] [J]	0.22	0.16	0.12	0.08	0.06	0.04
Total interlevel insulator and metal thickness except SN [μm] [K]	1.05	0.95	0.85	0.77	0.69	0.62
HAC depth [μm] [L]	2.00	1.79	1.56	1.19	0.97	0.97
HAC A/R	9.3	11.4	13.0	14.1	16.1	23.1
V_{dd} [V] [M]	1.8	1.5	1.2	0.9	0.6	0.5
Retention time [ms] [N]	128	256	512	1024	2048	4096
Leak current [fA/cell] [O]	0.527	0.220	0.088	0.033	0.011	0.005
Leak current density (nA/cm^2)	24.0	31.9	27.1	30.0	25.4	14.8

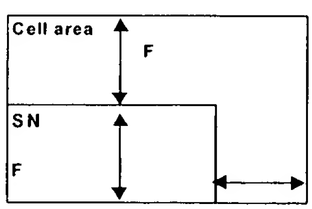
Table 35 DRAM Stack Capacitor Films Technology Requirements (continued)

YEAR	*1999*	*2002*	*2005*	*2008*	*2011*	*2014*
TECHNOLOGY NODE	*180 nm*	*130 nm*	*100 nm*	*70 nm*	*50 nm*	*35 nm*
Leak current density (nA/cm^2)	24.0	31.9	27.1	30.0	25.4	14.8
Deposition temperature [°C]	~ 500	~ 500	< 500	< 500	< 500	< 500
Film anneal temperature [°C]	~ 800	~ 750	< 750	~ 650	< 650	< 650
DRAM Gox [nm] [P]	6	5	4	3	2	1.5
C_{gate} [F/cell] [Q]	1.9×10^{-16}	1.2×10^{-16}	8.6×10^{-17}	5.6×10^{-17}	4.3×10^{-17}	2.8×10^{-17}
Wordline Rs [Ω/□] [R]	10	8.3	6.7	5.0	3.3	2.5
$C_{bitline}$ (S)	1	0.79	0.62	0.49	0.39	0.30
Bitline Rs [Ω/□] [T]	10	8.8	9.0	6.9	5.3	4.0

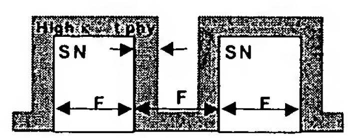
Solutions Exist   *Solutions Being Pursued*   *No Known Solutions*

Notes for Table 35 DRAM Stack Capacitor Requirements

[A] DRAM chip size model (Process Integration)
[B] a = (Cell size)/F^2 (F : minimum feature size)
[C] Cell size = a×F^2 (cell shorter side =2F)
[D] SN size =(a/2 -1)×F^2 (SN shorter side = F)
[E] Cylinder structure increases the capacitor area by a factor of 1.5.
[F] SC = (total capacitor area) / (Cell size)
[G] $t_{eq}=3.9\times\varepsilon_0\times$(total capacitor area)/25fF
[H] $t_{phy'} = t_{eq}\times\varepsilon_r/3.9$ If polysilicon is used as a bottom electrode. $t_{phy'} =(t_{eq}-1)\times\varepsilon_r/3.9$
[I] A/R of SN (OUT) = (SN height) / (F - 2× $t_{phy'}$)
[J] HAC diameter =1.2×F
[K] The thickness is assumed to be 1.05 µm at 180 nm. (10% reduction by each generation)
[L] HAC depth = SN height + total interlevel insulator and metal thickness
[M] Process Integration chapter Table 28 minimum logic V_{dd} (V) (desktop)
[N] DRAM retention time (Process Integration)
[O] (Sense limit×C×V_{dd}/2) / (retention time × MARGIN) (sense limit=30% leak, MARGIN=100)
[P] FEP Table 35—equivalent oxide thickness T_{ox}(nm) DRAM
[Q] Gate area =F^2
[R] Wordline Rs is assumed to be 10 Ω/□ at 180 nm. (wordline R)×(C_{gate}) is constant at same WL length.
[S] $C_{bitline}$ proportional to $F^{2/3}$) (relative value) [28]
[T] Bitline Rs is assumed to be 10 Ω/□ at 180 nm. (bitline R)×($C_{bitline}$) is constant when the number of BL cells about 1.4 ×/BL.
[U] See Reference [29]



(C)(D) Cell area and Projected SN area



(I) A/R of SN (OUT)

[28] A. Nitayama et al., "Future Directions for DRAM Memory Cell Technology," *IEDM 1998, Technical Digest*, Dec. 1998, pages 355-358.

[29] Koichi Kishiro et al., "Structure and Electrical Properties of Thin Ta2O5 Deposition on Metal Electrodes," *Jpn. J. Appl. Phys.* vol. 37, (1998) pages 1336-1339.

For the conventional cell structure with polysilicon as the bottom electrode of the storage node (Metal Insulator Silicon (MIS) structure), the effective dielectric constant of Ta_2O_5 decreases to about 22 due to the oxide layer grown at the interface during thermal annealing of the capacitor dielectric. On the other hand, if metals such as Ru and Pt are used as the bottom electrode of the storage node, Ta_2O_5 keeps its intrinsic dielectric constant of more than 50 because the metal electrode is free from oxidation and can provide a highly oriented crystal microstructure.[29] Therefore, a Metal Insulator Metal (MIM) structure is required at the 130 nm node. Refer to Figure 22.

In the 130 nm node, metals or conductive metallic oxides such as Pt, Ru, RuO_2 and IrO_2 have to be used as a storage node bottom electrode primarily to improve the immunity to oxidation and provide a template for preferred microstructure. From the thermal budget viewpoint, these dielectric materials should be deposited at low temperature by using CVD based methods. However, relatively higher temperature annealing in oxygen ambient will most likely be required. Lowering the process temperature is needed if metals are used for bit lines to minimize device performance degradation.

Reducing leakage current at lower processing temperatures is another difficult challenge for DRAM capacitor technology for the 130 nm node and beyond. Careful process integration is required to prevent capacitor film degradation caused by plasma damages and the oxide reducing processes used in the BEOL.

At the 100 nm node, a higher κ material such as BST with a dielectric constant of about 200–250 will be needed in order to reduce the aspect ratio of the storage node and the High Aspect Contact (HAC) hole.

At and beyond the 100 nm node, cell size has to be reduced below $5F^2$ to keep a reasonable chip size. New cell architecture such as an open bit line cell, a cross-point cell, and even a multi-state circuit will be required. At the 70 nm node, research and development for new materials such as epi-BST with a sufficiently high dielectric constant will be required. However, even if such new materials are successfully developed, an upper electrode deposition process for a very high aspect ratio storage node may limit the capacitor integration. Therefore, in addition to the material and process development, new memory cell concepts such as a gain cell architecture will be required at the 70 nm node and beyond.

At the 50 nm node and beyond, a dielectric constant of 1500 is needed. However, there is no known material with such a high κ value. Thus innovation of "super high κ" value is called for or a new device structure that uses ferroelectrics in the DRAM context may be attempted.

It is noted that retention times become "red" at and at below the 70 nm node, however cell leakage currents are adequately met. Thus silicon diffusion limited reverse bias leakage becomes a fundamental limitation for retention time, indicating the potential need for SOI substrates for 70 nm DRAM and below.

The process technology requirements for the System-on-a-Chip (SoC) with embedded DRAM present many variations depending on the ratio of logic area and memory area. Cell capacitance requirements for embedded DRAM may be smaller than those for standalone DRAM. One of the serious problems for SoC is the contact hole formation. The stack capacitor DRAM processes require relatively deep contact holes in comparison with those in logic processes. The contact hole size of DRAM has to be enlarged to minimize the hole aspect ratio. It will be difficult to achieve the same metal line pitch for the logic section using the same DRAM design rule. In the logic-based SoC, cell size expansion is needed to reduce the capacitor height and to decrease the aspect ratio of contact holes. On the other hand, in the memory-based SoC, the metal line pitch has to be adjusted so that the DRAM contact hole size may be kept large enough. In SoC, some additional break-through is required to solve this contact hole density issue.

Year	*1999*	*2002*	*2005*	*2008*	*2011*	*2014*
Technology Node	*180 nm*	*130 nm*	*100 nm*	*70 nm*	*50 nm*	*35 nm*
Upper Electrode (A)	poly-Si / TiN	TiON	metal			
High κ Dielectric	ON / Ta_2O_5		BST, STO	Epi-BST		super high κ
Bottom Electrode (A,B)	poly-Si		metal	perovskite		tbd

(A) Metal : W, Pt, Ru, RuO_2, IrO_2
(B) Perovskite : $SrRuO_3$ [30]

Figure 22 DRAM Stack Capacitor Films Potential Solutions

DRAM TRENCH CAPACITOR

Table 36 summarizes the technology requirements for DRAM trench capacitor technology. The target values are based on the assumption of a 35fF capacitance per DRAM cell. For storage nodes down to, and including the 100 nm technology node, trench capacitor technology is characterized by conventional thickness scaling of the NO capacitor dielectric, in combination with surface enhancement techniques such as bottle-shaped trenches. As a result of ground-rule shrinking, the aspect ratio (trench depth to trench width) will increase up to values of ~60 for the 100 nm technology node. It is expected that a new high κ dielectric material will not be required before the 70 nm technology node.

For embedded applications, the trench technology with its capacitor buried in the substrate, enables a planar transition between the DRAM cell array and the logic circuit. Thus, a critical thinning of individual metal lines of the multilevel metallization, or reduced lithographic resolution at the transition area is avoided. Also avoided is the need for deep, high aspect ratio contact holes. In addition, since the capacitor is processed prior to the transfer device, degradation of device performance from the capacitor-forming thermal cycle is not encountered.

The scaling of the cell area factors as a consequence of the new chip size model will require a further optimization of the layout and the areas consumed by each element of the DRAM storage cell. This implies measures such as the replacement of the conventional planar transfer device by a vertical transistor, or the reduction in storage node area by further increases in the aspect ratio of the capacitor structure. Finally, all current DRAM technologies with their lithographic defined wordline, and bitline pitch, will reach a theoretical scaling limit at a cell size of $4F^2$ given by the 2F pitch for each metal line. For smaller values, new concepts such as multi-bit circuits or multi-layer DRAMs are required. No currently known solutions exist for such fundamental changes.

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[30] N. Fukushima, et al., "Epitaxial (Ba, Sr) TiO3 Capacitors with Extremely High Dielectric Constant for DRAM Applications," *IEDM 1997, Technical Digest*, Dec. 1997, pages 257-260.

Table 36 DRAM Trench Capacitor Films Technology Requirements

YEAR TECHNOLOGY NODE	1999 180 nm	2002 130 nm	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
Storage node area, top view [(DRAM ½ pitch) ^{2}]	2	2	2	< 2	< 2	< 2
Trench structure	conventional	bottled	bottled	bottled	tbd	tbd
Trench area enhancement factor	1	1.5	2	2	1.5	1.5
Capacitor dielectric equivalent oxide thickness (nm)	4.5	3.5	3.2	1.5	1	1
Trench depth [µm], (at 35fF)	6–7	5–6	5–6	4–5	4–5	5–6
Aspect ratio (trench depth/trench width)	30–40	40–45	50–60	60–70	> 70	> 100
Upper electrode	Silicon	Silicon	Silicon	Metal	Metal	Metal
Dielectric material	NO	NO	NO	High κ	High κ	High κ
Bottom electrode	Silicon	Silicon	Silicon	Silicon	Metal	Metal

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

ENVIRONMENT, SAFETY, AND HEALTH

Key ESH concerns for Front End Processes center on development of new materials for gate dielectrics and electrodes, natural resources use (especially water), management of potential physical and chemical hazards to ensure worker protection, and optimization of processes to reduce chemical use and generation of wastes requiring abatement. New materials for 100 nm technologies and beyond (and corresponding precursors, clean techniques and etch gases) will require thorough ESH review.

The global EHS challenges affect all areas of Front End Processes. The primary chemical management strategy should be to optimize processes to maximize chemical use efficiency, including consideration of chemical throughput, waste generation, recovery of hazardous materials, and tool utilization factors. On-demand/in-situ chemical generation can contribute to improved efficiency. Energy needs (tool and facility systems) must be evaluated for new technologies. Thermal processes, wafer cleaning and exhaust ventilation are key areas for energy conservation. Installed base thermal processing could use some measurement and optimization especially in the idle stages. The measurement results would provide data for improvements in future designs. Novel heating approaches may be needed to drive further energy-efficiency. Wafer cleaning uses heated chemistries and UPW. New energy-efficient heating technologies are also needed for future generation tools. Process exhaust comprises a large portion of energy consumption. Optimizing existing exhaust systems and improving designs for future facility and tool ventilation systems would drive lower energy consumption. Worker protection measures should address potential physical (such as thermal, non-ionizing radiation, laser and robotics hazards) as well as chemical hazards, especially during equipment maintenance. Factory planning should identify ergonomic design criteria for wafer handling (especially for 300/450 mm wafers), tools, and factory layout. EHS Cost-of-Ownership (CoO) and risk assessment tools should be utilized to evaluate process improvements and identify potential risks of new materials.

ESH concerns for surface preparation focus on new clean techniques, chemical use efficiency, and consumption of water and energy. Surface prep methods will undergo fundamental changes to accommodate new materials after the 2005 time frame for expected adoption of new gate dielectrics and electrodes. There is a need for improved understanding of surface and interface science with the potential for significant reductions in chemical or water use. Front end processes use from 45% to 75% of the total ultra-pure water in a fab (depending on the number of CMP unit processes). Practically all of this water is for wafer rinsing. Therefore, water conservation should focus on developing more efficient and low-water rinse processes. However, the reduction in rinse water and the reuse of rinse wastewater are related and need to be optimized using an integrated approach. Sustainable, optimized water use strategies utilizing improved UPW production efficiency, reduced tool consumption, and efficient rinsing are being developed. However,

the energy-use impact of alternate clean or UPW production methods needs to be considered. Development of reliable sensors to speciate low-level organics is needed to mitigate the process risk of UPW recycling.

Silicon-on-insulator (SOI) materials may offer ESH advantages of fewer process step, reducing chemical, water and energy use. Transitions to larger wafers (200–300 mm; 300–450 mm) will require more chemicals, energy, and water although industry initiatives have been advanced to hold usage flat.

The evaluation of alternative higher κ materials must include thorough assessment of potential process hazards associated with both the materials and associated deposition processes. Alternate silicides (Co, Ni, others) present potential hazards requiring mitigation through engineering controls and appropriate personal protective equipment. Chemical use efficiency can be optimized through improved delivery systems and tool designs (small batch furnaces, single-wafer tools). Energy use for diffusion and implant tools and associated facility systems should be evaluated and optimized. The potential physical and chemical hazards of alternate doping technologies need to be evaluated and mitigated. Process hazards analysis tools will assist in managing hydrides, metal alkyls and laser sources.

Continued use of perfluorocompounds (PFCs) in plasma etch will necessitate near-term process optimization/increased gas utilization (such as conversion efficiency within the process). Over the longer term, alternative chemistries for PFCs that do not emit PFCs as by-products need to be developed. Changes in gate dielectric materials will drive corollary changes in etch chemistries, necessitating review of potential ESH impacts.

Table 37 Front End Processes ESH Needs and Potential Solutions

KEY AREAS	*SUMMARY OF NEEDS*	*POTENTIAL SOLUTIONS*
New high κ dielectric and gate electrode materials	ESH evaluation of new materials and deposition processes Avoid usage of Pb or other potentially toxic or bioaccumulative metals Increased chemical utilization efficiency	Utilize most ESH benign processes Identify and mitigate process hazards Need rapid ESH assessment for new materials in early stages of development Identify ESH issues with precursors for CVD or other deposition methods
Doping processes	Reduce use of hydride and halogenated chemistries Increased chemical utilization efficiency	Develop broader suite of sub-atmospheric delivery systems *In situ* hydride generation to minimize material quantity Increased segregation within tools to minimize potential exposures during tool maintenance
Surface preparation methodologies	Fundamental understanding of surface/interface process science Optimization/control to reduce chemical use Increased water use efficiency Reduced energy consumption	Reduced chemical use through optimized cleans, like cryogenic, supercritical fluids, ozone, dilute chemistries Reduced water use through increased rinse efficiency, optimized rinse sequences Low level speciation of organic by rapid sensors to reduce process risk of UPW recycling Worker protection through enclosed processes, ergonomic designs and robotics safety

Table 37 Front End Processes ESH Needs and Potential Solutions (continued)

KEY AREAS	*SUMMARY OF NEEDS*	*POTENTIAL SOLUTIONS*
Front end plasma etch	Minimize emissions of high global warming potential gases (such as PFCs) from CVD chamber cleaning and etch processes Utilize most ESH benign etch chemistries Minimize energy consumption	Optimize chamber clean and etch processes to increase utilization efficiency of PFCs Develop low CoO abatement and recycle systems for PFCs Develop lowest ESH impact alternative etch chemistries and chamber cleaning processes that do not emit high global warming potential by-products (such as PFCs) Develop predictive plasma emissions models Identify ESH issues with new etch chemistries Develop lowest ESH impact HDP etch processes that do not emit high global warming potential by-products Minimize energy consumption of HDP etch tools Measure and optimize equipment systems energy usage Minimize energy consumption of pumps for all low pressure process steps
Starting materials	Analysis of reduced process steps due to use of Silicon-on-Insulator wafers	Quantification of chemical use reduction
Thermal processes	Need continued thermal processing of wafers Need more precise, accurate and uniform heating of wafers	Optimize existing thermal processes New energy-efficient heating technologies
Heated wafer cleaning	Need heated chemistries and heated UPW for rinsing wafers	New energy-efficient heating technologies
Exhaust requirements	Exhaust for people and process protection	Measure and optimize exhaust ventilation Reduce exhaust requirements through design improvements
Wafer cleaning and rinsing	Low-water rinse processes	Novel rinse tools and techniques. Optimization of rinse sequence and duration

SUMMARY

This international roadmap has identified the end of conventional scaling for CMOS structures unless new materials and devices are introduced on an aggressive time scale. The immediate grand challenge for FEP as developed in the thermal/thin films section is the identification and introduction of new silicon compatible high κ dielectric and electrode materials for formation of the gate stack by the year 2005. Although these new materials will not guarantee scaling to the end of the present Roadmap, where new device structures will be needed, they will permit the realization of two nodes on the Roadmap. In addition, the knowledge base that will be developed by introducing these new silicon compatible materials will accelerate the learning curve for the introduction of new materials that will likely be required to realize the needed new device concepts for future scaling.

New high κ dielectric and associated electrode materials are also needed for DRAM storage capacitors, in order to permit continued scaling of the DRAM storage node area. In the long term, continued memory scaling may require new storage concepts to replace the traditional stacked or trench storage capacitor structures now in use.

In the doping area, on a near term basis (<2005) the realization of ultra-shallow abruptly doped junctions is needed, as is the achievement of very high non-equilibrium degrees of dopant activation in the contact junctions and in the dual-doped polysilicon gate electrodes. The fulfillment of these objectives will allow continued near- term device scaling in conjunction with the incumbent silicon oxynitride gate dielectric materials. In the longer term, an important challenge is the achievement of elevated contact structures with

high degrees of dopant activation in the low thermal budget regime required for CMOS integration of high κ gate stacks having dual metal gate electrodes.

In the etch area, future challenges are largely driven by decreasing critical dimensions (CDs) and new materials, notably metal gates and deposited high κ dielectrics. The most challenging FEP etch technical requirements are maintaining low CD bias and high CD uniformity at continually larger wafer diameters and obtaining the required etch selectivity and etch profiles for new materials. In addition, line edge roughness is expected to play an increasingly important role in overall transistor performance.

In the surface preparation area, the near-term challenges include the continued cost-effective reduction in post-clean particle, elemental, and structural defects. In the long term, the challenges include the integration of both aqueous and dry surface preparation techniques with the new process architectures required for CMOS integration of the required new high κ elevated contact devices.

Starting materials faces the challenge of achieving future cost-effective large area silicon substrates, as well as alternative substrate materials such as SOI that may be required to achieve the continued performance and productivity gains historically associated with Moore's law.

These new materials and processing requirements have been identified and documented here. The required process development and manufacturing integration needs present a challenge that will require the melding of efforts by university, national laboratory, semiconductor device, and semiconductor equipment industries. This is especially challenging when placed in the context of SoC. Here the challenge is further complicated by the necessity to integrate logic, embedded memory (such as DRAM, FeRAM, Flash), analog, RF, and other device technologies. The newly developed materials and processes must be compatible with SoC.

In the longer term (>2008), the work documented here anticipates that the continued scaling of the MOS transistor while still possible, will yield a device that is no longer capable of complying with the anticipated low voltage high speed IC chip requirements. Scaling is anticipated to come to an end, dictated by fundamental physical limits. Continued chip level scaling to the fundamental physical limits will require the development of innovative device concepts. It is further anticipated that the materials knowledge base developed in the interim will greatly expand the arena in which the invention of such new device concepts may take place.

In conclusion, new materials and processes are not the total solution to the future, but they will be required no matter what the approach. The industry has been able to squeeze the best out of a knowledge base developed during the past century. However, that knowledge base is limited and the time has come when new knowledge is needed and new solutions must be developed and engineered. In the area of front end processing, new resources will be required on an aggressive time scale to meet the forthcoming challenges. The challenges presented here are just that—*challenges*. Although fundamental limits are being approached for the materials and devices currently used, these same limits may not apply to new materials and devices.

High-risk approaches need to be combined with evolutionary approaches and the development of new knowledge to meet the challenge. This will require a partnership between the industry, universities, and research institutes on an international scale.

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS
1999 EDITION

LITHOGRAPHY

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LITHOGRAPHY

SCOPE

Lithography continues to be the key enabler and driver for the semiconductor industry. The growth of the industry has been the direct result of improved lithographic resolution and overlay across increasingly larger field sizes. Lithography is also a significant economic factor, currently representing over thirty-five percent of the chip manufacturing cost. In addition, it is a technology with heavy global interdependence for equipment and materials. Significant investments in research and development (R&D) and commercialization will be required to improve the infrastructure of this vital technology and to maintain industry growth.

The key elements of the lithography infrastructure include:

- Exposure equipment
- Resist materials and processing equipment
- Mask making, mask equipment and materials
- Metrology equipment for critical dimension (CD) and overlay control.

This chapter provides a 15-year roadmap defining lithography difficult challenges, technology requirements, and potential solutions for each of these elements. Additionally, the chapter defines the Lithography Technology Working Group (TWG) interaction with and dependencies on the crosscut TWGs for Environment, Safety, and Health (ESH); Defect Reduction; Metrology; and Modeling and Simulation.

Optical lithography continues to be the mainstream technology for the industry and is currently being used in production by leading-edge, high-volume factories at 180 nm design rules. Extensions of optical technology are being used to support 130 nm product and process development. Resolution enhancement techniques (RET) used for optical extensions include off-axis illumination (OAI), phase shifting masks (PSM) and optical proximity correction (OPC). In addition to RET, wavelength reductions (193 nm→157 nm) and increasing numerical aperture projection lenses are being pursued to extend the life of optical lithography. While the industry momentum is behind optical extensions to 100 nm, the key challenge will be maintaining an adequate and affordable process latitude (depth of focus/exposure window) necessary for 10 percent (3 sigma) post-etch CD control.

Advanced technologies, such extreme ultraviolet lithography (EUV), X-ray lithography (XRL), electron projection lithography (EPL), and ion projection lithography (IPL) have moved from the R&D phase into commercial development for applications down to 35 nm. The cost to develop a single total system solution through to a commercially available tool and infrastructure is expected to approach one billion dollars. This high cost necessitates a narrowing of the options in the near future to ensure a manufacturing solution on a timely basis. Achieving a global consensus on an affordable post-optical technology is the grand challenge for lithography.

The technology complexities and magnitude of investments in the future require a new global model for research, development, and commercialization. While lithography development is complex and expensive, the *leverage it provides is essential to the continued growth of the semiconductor industry.*

DIFFICULT CHALLENGES

The ten most difficult challenges to maintaining the industry productivity improvements are shown in Table 38. The five difficult challenges down to the 100 nm node include:

- Optical mask fabrication with resolution enhancement techniques (RET) for ≤130 nm and post optical mask fabrication
- Lithography technology consensus (193 nm, 157 nm, NGL)
- Cost control and return on investment (ROI)
- Gate CD control improvements
- Overlay improvements

Below 100 nm, the five difficult challenges are:

- Mask fabrication and process control
- Metrology and defect inspection
- Cost control and return on investment (ROI)
- Gate CD control improvements
- Overlay improvements and measurements

Mask-making capability and cost escalation have become the major limiter to lithography progress. With the roadmap acceleration over the past three years, the mask industry has fallen behind the requirements of the chipmakers. Mask equipment and process capabilities for complex OPC and PSM are just becoming available for the 180 nm node production requirements. These capabilities are being pushed beyond their limits for 130 nm to 100 nm development. Mask processes for advanced technologies (157nm, XRL, EUV, EPL, and IPL) are in research and development.

Industry consensus on the post-optical technologies remains a difficult challenge, and with the emergence of 157 nm technology the application may be pushed below 100 nm.

Overlay and CD improvements have not kept pace with resolution improvements. The estimates for machine to machine overlay appear to plateau around 30 nm. This will be inadequate for ground rules less than 100 nm. Overlay and CD control over large field sizes will continue to be a major concern for sub-100 nm lithography. Overlay requirements are among the most difficult technical challenges in lithography. Advances in stage technologies, environmental controls, interferometers, lens distortion, and alignment systems will be needed for sub-65 nm overlay.

The gate CD control requirements for the 130 nm node and below are also among the most difficult challenges. Advances in process control, resist materials, line edge roughness (LER) and metrology will be necessary to achieve less than 10 nm (3 sigma) CD control.

Table 38 Lithography Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥ 100 nm BEFORE 2005	*SUMMARY OF ISSUES*
Optical mask fabrication with resolution enhancement techniques for ≤ 130 nm and post-optical mask fabrication	Development of commercial mask manufacturing processes to meet requirements of Roadmap options (such as 157 nm substrates and films; defect free multi-layer substrate or membranes) Development of equipment infrastructure (writers, inspection, repair) for relatively small market
Lithography technology consensus (193 nm + RET, 157 nm, NGL)	Narrowing of Roadmap options for 100–50 nm nodes. Achieving global consensus among technology developers and chip manufacturers
Cost control and return on investment (ROI)	Achieving constant/improved throughput with larger wafers Development of cost-effective resolution enhanced optical masks and post-optical masks including an affordable ASIC solution, such as low costs masks. Achieving ROI for industry (chipmakers, equipment and material suppliers, and infrastructure) on large investments necessary for Roadmap acceleration, especially single node solutions at 100 nm and below.
Gate CD control improvements	Development of processes to control minimum feature size to less than 7 nm, 3 sigma
Overlay improvements	Development of new and improved alignment and overlay control methods independent of technology option
FIVE DIFFICULT CHALLENGES < 100 nm BEYOND 2005	
Mask fabrication and process control	Development of commercial mask manufacturing processes to meet requirements of Roadmap options (such as 157 nm substrates and films; defect free multi-layer substrate or membranes) Development of equipment infrastructure (writers, inspection, repair) for relatively small market Development of mask process control methods to achieve critical dimension, image placement, and defect density control below 100 nm nodes
Metrology and defect inspection	R&D for critical dimension and overlay metrology, and patterned wafer defect inspection for defects < 40 nm
Cost control and return on investment (ROI)	Development of innovative technologies, tools, and materials to maintain historic productivity improvements Achieving constant/improved throughput with post-optical technologies Achieving ROI for industry (chipmakers, equipment and material suppliers, and infrastructure) on large investments necessary for Roadmap acceleration, especially single node solutions at 100 nm and below.
Gate CD control improvements	Development of processes to control minimum feature size to less than 5 nm, 3 sigma, and reducing line edge roughness
Overlay improvements and measurements	Development of new and improved alignment and overlay control methods independent of technology option

LITHOGRAPHY TECHNOLOGY REQUIREMENTS

The lithography roadmap needs are defined in the following tables:

- Lithography Requirements (Table 39)
- Resist Requirements (Table 40)
- Mask Requirements (Table 41)

The lithography requirements table has been expanded to focus on the unique needs of DRAMs, MPUs and ASIC products. A study group, chartered by the Roadmap Coordinating Group (RCG), recommends new chip sizes for all product types that greatly reduce the long-term maximum chip size. These new chip sizes afford significant relief for lithography tools and masks. There is a strong financial incentive for semiconductor manufacturers to maintain the smallest possible chip sizes, and it is desired to hold the chip size constant over the timeframe of the ITRS outlined in this document. Detailed analysis by the study group combined with inputs from other experts around the world suggests the most likely rate of growth in chip size is 20% every four years, or a just under 5% per year. Prior versions of the Roadmap projected a growth rate of 40% every three years, or about 12% per year. The new lower growth rate has been reflected in Table 39.

The chip size growth is particularly important to the strategy for photolithography tools. Current 5× steppers in widespread use have a field size of 22 mm × 22 mm and current 4× scanners in widespread use have a field size of 25 mm × 32 mm. As the feature size requirements push the extreme limits of optical lithography it is important to keep the optical imaging field size as small as possible to allow affordable exposure tools and masks. A considerable interest has arisen in the past two years in increasing the reduction ratio of the exposure systems in order to provide relief to the difficult challenge of making masks.

Based on the new chip size growth model there is considerable opportunity to maintain both the current scanner field size and the current 152 mm × 152 mm mask format for at least 10 years. There is the potential for other solutions such as larger reduction ratios and smaller fields for some classes of applications, but this does not appear to provide a general solution beyond 2002.

Advanced deep ultraviolet (DUV) resists at 248 nm are in manufacturing with resolution capabilities down to 150 nm. Initial 193 nm resists are commercially available for development at 130 nm to 100 nm. In addition, resists are now being developed for specific levels to optimize response and manufacturing robustness.

The mask requirements table has also been expanded to include the mask error factor (MEF) needs for lower resolution constant factors (k_l). Advanced non-optical, next generation lithography (NGL), requirements are also defined. Continuous improvements in mask making technology (mask writers, inspection, repair, and substrates) are essential to support the technical and manufacturing needs of optical lithography below 180 nm. Mask inspection requirements will become more aggressive as optical lithography pushes to lower resolution constant factors (k_l). Meeting requirements for allowable sizes of hard and soft defects becomes an increasing concern at later nodes in the Roadmap. In the short term, small mask regions with phase or transmission errors are producing more soft defects in DUV lithography. Detection and repair of such small defects will be major challenges. Because advances in detection and repair capabilities will probably not keep pace with scaling requirements, we must reduce the number of defects created during mask manufacturing. In addition, significant improvements will be necessary for all non-optical approaches. Developing substrates with required mechanical properties and meeting patterning tolerances are challenges for masks used in non-optical lithography. Significant development of both materials and processes is necessary. In addition, methods to maintain non-optical masks with no printable defects in the same way a pellicle does for optical lithography need to be developed. Also, solutions for rapidly growing data volumes need to be developed, especially for optical proximity correction.

Cost containment and reduction will require a total systems approach that includes exposure tool, mask, resist, and metrology. Cost projections and cost targets are diverging in the sub-180 nm resolution regime. Mask cost escalation is becoming especially prohibitive for low volume applications, such as ASICs. Higher yielding processes and more productive equipment are keys to restraining the growth of mask cost. Development of solutions to pattern below 130 nm according to the time scale of Figure 23 requires resources beyond the funds allocated to them today. *Additional funding to resolve this issue is vital.*

Table 39a Lithography Technology Requirements—Near Term

YEAR *TECHNOLOGY NODE*	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*	*DRIVER*
DRAM								
Half pitch (nm)	180	165	150	130	120	110	100	
Contacts (nm)	200	185	170	150	145	140	130	
Overlay (nm, mean + 3 sigma)	65	58	52	45	42	38	35	
CD control (nm, 3 sigma, post-etch)	18	17	15	13	12	11	10	
MPU								
Half pitch	230	210	180	160	145	130	115	
Gate length (nm, in resist)	140	120	100	90	80	70	65	
Gate length (nm, post-etch)	140	120	100	90	80	70	65	
Contacts (nm, in resist)	230	210	180	160	145	130	115	
Gate CD control (nm, 3 sigma, post-etch)	14	12	10	9	8	7	6	
ASIC (SoC)								
Half pitch	230	210	180	160	145	130	115	
Gate length (nm, in resist)	180	165	150	130	120	110	100	
Gate length (nm, post-etch)	180	165	150	130	120	110	100	
Contacts (nm, in resist)	230	210	180	160	145	130	115	
Gate CD control (nm, 3 sigma, post-etch)	23	21	19	16	15	13	12	
Chip Size								
DRAM								
Introduction	400	—	438	—	480	—	526	
Sample (+2 years)	230	—	252	—	276	—	302	
Production (+4 years)	132	—	145	—	159	—	174	
Ramp (+6 years)	74	—	83	—	91	—	100	
MPU Cost Performance								
Introduction	340	—	340	—	372	—	408	
Ramp (+2 years)	170	—	170	—	214	—	235	
MPU High Performance								
Ramp (+2 years)	450	—	450	—	567	—	622	
ASIC/SoC								
Dependent on design up to the maximum field size at ramp	800	800	800	800	800	800	800	
Additional Requirements								
Minimum feature size for development (nm)	90	80	70	65	55	50	45	
Minimum field area (mm^2) DRAM introduction.	400	—	438	—	480	—	526	1 chip
Minimum field area (mm^2) DRAM production (year 4)	264	—	290	—	318	—	348	2 chips
Minimum field area (mm^2) MPU	450	—	450	—	567	—	622	1 chip
Depth of focus (μm)	0.7	0.7	0.7	0.6	0.6	0.6	0.5	
Mask size (mm, square optical/diameter non-optical)	152	152	152	152	152	152	152/200	
Wafer size (mm, diameter)	200	200	300	300	300	300	300	

Note: The dates in this table are the year of first product shipment of integrated circuits from a manufacturing site with volume exceeding 10,000 units. Exposure tools, resists and masks for manufacturing must be available one year earlier. Development capability must be available 2–3 years earlier.

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 39b Lithography Technology Requirements—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
DRAM				
Half pitch (nm)	70	50	35	
Contacts (nm)	100	70	50	
Overlay (nm, mean + 3 sigma)	25	20	15	
CD control (nm, 3 sigma, post-etch)	7	5	4	
MPU				
Half pitch	80	55	40	
Gate length (nm, in resist)	45	30	20	
Gate length (nm, post-etch)	45	30	20	
Contacts (nm, in resist)	80	55	40	
Gate CD control (nm, 3 sigma, post-etch)	4	3	2	
ASIC (SoC)				
Half pitch	80	55	40	
Gate length (nm, in resist)	70	50	35	
Gate length (nm, post-etch)	70	50	35	
Contacts (nm, in resist)	80	55	40	
Gate CD control (nm, 3 sigma, post-etch)	7	5	4	
Chip Size (mm^2)				
DRAM				
Introduction	—	691	—	
Sample (+2 years)	—	398	—	
Production (+4 years)	—	229	—	
Ramp (+6 years)	—	131	—	
MPU Cost Performance				
Introduction	—	536	—	
Ramp	—	308	—	
MPU High Performance				
Ramp (+2 years)	—	817	—	
ASIC/SoC				
Dependent on design up to the maximum field size at ramp	800	800	800	
Additional Requirements				
Minimum feature size for development (nm)	33	23	16	
Minimum field area (mm^2) DRAM introduction	—	691	—	1 chip
Minimum field area (mm^2) DRAM production (year 4)	—	458	—	2 chips
Minimum field area (mm^2) MPU	—	817	—	1 chip
Depth of focus (μm)	0.5	0.5	0.5	
Mask size (mm, square optical/diameter non-optical)	152/200	152/200	152/200	
Wafer size (mm, diameter)	300	450	450	

Note: The dates in this table are the year of first product shipment of integrated circuits from a manufacturing site with volume exceeding 10,000 units. Exposure tools, resists and masks for manufacturing must be available one year earlier. Development capability must be available 2–3 years earlier.

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 40a Resist Requirements—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
Resist meets lithography requirements for resolution and CD control (nm, 3 sigma)	13	11	9	8	7	7	6
Resist thickness (μm, imaging layer)*	0.54–0.72	0.50–0.66	0.45–0.60	0.39–0.52	0.36–0.48	0.33–0.44	0.3–0.4
Ultra thin resist thickness (μm)**	—	—	—	—	0.15–0.10	0.15–0.10	0.15–0.10
Post-exposure bake sensitivity (nm/°C)	5	4	4	3	3	2	2
Backside particles (particles/m² @ critical size, nm)	3000 @ 200	3000 @ 200	2500 @ 200	2000 @ 200	2000 @ 200	2000 @ 200	2000 @ 100
Other requirements	- Need for positive or negative resist will depend on the critical feature density - Slope should be 90 +0–2 degrees - Thermal stability should be in the range of 130–150°C - Etch selectivity should be comparable to or exceed polyhydroxystyrene (PHOST) - Strippability with no detectable residues - Airborne amine contamination ≤ 1000 pptM - Ionic/metal contaminants ≤ 5 ppb						

Table 40b Resist Requirements—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
Resist meets lithography requirements for resolution and CD control (nm, 3 sigma)	4	3	2
Resist thickness (μm, imaging layer)*	0.21–0.28	0.15–0.20	0.11–0.14
Ultra thin resist thickness (μm)**	0.15–0.10	0.15–0.10	0.15–0.10
Post-exposure bake sensitivity (nm/°C)	2	1	1
Backside particles (particles/m² @ critical size, nm)	2000 @ 100	2000 @ 100	2000 @ 100
Other Requirements	- Need for positive or negative resist will depend on the critical feature density - Slope should be 90 +0–2 degrees - Thermal stability should be in the range of 130–150°C - Etch selectivity should be comparable to or exceed polyhydroxystyrene (PHOST) - Strippability with no detectable residues - Airborne amine contamination ≤ 1000 pptM - Ionic/metal contaminants ≤ 5 ppb		

Exposure Dependent Requirements

Exposure technology	*Sensitivity*
248 nm	20–50 mJ/cm²
193 nm	10–20 mJ/cm²
157 nm	~ 10 mJ/cm²
Extreme ultraviolet	5–10 mJ/cm²
E-beam projection	5–10 μC/cm² @ 100 kV***
E-beam direct write	1–5 μC/cm² @ 50 kV***
Ion-beam projection	0.2–2.0 μC/cm²

* *Resist thickness determined by aspect ratio range of 3:1 to 4:1.*
** *Lower limit for ultra thin resist (UTR) determined by opacity to exposure source.*
*** *Linked with resolution.*

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 41a Mask Requirements—Near Term

YEAR *TECHNOLOGY NODE*	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*	
Wafer minimum half pitch (nm) [A]	180	165	150	130	120	110	100	
Wafer minimum isolated line (nm, in resist) (A)	140	120	100	90	80	70	65	
Wafer minimum contact hole (nm, in resist)	200	185	170	150	145	130	115	
Lithography technology	Optical	Optical	Optical	Optical	Optical	Optical	Optical	NGL
Magnification [B]	4	4	4	4	4	4	≥4	≥4
Mask minimum image size (nm) [C]	560	480	400	360	320	280	260	260
Mask OPC feature size (nm) [D]	280	240	200	180	160	140	130	—
Image placement (nm, multi-point) [E]	39	35	31	27	25	23	21	21
CD uniformity (nm, 3 sigma) [F]								
Isolated lines (MPU gates)	16	14	12	10/20*	9/18*	8/16*	7/14*	10
Dense lines (DRAM half pitch)	24	21	17	13/26*	12/24*	11/22*	10/20*	16
Contact/vias	24	21	17	14	13	12	11	18
Linearity (nm) [G]	28	26	23	20	18	16	14	
CD mean to target (nm) [H]	14	13	12	10	9	9	8	
Defect size (nm) [I]	144	132	120	104	96	88	80	
Data volume (GB) [J]	16	24	40	64	100	160	256	
Mask design grid (nm) [K]	10	10	10	8	8	8	4	
Attenuated PSM transmission mean Deviation from target (+/- % of target) [L]	6	6	5	5	5	5	5	—
Attenuated PSM transmission uniformity (+/- % of target) [M]	4	4	4	4	4	4	4	—
Attenuated PSM phase mean deviation from 180° (+/- degree)	5	5	5	5	4	4	3	—
Attenuated PSM phase uniformity (+/- degree)	2	2	2	2	2	2	2	—
Alternating PSM phase mean deviation from 180° (+/- degree)	—	—	—	2	2	2	2	—
Alternating PSM phase uniformity (+/- degree)	—	—	—	2	2	2	2	—

Mask materials and substrates (Exposure tool dependent)		
	Optical	- Absorber on fused silica, except for 157 nm optical which will be absorber on modified fused silica square with pellicles - Primary PSM choices are attenuated shifter and alternating aperture
	X-Ray	- Refactory metal on Si Carbide Membrane (100 mm diameter) - "Pellicle" definition required
	E-Beam Projection	- Refractory metal scatterer on strutted SiN_x membrane (200 mm diameter) - "Pellicle" definition required
	EUV	- Absorber on multilayer reflector substrate (152 mm square) - "Pellicle" definition required
	Ion Projection	- Carbon coated silicon membrane stencil mask (200 mm diameter) - "Pellicle" definition required

Note: The requirements are for critical layers at defined year. Early volumes are assumed to be relatively small and difficult to produce.
** The second number applies to alternating PSM only. Delta between NGL and Optical is due to optical MEF at low k_1*

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 41b Mask Requirements—Long Term

YEAR TECHNOLOGY NODE	*2008* *70 nm*		*2011* *50 nm*	*2014* *35 nm*
Wafer minimum half pitch (nm) [A]	70		50	35
Wafer minimum isolated line (nm, in resist) [A]	45		30	20
Wafer minimum contact hole (nm, in resist)	80		55	40
Lithography technology	Optical	NGL	NGL	NGL
Magnification [B]	≥4	≥4	≥4	≥4
Mask minimum image size (nm) [C]	180	180	120	80
Mask OPC feature size (nm) [D]	90	—	—	—
Image placement (nm, multi-point) [E]	15	15	12	9
CD uniformity (nm, 3 sigma) [F]				
Isolated lines (MPU gates)	10*	7	5	3
Dense lines (DRAM half pitch)	14*	11	8	5.6
Contact/vias	8	12	9	6.4
Linearity (nm) [G]	10		7	5
CD mean to target (nm) [H]	6		5	4
Defect size (nm) [I]	55		40	28
Data volume (GB) [J]	1024		2048	8196
Mask design grid (nm) [K]	4		4	4
Attenuated PSM transmission mean deviation from target (+/- % of target) [L]	4	—	—	—
Attenuated PSM transmission uniformity (+/- % of target) [M]	4	—	—	—
Attenuated PSM phase mean deviation from 180° (+/- degree)	3	—	—	—
Attenuated PSM phase uniformity (+/- degree)	2	—	—	—
Alternating PSM phase mean deviation from 180° (+/- degree)	1	—	—	—
Alternating PSM phase uniformity (+/- degree)	1	—	—	—
Mask materials and substrates (exposure tool dependent)	**Optical**	- Absorber on fused silica, except for 157 nm optical which will be absorber on modified fused silica square with pellicles - Primary PSM choices are attenuated shifter and alternating aperture		
	X-Ray	- Refactory metal on Si Carbide Membrane (100 mm diameter) - "Pellicle" definition required		
	E-Beam Projection	- Refractory metal scatterer on strutted SiN_x membrane (200 mm diameter) - "Pellicle" definition required		
	EUV	- Absorber on multilayer reflector substrate (152 mm square) - "Pellicle" definition required		
	Ion Projection	- Carbon coated silicon membrane stencil mask (200 mm diameter) - "Pellicle" definition required		

Note: The requirements are for critical layers at defined year. Early volumes are assumed to be relatively small and difficult to produce.
** This number applies to alternating PSM only. Delta between NGL and Optical is due to optical MEF at low k_1*

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Notes for Table 41a and b Mask Requirements

[A] *Wafer Minimum Feature Size—Minimum wafer line size imaged in resists. Line size as drawn or printed to zero bias (Most commonly applied to isolated lines. Drives CD uniformity and linearity.)*

[B] *Magnification—Lithography tool reduction ratio, N:1*

[C] *Mask Minimum Image Size—The nominal mask size of the smallest primary feature to be transferred to the wafer (Commonly equivalent to wafer minimum feature size times the reduction ratio.)*

[D] *Mask OPC Feature Size—The minimum width of isolated non-printing features on the mask.*

[E] *Image Placement—The maximum component deviation (x or y) of the array of the images centerline relative to a defined reference grid.*

[F] *CD Uniformity—The three sigma deviation of actual image sizes on a mask for a single size and tone critical feature. Applies to features in X and Y and multiple pitches from isolated to dense. Contacts: Measure and tolerance refer to the area of the Mask Feature. For table simplicity the roadmap numbers normalize back to one dimension.* $\sqrt{AREA} - \sqrt{TARGET\ AREA}$

[G] *Linearity—Maximum deviation between mask "Mean to Target" for a range of features of the same tone and different design sizes. This includes features that are greater than half the primary feature size and less than five times the primary feature size.*

[H] *CD Mean to Target—The maximum difference between the average of the measured feature sizes and the intended feature size (design size). Applies to a single feature size and tone.* Σ*(Actual-Target)/Number of measurements.*

[I] *Defect Size—A mask defect is any unintended mask anomaly that prints or changes a printed image size by 10% or more. The Mask Defect Size listed in the roadmap are the square root of the area of the smallest opaque or clear "defect" that is expected to print for the stated generation.*

[J] *Date Volume—This is the expected maximum file size for uncompressed data for a single layer as presented to a raster write tool.*

[K] *Mask Design Grid—Wafer design grid times the mask magnification.*

[L] *Transmission—Ratio of the fraction of light passing through an attenuated PSM layer and the mask blank with no opaque films expressed in a percent.*

[M] *Phase—Change in optical path length between two regions on the mask expressed in degrees.*

POTENTIAL SOLUTIONS

The lithography strategy is presented in the following roadmaps:

- Exposure Technology Potential Solutions (Figure 23)
- Resist Technology Potential Solutions (Figure 24)
- Mask Technology Potential Solutions (Figure 25)

Optical lithography is the desired mainstream approach to its cost-effective limits. Significant efforts are required to extend 248 nm DUV lithography beyond 180 nm production. Lens designs and optical enhancements must be developed to increase depth of focus. Improved DUV resists and anti-reflection materials and processes are also required.

Significant emphasis and resources have been applied to 193 nm DUV technology in the past five years. Current programs are targeted to bring the technology to the marketplace for the 130 nm node. Affordable solutions to the depth of focus challenge must also be developed for this technology.

With the acceleration of the Roadmap and recent advancements in optical materials, 157 nm technology has received growing support over the past year. Commercial activity has been initiated in most sectors of the infrastructure. 157 nm technology is becoming a preferred option for the 100 nm node. As with 193 nm technology, significant worldwide resources must be focused to bring 157 nm to the marketplace for the 100 nm node.

The post-optical or next generation lithography (NGL) alternatives are all candidates at and below 100 nm. They each have strong regional support. 1× proximity XRL is now championed by Japan, along with electron beam direct-write (EBDW). IPL is being developed in Europe. EPL is being developed in the USA

and Japan. EUV is being developed in the USA, Japan, and Europe. Currently industry support is greatest for EUV and EPL.

Advanced resist systems will need to be developed for most advanced lithography approaches. Chemically amplified, multilayer, or thin layer imaging (TLI) resists may be needed to maintain the requirements of process latitude, etch resistance, implant blocking, and mechanical stability.

Evolutionary upgrades for existing mask equipment (such as mask writer, inspection, repair, and metrology) will be needed for each lithography generation. Mask inspection may require at-wavelength solutions for 193 nm technology and beyond. Significant process and materials development will be needed for all advanced lithography alternatives. Mask equipment for 1× proximity XRL will drive some requirements for advanced nx technologies.

Although many technology approaches exist, the industry is limited in its ability to fund the development of the full infrastructure (exposure tool, resist, mask, and metrology) for multiple technologies. Closely coordinated global interactions among government, industry, and universities are absolutely necessary to narrow the options for these future generations.

The introduction of non-optical lithography will be a major paradigm shift that may be necessary to meet the technical requirements and complexities driven by Moore's Law. This shift will drive major changes throughout the lithography infrastructure and require significant resources to commercialize the system.

Breakthroughs in direct-write technologies that achieved high throughput would be a significant paradigm shift. It would eliminate the need for masks, offering inherent cost and cycle-time reductions. Other technologies that eliminate the need for masks and resist would likewise constitute a paradigm shift.

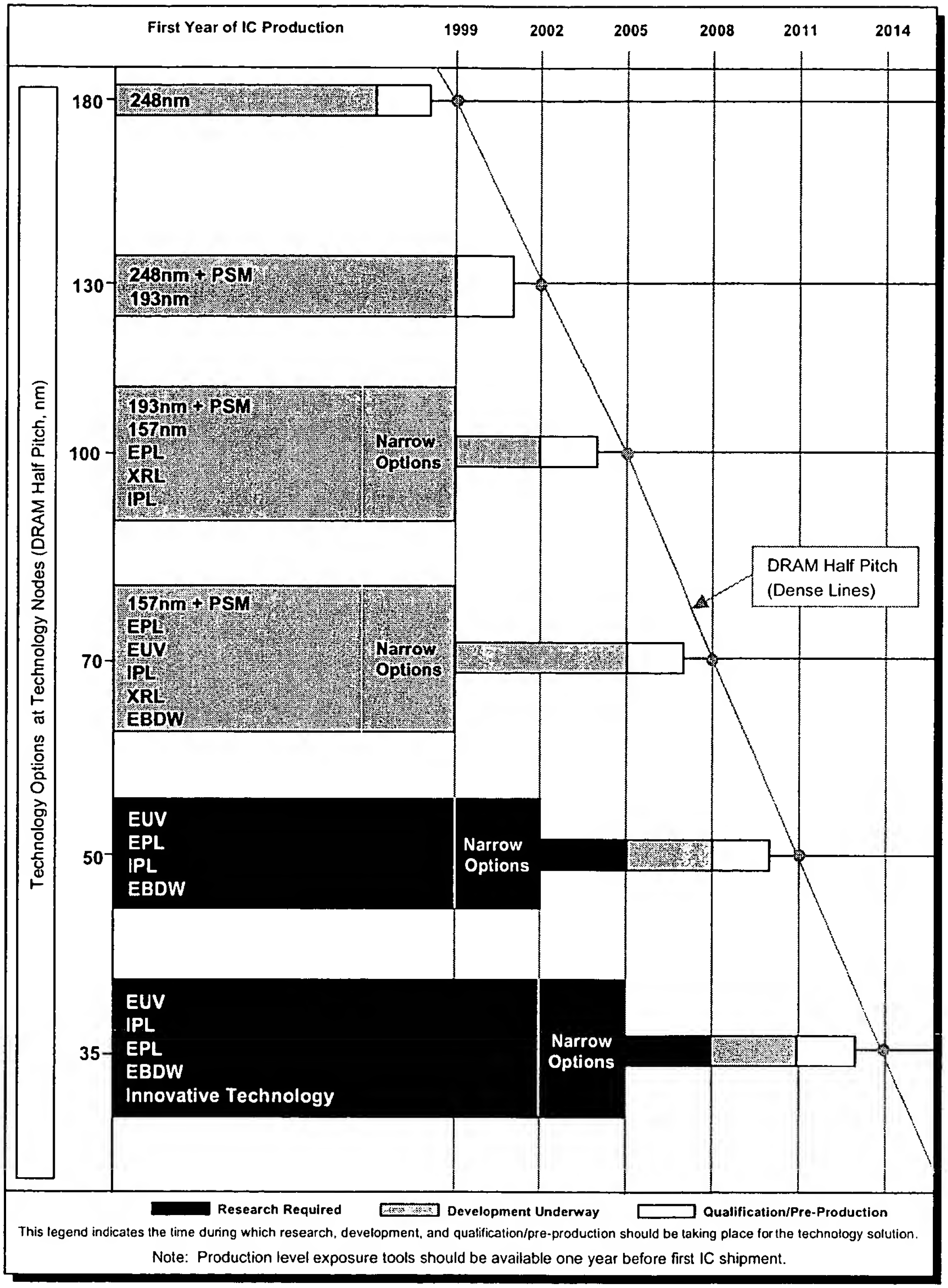

Figure 23 Lithography Exposure Tool Potential Solutions

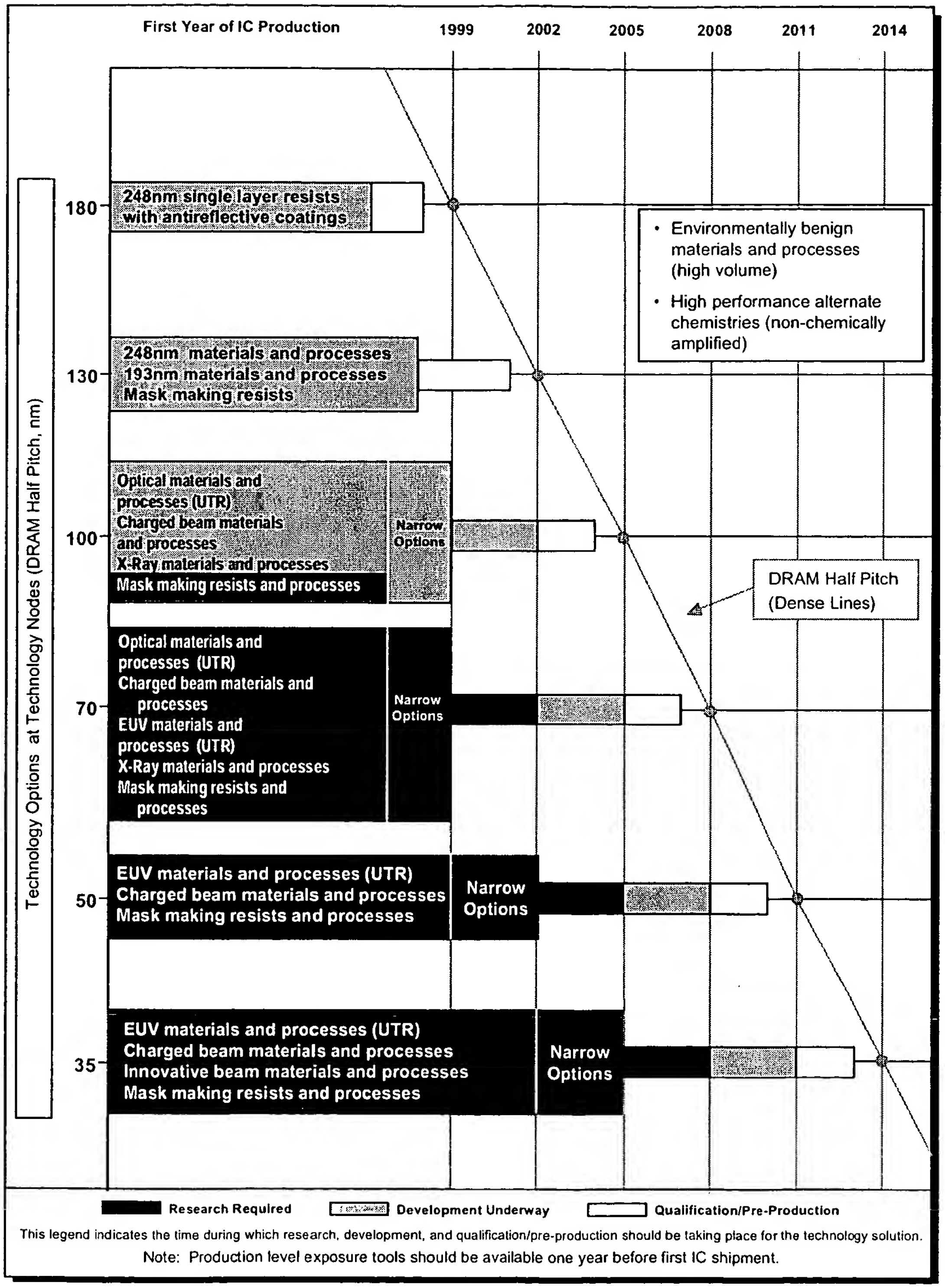

Figure 24 Resist Technology Potential Solutions

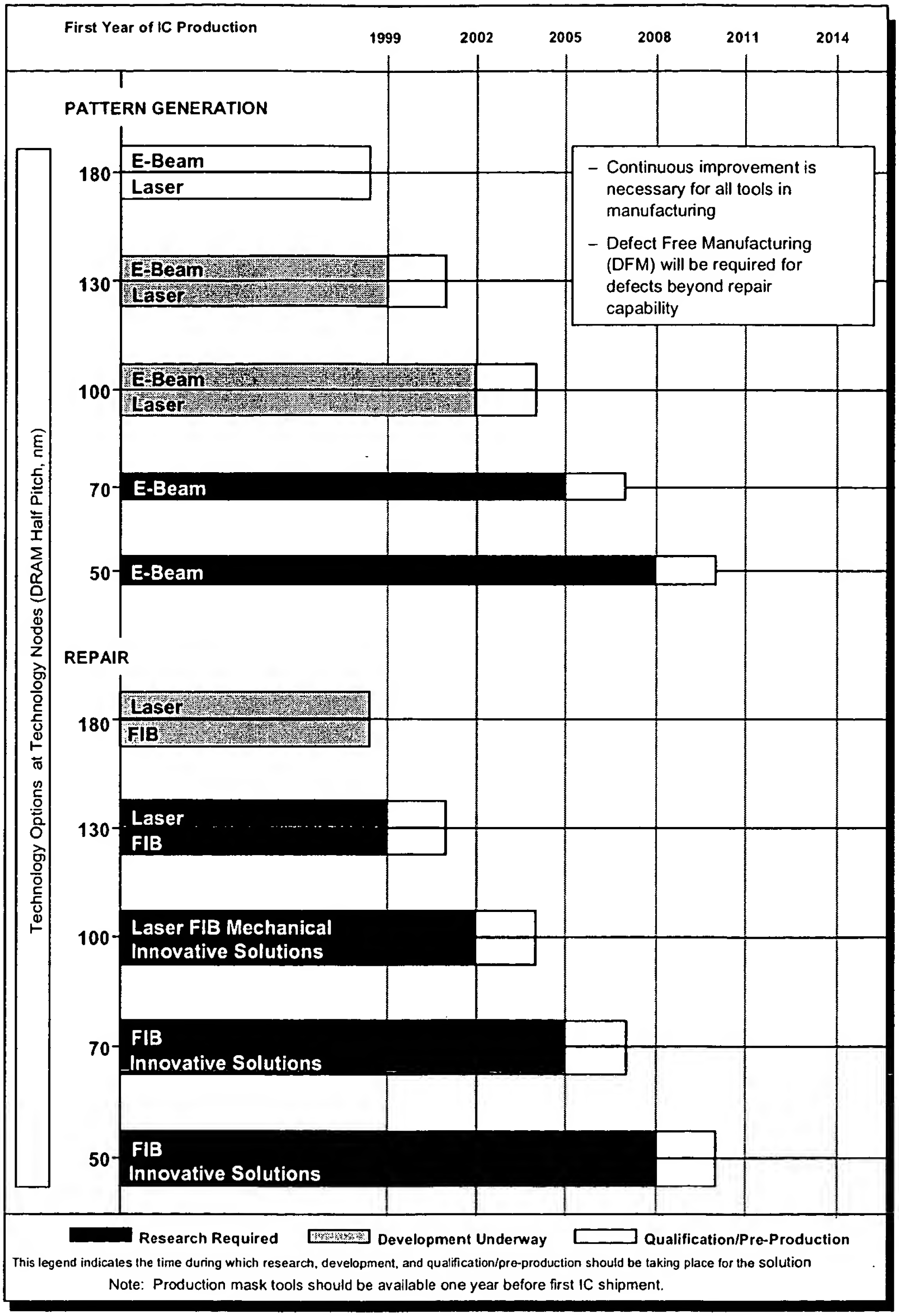

Figure 25 Mask Potential Solutions

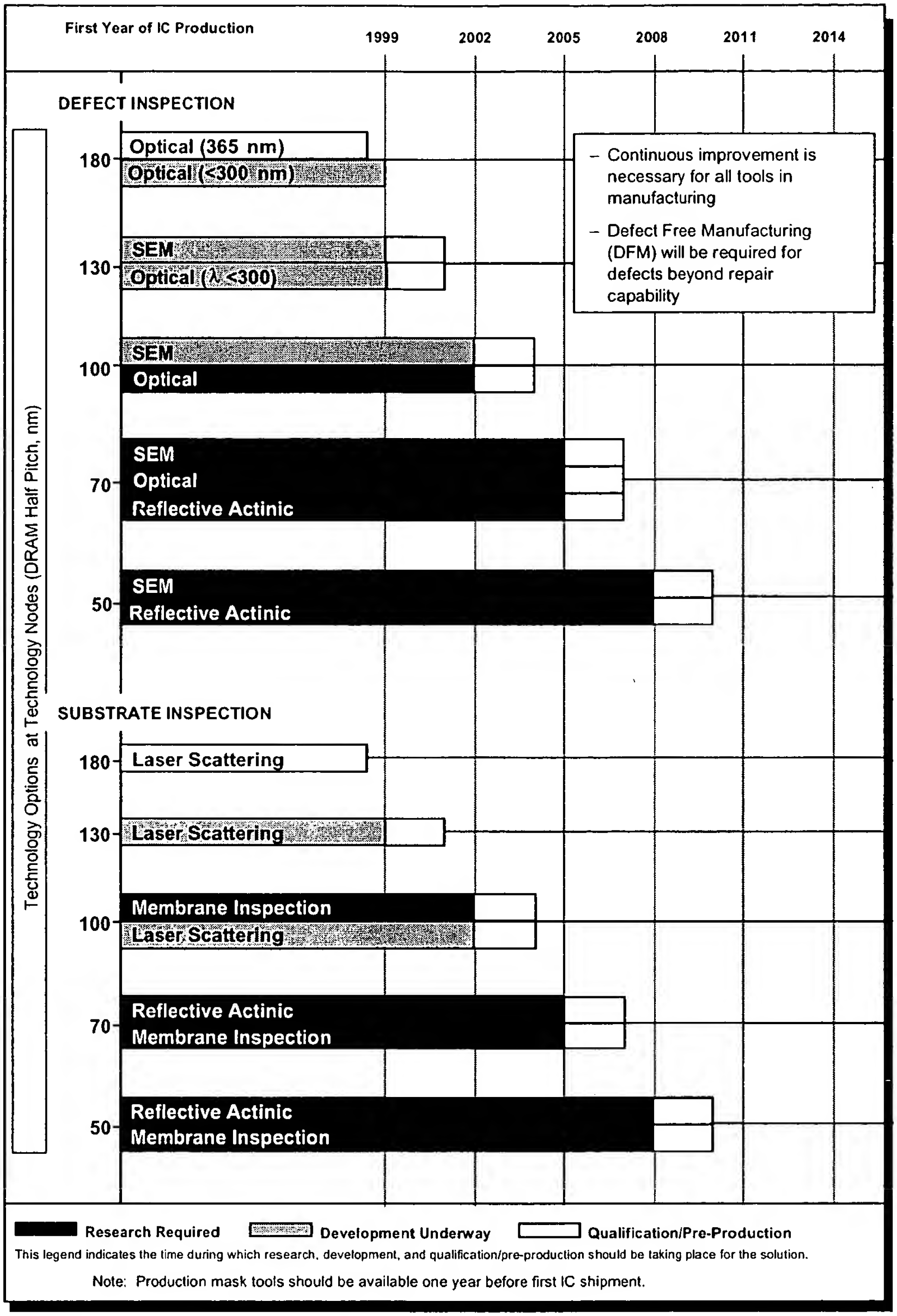

Figure 25 Mask Potential Solutions (continued)

CROSSCUT NEEDS AND POTENTIAL SOLUTIONS

The crosscut technology needs and potential solutions are defined in the following tables and figures:

- Lithography ESH Needs and Potential Solutions (Table 42)
- Lithography Defect Reduction Needs and Potential Solutions (Figure 26)
- Lithography Metrology Needs and Potential Solutions (Table 43)
- Lithography Modeling & Simulation Needs and Potential Solutions (Table 44)

ENVIRONMENT, SAFETY, AND HEALTH

From the perspective of ESH, lithography is represented by four subject areas. These are lithography and mask manufacturing chemicals (photoresists, thinners, developers, rinses, and strippers); processing equipment (spinners, vapor-phase deposition systems, and silylation ovens); exposure equipment (DUV, E-beam, X-ray, and ion beam); and equipment cleaning. Of critical concern with respect to these areas and the implementation of new lithography technologies is the avoidance of showstopper problems (see Table 42). In particular, issues such as new process chemicals evaluation, compliance with environmental regulations, equipment safety, and worker protection must be considered before changes are made.

Table 42 Lithography ESH Needs and Potential Solutions

Key Areas	*Summary of Needs*	*Potential Solutions*
Photolithography and Mask Manufacture Chemicals	Chemical Properties and Data: Chemical toxicity, risk assessment, status under TSCA* for new chemicals, ability to monitor potential exposures, and emissions from processes (HAPs** and VOCs), including materials for etch, strip, and etc. Materials Management: Integration of new materials into patterning; maintaining performance and cost, while promoting recycling and minimum use	Preparation of a list of acceptable lithography chemicals based on evaluation of TSCA conformance; development of analytical protocols that enable monitoring of new chemicals, robust chemical selection criteria; risk assessment; and the use of pollution prevention principles Alternate materials and chemistries Life cycle analysis of new materials and chemistries Use of additive technologies Use of benign materials
Processing Equipment	Exposure to toxic materials, emission of HAPs and VOCs, hazardous waste disposal, cost of ownership, and energy consumption Ergonomic design of equipment, PFC† usage, and plasma byproducts Minimize waste, for example, due to spin-on processes and assorted "wet" processes	Effective point-of-use abatement, optimization of tool exhaust, use of pollution prevention and DFESH‡ principles, specify supplier use of S2 and S8 standards Deployment of zero impact processes, elimination of the need for materials with significant global warming potentials, and utilization of DFESH tools in design for manufacture
Exposure Equipment	Toxicity of chemicals, exposure to radiation, risk assessment, cost-of-ownership, hazardous energies, and beam shielding	Perform risk assessment and cost-of-ownership analyses Establish radiation protection programs as necessary
Equipment Cleaning	Solvent usage, emission of HAPs and VOCs, hazardous waste disposal, and personal protective equipment Selection of cleaners and cleaning methodologies	Cryogenic cleaning, solvent free cleaning, dry resist technology, point-of-use abatement, pollution prevention, and optimization of tool design Redesign of processes and equipment to achieve minimal environmental impact

** TSCA—toxic substance control act*
*** HAPs—hazardous air pollutants*
VOCs—volatile organic compounds
† PFC—perfluorocompound
‡ DFESH—design for ESH

DEFECT REDUCTION

Figure 26 is intended to be a guide to enhance awareness of these defect reduction issues as the industry follows the 1999 Roadmap.

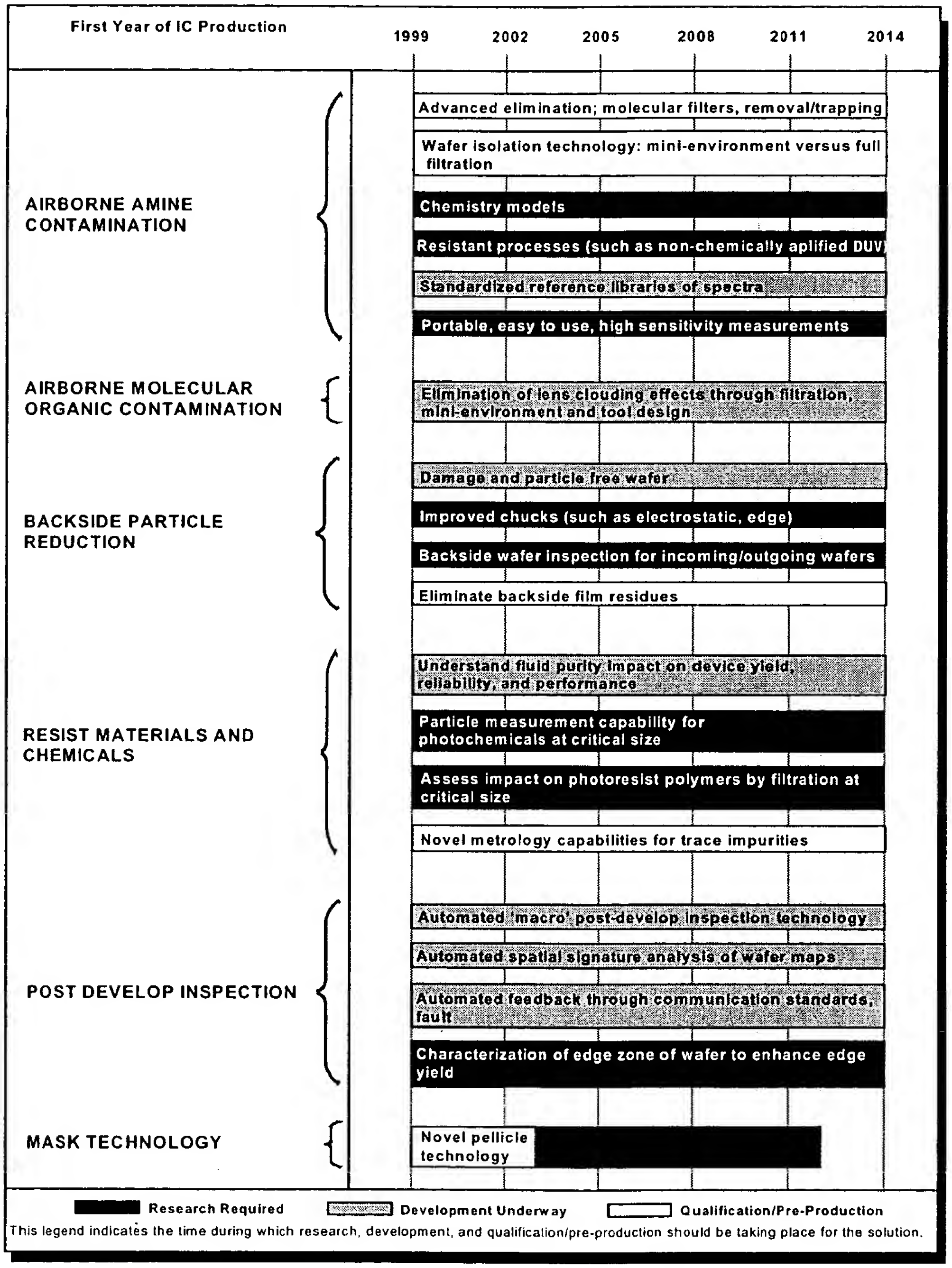

Figure 26 Lithography Defect Reduction Needs and Potential Solutions

METROLOGY

Physical metrology is challenged by the rapid advancement of lithography capabilities and is not meeting scheduled improvements for precision and reproducibility. CD metrology tool resolution, accuracy, tool-to-tool matching, and reproducibility all require significant advancement if they are to meet the goals stated in the *Metrology* chapter Table 83. Electrical measurements provide a monitoring of gate and interconnect linewidth, but only after the point where reworking the wafers is possible. Future overlay metrology requirements, along with problems caused by the low contrast levels, will drive the development of new optical methods along with scanning probe microscopy (SPM) and scanning capacitance microscopy (SCM). Statistical methods such as dynamic averaging are under investigation. Innovations, such as scatterometry sensor-based measurement, will require application development before being accepted. Further innovations are required, including those captured in the *Metrology* chapter section on Microscopy, Figure 59. A summary of these needs and potential solutions are shown in Table 43.

Table 43 Lithography Metrology Needs and Potential Solutions

KEY AREAS	*SUMMARY OF NEEDS*	*POTENTIAL SOLUTIONS*
Wafer CD Measurement	Enhance precision and tool matching and meeting sub 100 nm precision requirements Accelerate development of improved resolution Extend CD to damascene Processing and low κ materials Accuracy for sub-100 nm nodes	Extend CD-SEM to 100 nm using model based measurement Develop electron holography for sub 100 nm nodes Investigate scatterometry for inline and *in situ* Develop new probe tips for CD-AFM for > 100 nm CD-SEM calibration and as a potential solution for sub-100 nm CD Develop reference material for sub 100 nm that correlates physical and electrical measurements
Mask CD Measurement	OPC and PSM features require 2D and 3D measurements Charging of mask during measurement	CD-AFM, CD-SEM, and electron holography are potential long term solutions
Overlay	Meet Roadmap requirements for damascene processes and low κ materials Overcome issues with errors not observed by Box-in-Box target for phase shift masks	Potential solutions include new optical measurement technology, SEM, and scanning capacitance microscopy. Investigate new target structures.
Mask Image Placement	Feed-forward corrections for process induced shifts from pellicle and membrane masks Meeting sub-100 nm requirements for precision	Interferometry and Moire scale measurements

MODELING & SIMULATION

Table 44 outlines the technology needs and potential solutions for Lithography modeling and simulation.

Table 44 Lithography Modeling & Simulation Needs and Potential Solutions

KEY AREAS	SUMMARY OF NEEDS	POTENTIAL SOLUTIONS
Resist Modeling	Predictive quantitative models, polymer surface interactions, coating and baking processes, silylation, edge roughness, E-beam, X-ray, and EUV resists, physically correct models for diffusion in chemically amplified resists.	Establish mechanism-based models from basic studies on model materials Extend models to emerging materials Develop methodology for calibrating models on production tooling Validate models on 2D and 3D profiles
Optical System Modeling	Nonuniformity over field, resolution enhancements, and interactions with optical system nonidealities, global application of OPC* and PPC** to 10^8 features, photomask nonidealities, substrate reflections	Strategies and engines for transparent application of process and tool dependent OPC and PPC Engineering workbench TCAD*** tools for optical system level consideration of resolution enhancements and device pattern/transfer context Simulation of mask writing nonidealities and their impact on printing Calibration of simulators with profile SEMs† and statistical metrology
130 nm and Beyond	Image quality, overlay, throughput, and patterning/transfer in advanced lithography systems based on EUV, X-ray, E-beam and maskless approaches, pattern dependence, stress and edge roughness in dissolution	Full system simulation of lithography tools with emphasis on balancing tradeoffs in performance limiters such as resolution throughput, nonidealities in masks and mechanical and electrical components, materials inhomogeneities and transport effects in resists Simulation-based assessment of out-of-the-box approaches to maskless lithography
TCAD and Metrology	Implications of processing physics at the IC system design level, knowledge of manufacturing tolerance in simulating process design, technologist friendly tools, accurate interpretation of optical monitors, scanning probes and SEMs	Integration of TCAD with IC CAD‡ Integration of TCAD simulation with parameter extraction and statistical metrology of CIM§ Standard engineering workbench-based simulation environments Modeling of optical monitoring and SEM measurements

** OPC—optical proximity correction*
*** PPC—process proximity correction*
**** TCAD—technology computer aided design*
† SEM—scanning electron microscope
‡ CAD—computer aided design
§ CIM—computer integrated manufacturing

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS
1999 EDITION

INTERCONNECT

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INTERCONNECT

SCOPE

The *Interconnect* chapter of the 1994 National Technology Roadmap for Semiconductors (NTRS) described the first needs for new conductor and dielectric materials that would be necessary to meet the projected overall technology requirements. With the publication of the 1997 edition of the NTRS, the introduction of copper-containing chips was imminent. The 1999 International Roadmap highlights a continued change to new materials, now being introduced at an unprecedented pace. Further, although the technical product driver for the smallest feature size remains the dynamic memory chip, an emerging classification of chips, the system-on-a-chip, or SoC, will challenge microprocessors for increased complexity and decreased design rules. Managing this rapid rate of materials introduction and the concomitant complexity represents the overall near term challenge. For the long term, material innovation with traditional scaling will no longer satisfy performance requirements. Interconnect innovation with optical, RF or vertical integration combined with accelerated efforts in design and packaging will deliver the solution.

The function of an interconnect or wiring system is to distribute clock and other signals and to provide power/ground to and among the various circuits/systems functions on a chip. Current leading-edge logic processors have 6–7 levels of high-density interconnect, and current leading-edge memory has three levels. Distribution of the clock and signal functions is accomplished on three types of wiring (local, intermediate, and global). Local wiring, consisting of very thin lines, connects gates and transistors within an execution unit or a functional block (such as embedded logic, cache memory, address adder) on the chip. Local wires usually span a few gates and occupy first and sometimes second metal layers in a multi-level system. The lengths of these wires tend to scale down with technology. Intermediate wiring provides clock and signal distribution within a functional block with typical lengths up to 3–4 mm. Intermediate wires are wider and taller than local wires to provide lower resistance signal/clock paths. Global wiring provides clock and signal distribution between the functional blocks, and delivers power/ground to all functions on a chip. Global wires, which occupy the top one or two layers, are longer than 4 mm and can be as long as half of the chip perimeter.

DIFFICULT CHALLENGES

Table 45 highlights and differentiates the five key challenges in the near term (≥ 100 nm) and long term (< 100 nm). In the near term, the most difficult challenges for interconnect include the rapid introduction and integration of new materials and processes, dimensional control, physical/electrical reliability of interconnect structures and interconnect processes with low or no device impact. The introduction of new low κ dielectrics, chemical vapor deposition (CVD) metal/barrier/seed layers, and additional elements for SoC, provide significant process and process integration challenges. Interfaces, contamination, adhesion, mechanical stability, electrical parametrics, and thermal budget, confounded by the number of wiring levels for interconnect, ground planes and passive elements, create a difficult to manage complexity.

Table 45 Interconnect Difficult Challenges

Five Difficult Challenges ≥100 nm / Through 2005	*Summary Of Issues*
New materials	Rapid introduction of materials/processes are necessary to meet resistivity and low/high κ targets and address SoC needs.
Reliability	New materials create new chip reliability (electrical, thermal and mechanical) exposure. Detecting, testing, modeling and control of failure mechanisms will be key.
Process integration	Combinations of materials (Cu, Al, low κ, high κ, ferroelectrics, new barriers/nucleation layers) along with multiple technologies used in SoC applications open new integration challenges.
Dimensional control	Multi-dimensional control of interconnect features is necessary for circuit performance and reliability. Multiple levels, new materials, reduced feature size and pattern dependent processes create this challenge.
Interconnect process with low/no device impact	As feature sizes shrink, interconnect processes must be compatible with device roadmaps. Low plasma damage, contamination and thermal budgets are key concerns.
Five Difficult Challenges <100 nm / Beyond 2005	*Summary Of Issues*
Dimensional control and metrology	Multi-dimensional control and metrology of interconnect features is necessary for circuit performance and reliability.
Aspect ratios for fill and etch	As features shrink, etching and filling high aspect ratio structures will be challenging, especially for DRAM. Dual damascene metal structures are also expected to be difficult.
New materials and size effects	Continued introductions of materials/processes are expected. Microstructural and quantum effects become important.
Solutions beyond copper and low κ	Material innovation with traditional scaling will no longer satisfy performance requirements. Accelerated design, packaging and unconventional interconnect innovation will be needed.
Process integration	Combinations of materials along with multiple technologies used in SoC applications are a continued challenge. Plasma damage, contamination and thermal budgets are key concerns.

Dimensional control is a key challenge for present and future interconnect technology generations. The dominant architecture, damascene, requires tight control of pattern, etch and planarization. To extract maximum performance, interconnect structures cannot tolerate variability in profiles without producing undesirable RC degradation. These dimensional control requirements place new demands on high throughput imaging metrology for measurement of high aspect ratio structures. New metrology techniques are also needed for inline monitoring of adhesion and defects. Larger wafers and the need to limit test wafers will drive the adoption of more *in situ* process control techniques. Dimensional control, a challenge now, will become even more critical as new materials, such as porous low κ dielectrics and CVD metals, play a role at the tighter pitches and higher A/R (aspect ratio) of intermediate and global levels. At the 50 nm node, feature size effects, such as electron surface scattering, will increase the effective resistivity and new conductor technologies may be required. Cu and low κ will continue to find applications in future chip generations, but for global wiring, new interconnect solutions incorporating RF or optical propagation will be required, bringing even more material and process integration challenges.

Feature size reduction, new materials, and damascene structures all challenge metrology for on-chip interconnect development and manufacture. Critical dimension measurements are needed for very high

aspect ratio features and ultra-thin barriers. Methods must be developed to accommodate the increased complexity of the wiring levels of future chips. Other metrology challenges include measuring resistivity and dielectric constant at high frequency, adhesion and mechanical properties.

TECHNOLOGY REQUIREMENTS

To adequately describe the wiring needs of interconnect, near term (1999–2005) and long term (2008–2014) technology requirements and potential solutions are addressed for three specific classes of products: microprocessors (MPU), dynamic memory (DRAM) and system-on-a-chip (SoC) [Tables 46–48]. For MPUs, local, intermediate, and global wiring pitches/aspect ratios are differentiated to highlight a hierarchical scaling methodology that has been broadly adopted. Implementation of copper and low κ materials allows scaling of the intermediate wiring levels and minimizes the impact on wiring delay. Local wiring levels are relatively unaffected by traditional scaling. RC delay, however, is dominated by global interconnect and the benefit of materials changes alone is insufficient to meet overall performance requirements. Figure 27 shows the delay of local and global wiring in future generations. Repeaters can be incorporated to mitigate the delay in global wiring but consume power and chip area.

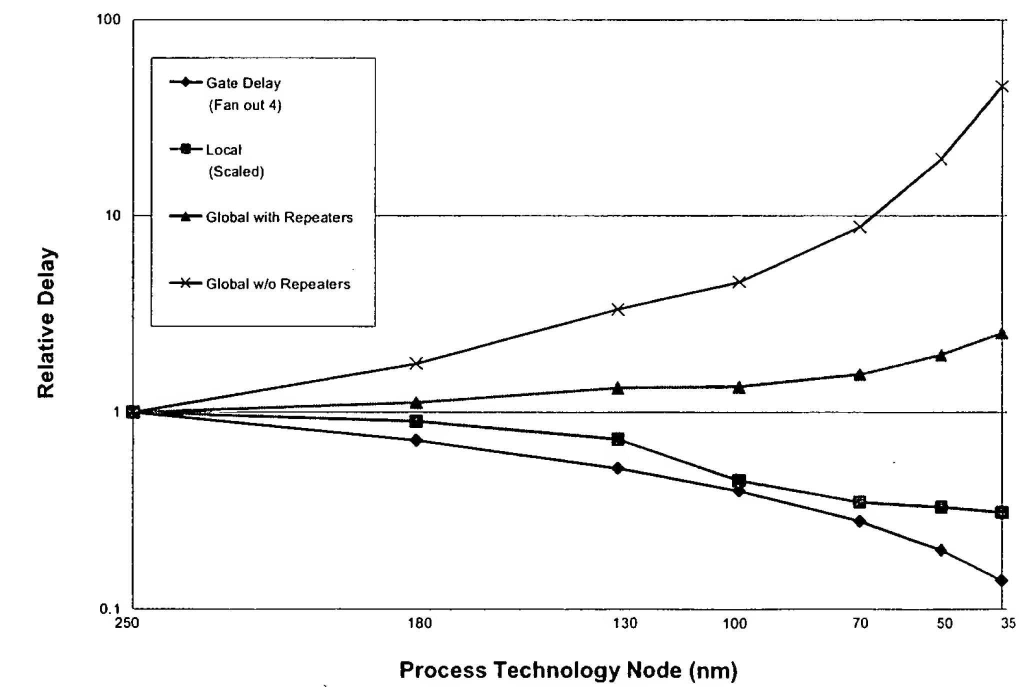

Figure 27 Delay for Local and Global Wiring versus Feature Size

In the long term, new design or technology solutions (such as coplanar waveguides, free space RF, optical interconnect) will be needed to overcome the performance limitations of traditional interconnect. Inductive effects will also become increasingly important as frequency of operation increases, and additional metal patterns or ground planes may be required for inductive shielding. As supply voltage is scaled or reduced, crosstalk has become an issue for all clock and signal wiring levels; the near term solution adopted by the industry is the use of thinner metallization to lower line-to-line capacitance. This approach is more effective for the lower resistivity copper metallization, where reduced aspect ratios (A/R) can be achieved with less

sacrifice in resistance as compared with aluminum metallization. The 1999 Roadmap reflects this design trend by featuring reduced aspect ratios (as an alternative means of reducing capacitance) and less aggressive scaling of dielectric constant in comparison with the 1997 Interconnect Roadmap. The latter change expands the development window to address the difficulty in integrating low κ dielectrics into a damascene architecture.

MPUs utilize a high number of metal layers; designers are adopting a hierarchical wiring approach with steadily increasing pitch and thickness at each conductor level to alleviate the impact of interconnect delay on performance. Refer to Figure 28.

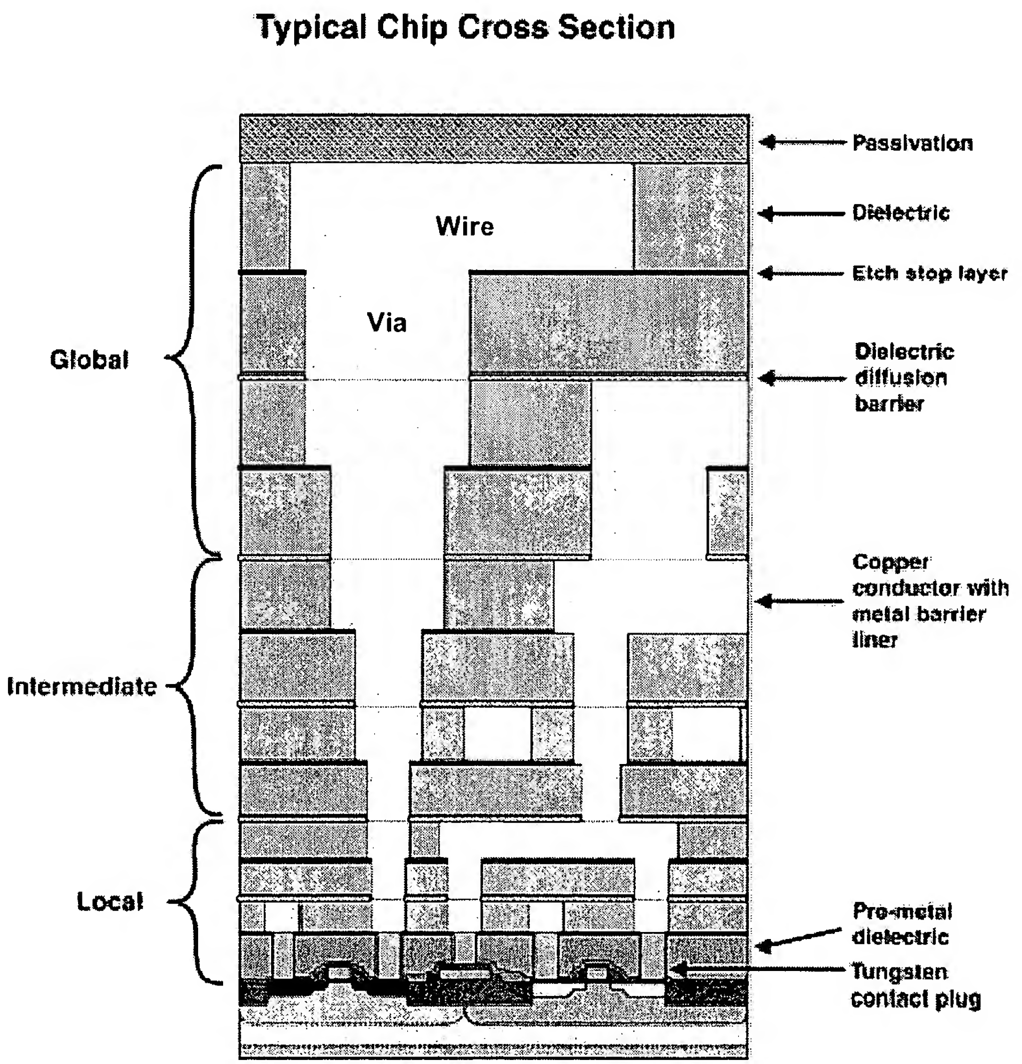

Figure 28 Cross-section of Hierarchical Scaling

To accommodate the need for ground planes or on-chip de-coupling capacitors, the growth of metal levels is projected to increase beyond those specified solely to meet performance requirements. Copper wire aspect ratios are lower than those for Al, which provides for a reduction in line-to-line capacitance and crosstalk

but leads to higher wire resistance. Aspect ratios of features at the global levels will be comparable for both copper and aluminum conductor solutions, to minimize delay. Refer to Table 46a and b.

Table 46a MPU Interconnect Technology Requirements—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
MPU ½ pitch	230	210	180	160	145	130	115
MPU gate length (nm)	140	120	100	85	80	70	65
Number of metal levels	6-7	6–7	7	7–8	8	8	8–9
Number of optional levels—ground planes/capacitors	0	0	0	2	2	2	2
Jmax (A/cm^2)—wire (at 105°C)	5.8E5	7.1E5	8.0E5	9.6E5	1.1E6	1.3E6	1.4E6
Imax (mA)—via (at 105°C)	0.36	0.36	0.33	0.32	0.29	0.27	0.24
Local wiring pitch (nm)	500	450	405	365	330	295	265
Local wiring A/R (for Al)	2	2	2.1	2.1	2.2	**	**
Local wiring A/R (for Cu)	1.4	1.4	1.5	1.5	1.6	1.6	1.7
Cu local dishing (nm), 5% × height	18	16	15	14	13	12	11
Intermediate wiring pitch (nm)	640	575	520	465	420	375	340
Intermediate wiring A/R (Al)	2.2	2.3	2.4	2.5	2.6	**	**
Intermediate wiring dual damascene A/R (Cu wire/via)	2.0/2.1	2.1/2.1	2.2/2.1	2.2/2.1	2.2/2.2	2.3/2.2	2.4/2.2
Cu intermediate dishing (nm), 15 micron wide wire, 10% × height	64	60	57	51	46	43	41
Dielectric erosion (nm), intermediate wiring, 50% areal density, 10% × height	64	60	57	51	46	43	41
Minimum global wiring pitch (nm)	1050	945	850	765	690	620	560
Global wiring A/R (Al)	2	2.1	2.2	2.3	2.4	**	**
Global wiring dual damascene A/R (Cu wire/via)	2.2/2.4	2.3/2.6	2.4/2.7	2.5/2.7	2.6/2.8	2.7/2.8	2.7/2.8
Cu global wiring dishing (nm), 15 micron wide wire, 10% × height	116	109	102	95	90	84	76
Conductor effective resistivity (μΩ-cm) Al wiring	3.3	3.3	3.3	3.3	3.3	**	**
Conductor effective resistivity (μΩ-cm) Cu wiring*	2.2	2.2	2.2	2.2	2.2	2.2	2.2
Barrier/cladding thickness (for Cu wiring) (nm)***	17	16	14	13	12	11	10
Interlevel metal insulator —effective dielectric constant (κ)	3.5–4.0	3.5–4.0	2.7–3.5	2.7–3.5	2.2–2.7	2.2–2.7	1.6–2.2

* *Assumes a conformal barrier/nucleation layer*
** *This technology is not expected to extend to this node*
*** *Calculated for a conformal layer in local wiring to meet minimum effective conductor resistivity*

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 46b MPU Interconnect Technology Requirements—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
MPU ½ pitch	80	55	40
MPU gate length (nm)	45	32	22
Number of metal levels	9	9–10	10
Number of optional levels – ground planes/capacitors	3	4	4
Jmax (A/cm^2)—wire (at 105°C)	2.1E6	3.7E6	4.6E6
Imax (mA)—via (at 105°C)	0.18	0.16	0.11
Local wiring pitch (nm)	185	130	95
Local A/R (for Cu)	1.9	2.1	2.3
Cu local dishing (nm), 5% × height	9	7	5
Intermediate wiring pitch (nm)	240	165	115
Intermediate wiring dual damascene A/R (Cu wire/via)	2.5/2.3	2.7/2.4	2.9/2.5
Cu intermediate wiring dishing (nm), 15 micron wide wire, 10% × height	30	22	17
Dielectric erosion (nm), intermediate wiring	0	0	0
Minimum global wiring pitch (nm)	390	275	190
Global wiring dual damascene A/R (Cu wire/via)	2.8/2.9	2.9/3.0	3.0/3.1
Cu global wiring dishing (nm), 15 micron wide wire, 10% × height	55	38	29
Conductor effective resistivity (μΩ-cm) Cu wiring	1.8	<1.8	<1.8
Barrier/cladding thickness (nm)	0	0	0
Interlevel metal insulator—effective dielectric constant (κ)	1.5	<1.5	<1.5

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

DRAM interconnect technology reflects the most aggressive metal pitch and highest aspect ratio contacts and will continue to provide the most significant challenges in dimensional control and defect management (refer to Table 47). The introduction of low κ dielectric materials at 130 nm and copper at the 100 nm technology node is required to meet the performance of high speed memory products (including RAMBUS). However, the pricing sensitivity of the marketplace may delay introduction if cost savings associated with copper are not realized. This suggests that capability for aluminum processing must be continuously improved and extended.

Table 47a DRAM Interconnect Technology Requirements—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
DRAM ½ pitch	180	165	150	130	120	110	100
Number of metal levels	3	3	3	3–4	4	4	4
Contact A/R—stacked capacitor	9.3	10.0	10.7	11.4	11.9	12.4	13.0
Local wiring pitch (nm) noncontacted	360	330	300	260	240	210	200
Specific contact resistance (Ω-cm^2)	3.0E-7	2.5E-7	2.0E-7	1.7E-7	1.6E-7	1.1E-7	1.0E-7
Specific via resistance (Ω-cm^2)	7E-9	5E-9	3E-9	2E-9	2E-9	1E-9	1E-9
Conductor effective resistivity (μΩ-cm)*	3.3	3.3	3.3	3.3	3.3	3.3	2.2
Interlevel metal insulator—effective dielectric constant (κ)	4.1	4.1	4.1	3.0–4.1	3.0–4.1	3.0–4.1	2.5–3.0

* *Assumes a conformal barrier/nucleation layer*

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 47b DRAM Interconnect Technology Requirements—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
DRAM ½ pitch	70	50	35
Number of metal levels	4	4	4
Contact A/R—stacked capacitor	14.1	16.1	23.1
Local wiring pitch (nm) non-contacted	140	100	70
Specific contact resistance (Ω-cm^2)	5.0E-8	2.5E-8	1.5E-8
Specific via resistance (Ω-cm^2)	6E-10	3E-10	1.5E-10
Conductor effective resistivity (μΩ-cm)*	2.2	2.2	2.2
Interlevel metal insulator—effective dielectric constant (κ)	2.5–3.0	2.0–2.5	2.0–2.3

* *Assumes a conformal barrier/nucleation layer*

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

System-on-a-chip technology requirements, shown in Table 48, reflect vertical scaling trends and reductions in dielectric constant similar to MPUs. SoC design methodology does not incorporate hierarchical scaling because system clock speed is not the sole driver of performance. Optional additional levels of conductors and dielectrics for the integration of resistors, inductors, capacitors or other SoC elements are specified. However, the need for embedded memory and/or passive components in SoC applications presents significant material and process integration challenges.

Table 48a SoC Interconnect Technology Requirements—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
MPU ½ pitch (nm)	230	210	180	160	145	130	115
ASIC gate (nm)	180	165	150	130	120	110	100
Number of metal levels	6	6	7	7	7–8	8	8
Number of optional levels—passive elements	1	1	2	2	4	4	4
Local wiring pitch (nm)	450	405	360	325	290	260	230
Local wiring A/R (for Al)	2	2	2.1	2.1	2.2	**	**
Local wiring A/R (for Cu)	1.4	1.4	1.5	1.5	1.6	1.6	1.7
Intermediate wiring pitch (nm)	560	505	450	405	360	325	285
Intermediate wiring A/R (Al)	2.2	2.3	2.4	2.5	2.6	**	**
Intermediate via A/R (Al)	2.8	2.8	2.9	2.9	3.0	**	**
Intermediate wiring dual damascene A/R (Cu wire/via)	2.0/2.1	2.1/2.1	2.2/2.1	2.2/2.1	2.2/2.2	2.3/2.2	2.4/2.2
Global wiring pitch (nm)	900	810	720	650	580	520	460
Global wiring A/R (Al)	2.2	2.3	2.4	2.5	2.6	**	**
Global wiring dual damascene A/R (Cu wire/via)	2.2/2.4	2.3/2.6	2.4/2.7	2.5/2.7	2.6/2.8	2.7/2.8	2.7/2.8
Interlevel metal insulator—effective dielectric constant (κ)	3.5–4.0	3.5–4.0	2.7–3.5	2.7–3.5	2.2–2.7	2.2–2.7	1.6–2.2

** *This technology is not expected to extend to this node.*

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 48b SoC Interconnect Technology Requirements—Long Term

YEAR TECHNOLOGY NODE	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
MPU ½ pitch (nm)	80	55	40
ASIC gate (nm)	70	50	35
Number of metal levels	9	9–10	10
Number of optional levels—passive elements	6	6	6
Local wiring pitch (nm)	165	120	85
Local wiring A/R (for Cu)	1.9	2.1	2.2
Intermediate wiring pitch (nm)	210	145	110
Intermediate wiring dual damascene A/R (Cu wire/via)	2.5/2.3	2.7/2.4	2.9/2.5
Global wiring pitch (nm)	330	240	170
Global wiring dual damascene A/R (Cu wire/via)	2.8/2.9	2.9/3.0	3.0/3.1
Interlevel metal insulator—effective dielectric constant (κ)	1.5	< 1.5	< 1.5

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Although the bulk conductor material (alloys of aluminum) has remained invariant, both new materials, including spin-on-glass (SOG) and new processes, chemical mechanical planarization (CMP), for example, have characterized successive generations. For MPUs, the 1998 implementation of copper conductors in manufacturing was necessary to meet clock speed requirements and represented the beginning of an accelerated pace of new materials changes. DRAM applications are expected to utilize tungsten and aluminum alloy wiring and studs until the 100 nm node, driving a need for improvements in filling of high A/R contacts and wires.

Damascene processing flows will dominate fabrication methodologies. Figure 29 illustrates several typical interlevel dielectric (ILD) architectures available to create the interconnect wiring levels. While current copper damascene processes utilize physical vapor deposited (PVD) Ta-based barriers and Cu nucleation layers, continued scaling of feature size requires development of other materials and seed deposition solutions by 2002. Continuous improvement of tools and chemistries will extend electrochemically deposited Cu (ECD) to 100 nm and beyond but small, high A/R features necessitate the simultaneous development and subsequent selection of alternative filling techniques. A thin barrier is also needed to maintain the effective conductor resistivity in these features. Nucleation layer conformality requirements become more stringent to enable Cu ECD filling of damascene features. Surface segregated, CVD, and dielectric barriers represent intermediate potential solutions but, by 2008, zero thickness barriers are required.

Near term dielectric needs include lower permittivity materials for wire insulators and etch stops, higher permittivity materials for de-coupling capacitors and materials with high remanent polarization for ferroelectric memories. The thermal, mechanical and electrical properties of these new materials present a formidable challenge for process integration. In the longer term, dielectric characteristics at high frequency will become more important, and optical materials may be required that have sufficient optical contrast to serve as low-loss waveguides.

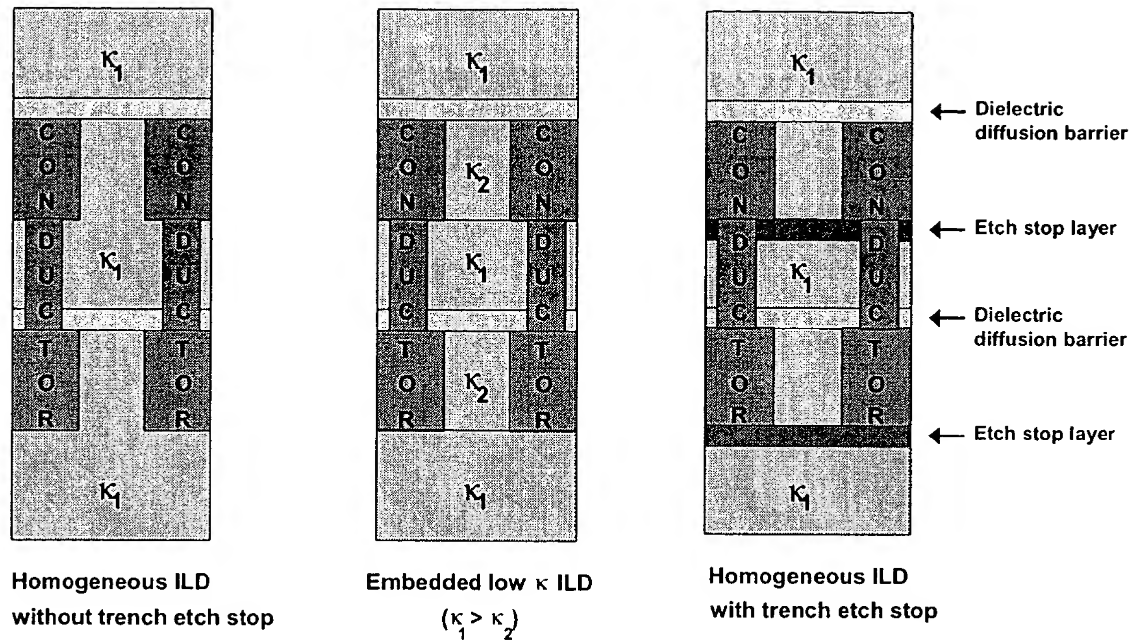

Figure 29 Typical ILD Architectures

Continuous improvement in dielectric CMP and post-CMP defect reduction will be needed in the near term. The development of alternative planarization techniques is a potential long term solution. For copper CMP, minimization of erosion and dishing will be necessary to meet performance needs as the wiring thickness is scaled. Planarization processes (with associated end-point) that are compatible with low κ dielectrics which may have low density and poor mechanical strength, must be developed. Improvements in post-CMP clean will be critical to achieving the low defect densities required in future devices. Etch, resist strip and post-etch cleans must be developed that maintain the desired selectivity to etch stop layers and diffusion barriers but do not degrade low κ dielectrics. Low or no device damage during etch and deposition processes is the goal, especially as thinner gate oxides and/or new gate dielectric materials are introduced.

POTENTIAL SOLUTIONS

DIELECTRIC POTENTIAL SOLUTIONS

The Dielectric Potential Solutions roadmap, Figure 30, describes solutions that cover the broad range of material permittivity from 1 to >100. Here, the represented κ values are for the bulk material, averaged for anisotropy. Three main challenges in the dielectric area are foreseen in the upcoming technology generations:

1. development and integration of materials with the lowest possible permittivity (κ)
2. development and integration of dielectric materials with the highest possible permittivity for memory and system-on-a-chip applications
3. dielectrics for new interconnect technologies beyond Cu/low κ.

Of these, the first two problems are mostly well defined, with solutions being pursued; the third is in the research and definition stages.

High κ materials for interconnect de-coupling capacitors are expected to be introduced in SoC and logic applications at the 130 nm node. Technical drivers are the frequency independence of the dielectric constant, low electrical leakage, controlled process, low cost, and integration with electrode materials. In the short term, development of CVD tantalum oxide is underway; integrated metal-insulator-metal (MIM) capacitors using aluminum oxide are an additional potential solution. More research is required leading to the development of barium strontium titanate (BST) high κ capability. Ferroelectric memory elements require materials with high remanent magnetization that are compatible with interconnect processing, such as lead zirconium titanate (PZT) or compounds of strontium, bismuth, and tantalum (SBT).

It is anticipated that the first introduction of $\kappa < 3.0$ dielectric materials with Cu interconnect will be at the 130 nm node. Materials suitable for introduction at this node are now relatively mature and include CVD carbon-doped silicon oxide, organic polymers and inorganic hydrogen silsequioxanes. Development effort is now focusing on integration with other interconnect processes, such as etch, post-etch ash and clean, metallization, and planarization. Electromigration resistance and packaging compatibility of Cu/low κ structures has not yet been documented. Multiple dielectric materials and processes will be used, depending on process requirements, cost, and compatibility. Reducing the dielectric constant below 2.5 requires lowering of the material density (usually by the introduction of pores) or the addition of fluorine (fluoropolymers). Development work is underway on emplacing controlled porosity into most of the existing leading low κ materials types. The ideal porous material would consist of a closed network of small pores (pore size << feature size) with a tight size distribution. A key challenge for porous materials is mechanical robustness. Unfortunately, vital properties such as elastic modulus, yield strength, and fracture toughness scale, at best, linearly with density. Novel integration schemes may be required to enable integration of materials with $\kappa < 2.0$. To realize the lowest effective permittivity of the integrated structure, dielectric barriers or liners will be needed. This drives the development of new materials with lower κ to replace Si_3N_4 for Cu barrier, etch stop, and hard mask applications. Solutions with the lowest κ must contain porous materials, air gap structures, or both.

Among the new interconnect approaches being suggested, optical interconnection imposes stringent demands on dielectrics. If Si/SiO_2 are used as the optical waveguide materials, process development is required to enable deposition and patterning of materials with sufficiently low loss at temperatures compatible with CMOS. For polymeric systems, materials with greater optical contrast are needed to enable a small turning radius (Δ refractive index > 0.5).

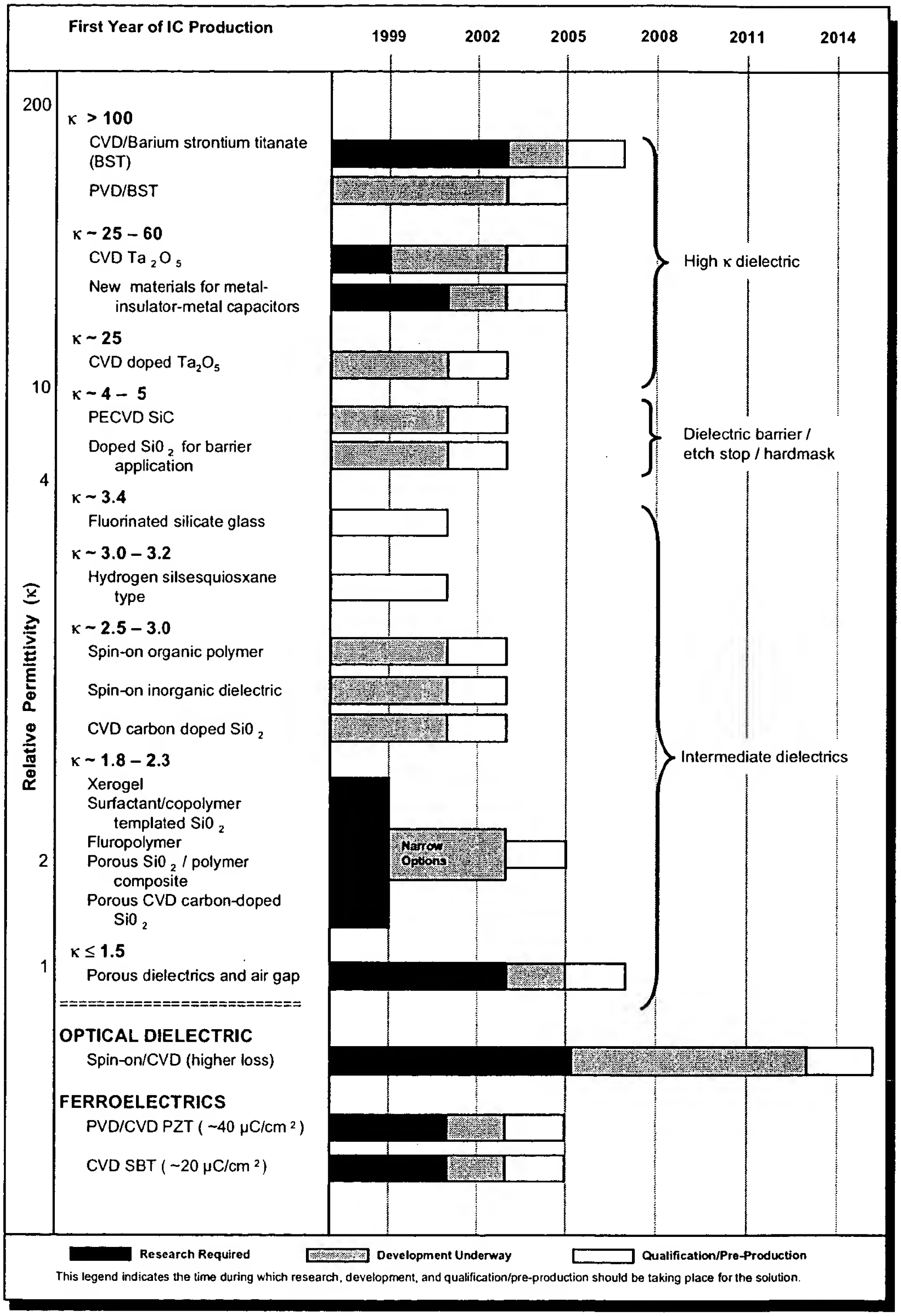

Figure 30 Dielectric Potential Solutions

CONDUCTOR POTENTIAL SOLUTIONS

The introduction of copper wiring occurred at the 220 nm technology node in MPUs where performance was being limited by the conductivity of the aluminum-alloy conductor. SoC will be the next class of products to use copper, again for performance reasons. Although DRAMs will also need Cu for the highest speed memory, process maturity and cost will determine the technology timing. Electrochemical deposition (ECD) is currently the preferred method for producing the copper conductor film, however, the required barriers and nucleation layers are still deposited by physical vapor deposition (PVD) or ionized PVD (iPVD). Damascene process flows are being used for copper pattern definition rather than reactive ion etching; this increases the dependence of interconnect on chemical mechanical polishing. Refer to Figure 31.

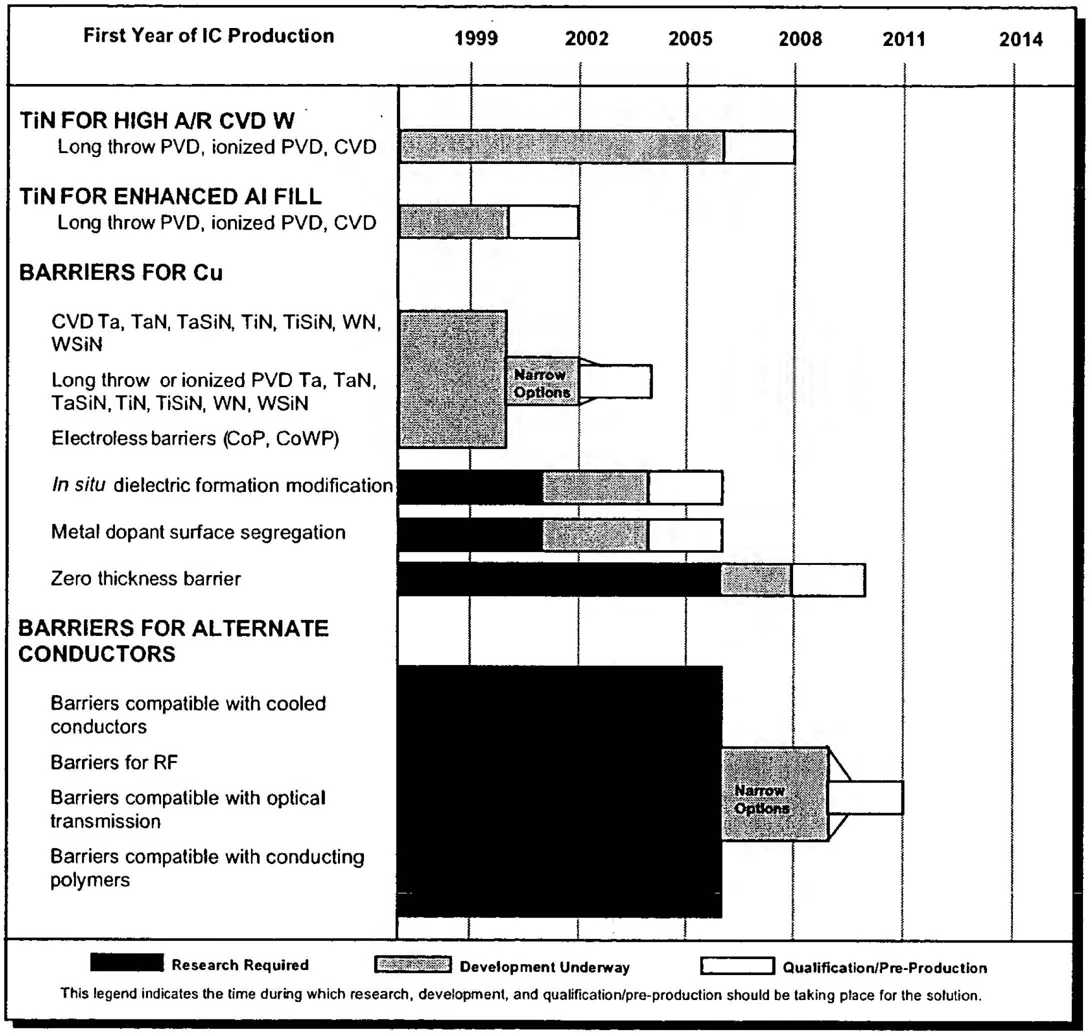

Figure 31 Barrier Potential Solutions

Barrier, nucleation and conductor solutions are available for stated technology requirements until 2004, as indicated in Figure 32. Beyond this generation, the desire to maintain or reduce the effective Cu resistivity, while migrating to reduced critical dimensions at higher aspect ratios, creates a need for increased research into and development of thin, conformal barriers and alternative Cu fill technology. DRAM utilizes the most

aggressive metal pitch of the major product categories. Tungsten and aluminum alloy wiring will be used for DRAMs until at least the 100 nm technology node. Managing defects for 130 nm is already difficult and continued defect density management is necessary for long-term success. The contact aspect ratios for DRAMs utilizing stacked capacitor storage cells are the most aggressive on the roadmap and need special focus. SoC will eventually utilize even more levels of metal than MPUs for incorporating the capacitors, inductors and other passive elements that will be integrated on the chip.

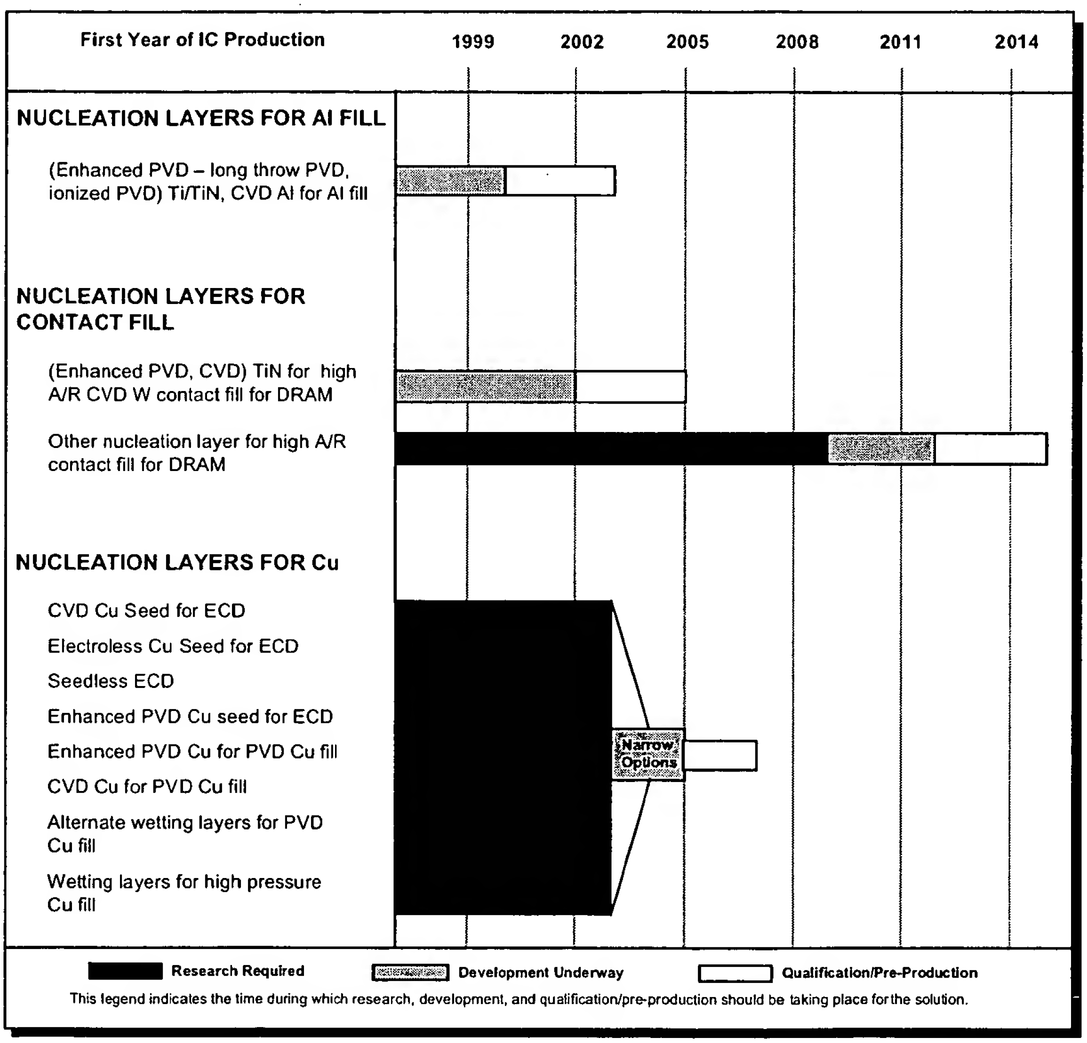

Figure 32 Nucleation Potential Solutions

CONDUCTOR POTENTIAL SOLUTIONS ≥100 nm

Development of a tungsten (W) conductor solution compatible with the thermal processing capability of low κ dielectrics is needed for mixed conductor applications. Contact aspect ratios of 13:1 are expected by the 100 nm node for stacked capacitor DRAM. No current solutions exist to meet these fill requirements and

R&D of advanced CVD W processes is necessary. Long throw PVD, ionized PVD and CVD Ti and TiN are also being developed as the contact and barrier solutions for this high aspect ratio CVD W process. Figure 33 shows the conductor potential solutions.

Advanced Al fill technology is being developed as a conductor potential solution for dual damascene DRAM wiring. Enhanced PVD (long throw PVD, ionized PVD, other PVD) and CVD Ti and TiN barriers and nucleation layers, along with CVD Al as a wetting layer, are the enablers for these enhanced Al fill processes. The potential yield and reliability improvements of these technologies must be assessed in light of their increased capital cost and process complexity compared to the traditional RIE defined W plug/Al wiring. Even more than MPUs or SoC, DRAM will continue to be driven to adopt the overall lowest cost solution.

Second generation, enhanced electrochemical deposition (ECD) for Cu conductors is currently being developed. Improvements in tools, electrical waveforms and plating chemistry are being explored to enable fill of higher aspect ratio dual damascene structures. Closed-loop bath recycling systems may ensure controlled chemistries are available at the wafer. Long-throw PVD and ionized PVD Ta, TaN and TiN (and combinations of these materials) barriers for Cu are in production at the 180 nm node. Additional binary and ternary films, both PVD and CVD, WN, TiSiN, TaSiN and WSiN, are also potential solutions to fill the requirement for thin, conformal barriers. CVD and electroless techniques appropriate for barrier deposition and nucleation layers offer improved conformality and will challenge the dominance of enhanced PVD for Cu dual damascene barriers. Improvement in conformality of seed layers for ECD is also necessary. Enhanced PVD, CVD and electroless techniques are all being developed as potential solutions.

Third generation ECD fill research is underway to further improve high aspect ratio fill at reduced critical dimensions. ECD Cu will face competition from alternative dual damascene Cu fill techniques such as CVD, CVD/PVD fill and high pressure flow. Alternative conductor materials may also be explored. At the 100 nm node, qualification will commence after an expected narrowing of these options. Dielectric barriers for Cu, deposited by CVD techniques, or formed *in situ* by modification of the low κ dielectric films, will be explored. Thin conformal metal barriers deposited by CVD techniques will compete with barriers formed *in situ* by diffusion and segregation of metal dopants to the Cu interfaces and surfaces. Atomic layer deposition (ALD) is another technique for depositing thin, conformal films and offers the further opportunity to do materials engineering using multiple thin layers with different components. Selective deposition of metallic barriers (such as CoP, CoWP, or others) may also prove viable for copper passivation. Nucleation layer potential solutions for the 100 nm node are CVD Cu, electroless Cu, seedless ECD directly on barrier layers and alternate wetting layers.

CONDUCTOR POTENTIAL SOLUTIONS < 100 nm

Cu interconnect, along with low κ dielectrics, will continue to be used for technology nodes below the 100 nm generation. However, these material solutions alone will not be adequate to meet future performance requirements. Design and packaging must play a central role in mitigating future interconnect related problems.

It is necessary to reduce the 2.2 μΩ-cm conductor effective resistivity specification that is characteristic of the barrier/Cu conductor. A potential solution that will give some modest lowering of resistivity, is elimination of Cu barriers through low κ dielectric modification to prevent Cu diffusion. Certain low κ dielectric materials themselves may already exhibit sufficient barrier properties to copper and would meet the zero thickness barrier requirement. More significant reductions of conventional Cu interconnect resistivity can be achieved through lowering the chip operating temperature and this can also dramatically increase the number of superconductor material alternatives. Other potential solutions include the use of 3D devices and on-chip/off-chip RF and optical interconnect. Research is needed to assess the viability of these and other potential solutions.

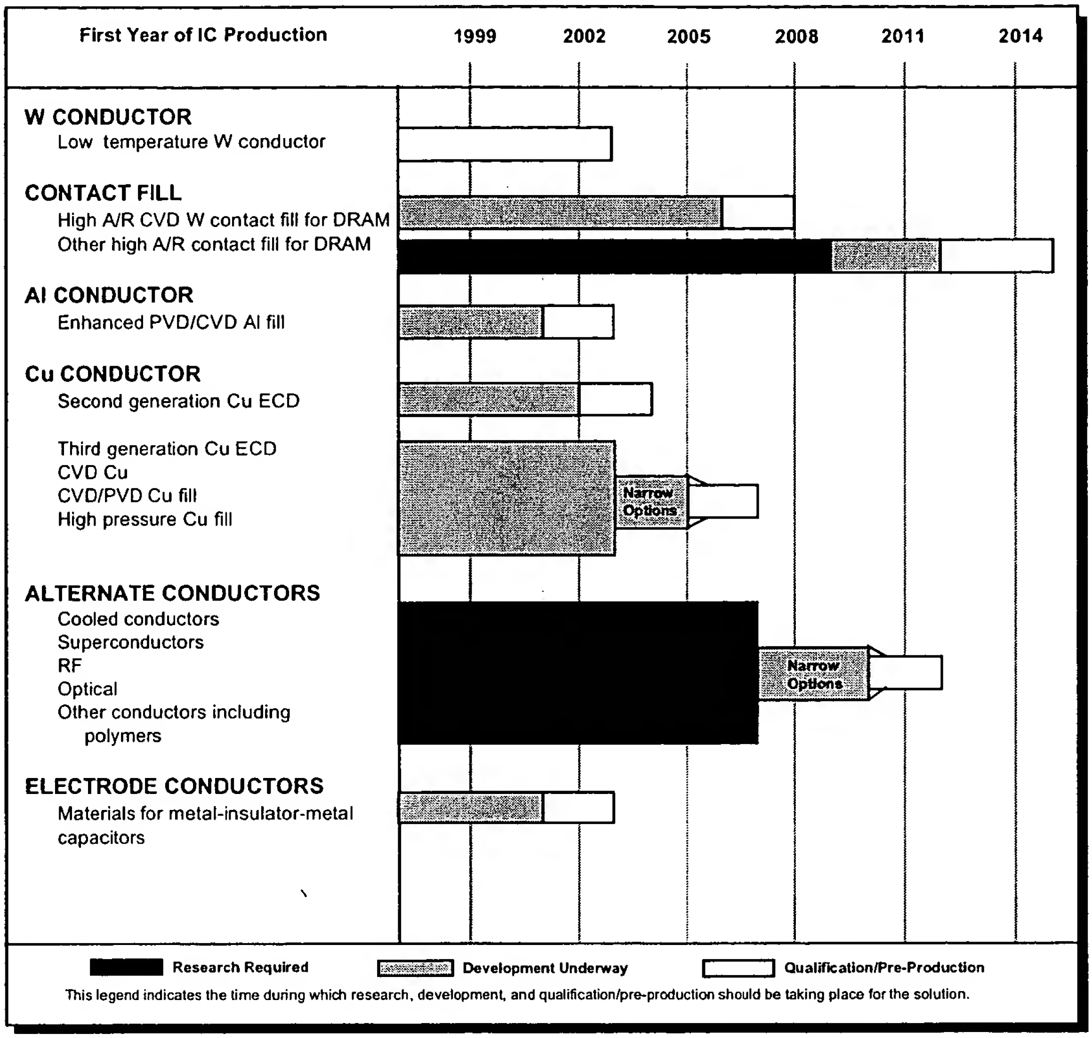

Figure 33 Conductor Potential Solutions

PLANARIZATION POTENTIAL SOLUTIONS

Chemical mechanical polishing is likely to remain the dominant metal and dielectric planarization technique, as indicated in Figure 34. CMP will continue for some time, either for conventional silicon dioxide ILD polishing over aluminum, or for polishing the pre-metal oxide dielectric. Direct polishing of low κ materials will be required, for stop-layers and other integration schemes. The planarization of dielectric layers deposited over vertical capacitor structures, such as crown capacitors in DRAMs, will be particularly challenging. Crown capacitors are currently ~1 micron high and will gradually be reduced in size in future generations. Aluminum, tungsten, and copper damascene polishing will be used concurrently for several process generations. Copper and low κ dielectrics have spurred rapid development of tools and consumables optimized to meet interconnect damascene requirements. Activity associated with combining the use of chemical etching, in conjunction with CMP, is defined as chemically enhanced planarization (CEP). CEP is a

potential solution that has both attractive cost of ownership possibilities and some process advantages for defect control. Electrowinning to remove metals electrolytically falls into this general CEP arena. The continual introduction of new materials mandates improved process control for dishing and erosion. Pattern dependency remains a key issue, as well as reducing defects and metallic contamination. Thinning of conductors in wide features (dishing) and excessive removal of both dielectrics and conductors in tightly spaced features (erosion) creates variability in RC and needs to be minimized. Allowable dishing and erosion targets have been listed in Tables 46a and b. The 2005 requirement that specifies a zero tolerance for erosion sends a message that alternative solutions must receive research focus. There are few identified current alternatives in the "other" category.

Rotary, orbital, ellipsoidal, linear, and other styles of planarization tools each offer unique advantages and disadvantages that must be reconciled by technology applications. There is still no consensus as to whether one type of CMP tool will ultimately dominate all applications, or if the different tool approaches will be used to fit individual applications. Planarization tools with integrated pre- and post-clean capability have been developed, but with the multitude of cleaning options, integration will be driven only if there are demonstrated cost benefits. Offering a variety of integrated cleaning modules available for each CMP tool might facilitate their integration. Similarly, *in situ* metrology and endpoint must be integrated into CMP tools for automatic process control.

CMP consumables must continue to meet the needs of several process modules. Continuous reductions in erosion, dishing, scratching, and particle density will be needed. Parallel improvements in tools, pads, and slurries will be needed for some time to meet these needs. Reductions in consumables costs is also desirable. The proliferation of layers to address integration issues has increased the need for slurries with specified (ranging from low to high) selectivity. Abrasive pads that eliminate or reduce the use of slurry/chemicals are an attractive enhancement with waste reduction and potential process benefits.

Increasing demands will be made on post-CMP cleaning technology. It will be necessary to remove slurry residue and residual copper from polished wafers while preventing corrosion or pattern damage. Several different types of cleaning technology are under development. These include all combinations of brush and spray with and without megasonic excitation. Continuing research in new chemical additives will also be required; these will be used for corrosion protection, metal ion chelation, and particle removal. The use of supercritical fluids, which are finding general applications in via/trench clean, may be applied here. Parallel improvements in defect detection technology must occur. Continued improvements in waste stream control and contaminant reduction are a must. Ideally, CMP processes should be designed to produce a minimum of environmentally deleterious waste, especially Cu and other metals.

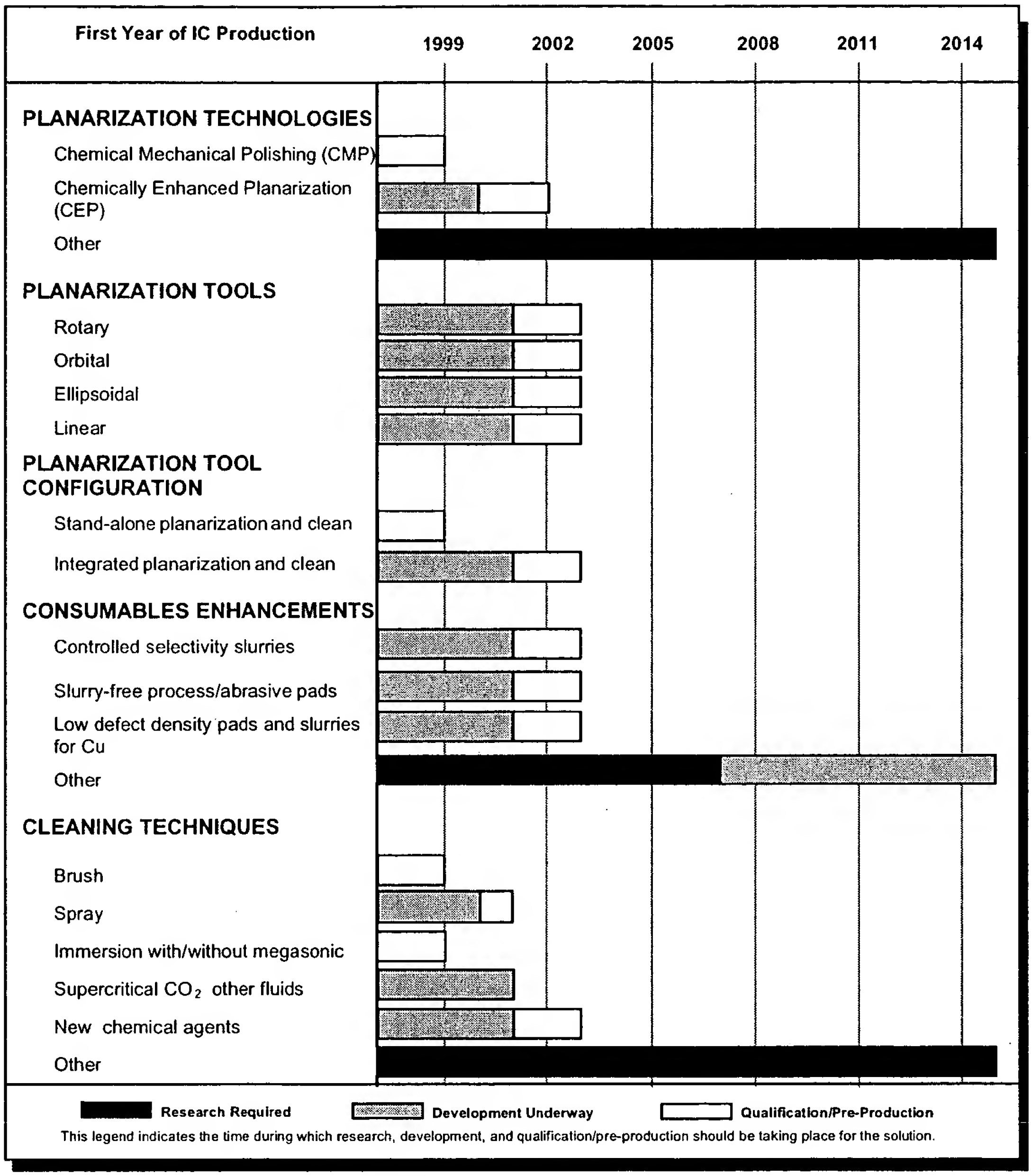

Figure 34 Planarization Potential Solutions

ETCH POTENTIAL SOLUTIONS

Plasma etching of interconnect structures will be required throughout the ITRS forecast period, as shown in Figure 35. Subtractive metal etch, the standard for pattern transfer for many decades, will continue to be used for DRAM until at least 100 nm; there may also be limited applications in logic products with copper

conductors. RIE etch of high A/R aluminum conductors for DRAM 100 nm and 70 nm technology nodes is expected to be extremely difficult and will require continued development by tool suppliers. Contact/via etch for all product classes will extend out to 50 nm. Damascene and dual damascene approaches will be utilized with copper conductors.

Geometric issues, such as smaller feature sizes, higher aspect ratios, and profile control, will have a major impact on etch technology. Reactive ion etching (RIE) will find applications out to about 130 or 100 nm, after which time high-density plasma (HDP) tools will be required to meet the critical etch needs. The driving force for this is the ability for high rate etching of small features with accurate dimensional control and minimized aspect-ratio-dependent etching (ARDE). Porous materials are particularly sensitive to distortion, and geometric control is a key etch development need. Etch processes must not introduce electrical, chemical, or physical damage; for the 70 nm node, new processes such as neutral stream, are a potential solution. Damascene and dual damascene structures and associated incorporation of low κ and high κ materials will require new etch processes. Development of needed etch capability must be timed to match the permittivity trend in the dielectric potential solutions roadmap. <u>A detailed matrix enumerating technical drivers and requirements for etching is presented in a supplemental table linked to this chapter.</u>

Damascene approaches may change the approach to interconnect photoresist stripping and subsequent cleaning. The use of hard mask materials and oxygen-based chemistries for etching organic low κ dielectrics enables *in situ* stripping of the photoresist during the trench, contact or via etch steps. Dry stripping alone may be insufficient to remove residues and particles from structures with high aspect ratios without attacking the low κ dielectrics or copper\barriers. Wet chemicals or other techniques including the use of supercritical fluids can be effective and may be necessary. Alternative stripping gases, such as hydrogen-reducing chemistries, might be needed for porous silicon oxide or similar low κ materials.

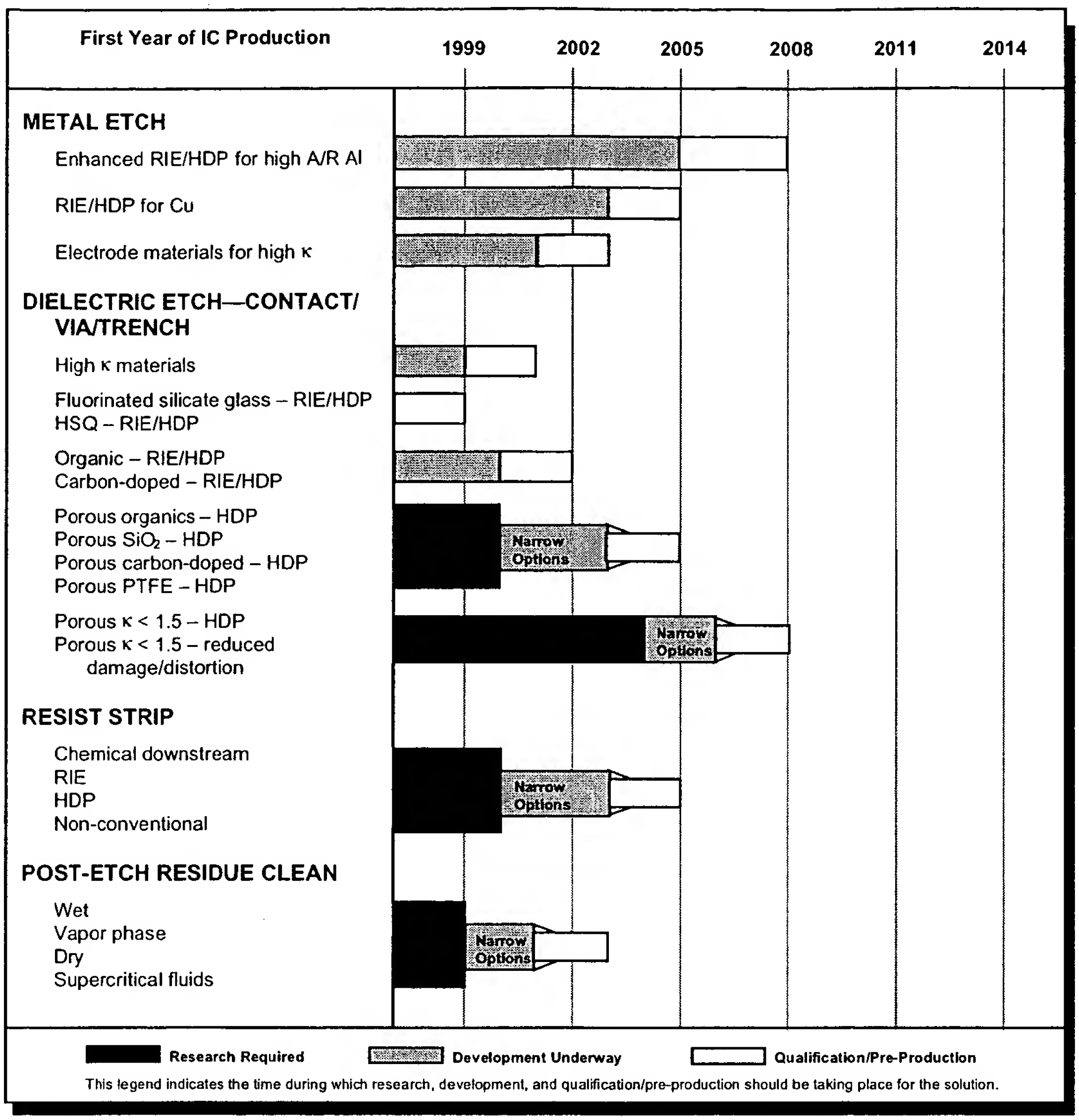

Figure 35 Etch Potential Solutions

Other issues that will affect the development of future etching technologies include the development of new chemistries that are compatible with ESH mandates, selectivity needs, and electrical requirements. These are listed in Table 50.

RELIABILITY

Damascene structures may change the approach to interconnect photoresist stripping and subsequent cleaning. The use of hard mask materials and oxygen-based chemistries for etching organic low κ dielectrics enables *in situ* stripping of the photoresist during the trench, contact or via etch steps. Dry stripping alone may be insufficient to remove residues and particles from structures with high aspect ratios without attacking the low κ dielectrics or copper and its barriers. The implementation of porous silicon oxide or similar low κ materials may allow the continued use of traditional oxygen-based stripping processes.

Copper metallization promises significant interconnect reliability improvement but presents numerous material integration and reliability challenges. Since copper readily diffuses into silicon and most dielectrics, it must be encapsulated with metallic (such as Ta, TaN) or dielectric (such as SiN, SiC) diffusion barriers to prevent electrical leakage between metal wires and degradation of transistor performance. Cu diffusion is also greatly enhanced by electric fields imposed between adjacent wires during device operation, and absolute barrier integrity is crucial to long term device reliability. As barrier thickness scales with metal width to meet effective resistivity goals, copper containment becomes increasing more problematic, and eventually new copper passivation techniques and/or diffusion-resistant dielectrics are needed to provide "zero thickness" solutions.

Copper, unlike aluminum, has no self-passivation layer. Therefore, surface diffusion is expected to dominate electromigration behavior, and material interfaces will play a key role in determining overall reliability. Maintaining the mechanical and electrical integrity of dielectric and metal barriers, particularly at their critical corner juncture, will also be essential to prevent catastrophic copper diffusion between metal leads. CVD copper barriers and seed layers, while providing scaling relief, bring additional integration concerns, and the impact of texture and intermixed CVD/ECD copper layers must be understood.

The integration of new low κ dielectrics needed for performance enhancement bring numerous reliability concerns that include thermally or mechanically-induced cracking or adhesion loss, poor mechanical strength, moisture absorption, time-dependent behavior, texture effects, and poor thermal conductivity. The typical thermal conductivity of low κ dielectrics is less than one third that of oxide, leading to higher metal wire temperatures and enhanced electromigration. Bi-layer or embedded oxide/low κ dielectric schemes may be required to enhance the mechanical strength and heat dissipation of future low κ dielectric systems in addition to novel packaging techniques.

Computer-aided design (CAD) tools will need to incorporate contextual reliability considerations in the design of new products and technologies. It is essential that advances in failure mechanism understanding and modeling, which result from the use of improved test methodologies, be used to provide input data for these new CAD tools. With these data and smart reliability CAD tools, the impact on product reliability of design selections can be evaluated.

New CAD tools need to be developed that can calculate degradation in electrical performance of the circuit over time. The inputs used would be the predicted resistance increases in interconnect wires and vias in the circuit based on the following:

- wire length
- current densities expected for the currents required by the circuit
- calculated local operating temperature, which includes the effects of Joule heating in the circuit element and elsewhere

These tools will need to become an integral part of the circuit designer's tool set to help predict product reliability before processing begins and to develop solutions that anticipate technology and thereby accelerate their introduction.

Expanding use of technology in assembly, such as area-array bumps, need to be considered and integrated with circuit, material, and process selections in order to maintain product reliability in the future. This is especially important to encompass low κ dielectrics and assembly-related process steps, such as under-bump fill, which may be performed on the wafer.

Extensive research is needed to fully understand the multi-variable nature of copper and low κ interconnect reliability and provide accurate models for designed-in reliability. The fundamental limits of copper metallization must also be explored to assess technology extendibility, especially to feature sizes where electron surface scattering effects become a significant contributor to resistivity (< 50 nm for Cu). Finally, reliability studies of alternative conductor systems must also be considered for long term needs to align future interconnect research.

SYSTEMS AND PERFORMANCE ISSUES

INTERCONNECT PERFORMANCE

The adequacy of near term interconnect technologies (copper wires and low κ dielectrics) to continue meeting the design performance requirements for ICs fabricated for succeeding technology nodes or the SIA scaling factor (0.7 × per technology node) varies with the intended function of the interconnect net. For a constant span of gates (such as 40 gates), the signal delay time for local wires, being a very small fraction of a clock cycle, is expected to decrease at a rate similar to the reduction of the gate propagation delay as a function of technology scaling. This trend is expected to continue down to the 70 nm or 50 nm nodes, at which point the signal delay for local wires will begin to increase. The delay for intermediate wires in terms of half the perimeter of a functional block will grow only slightly with technology scaling. Conversely, crosstalk and noise for local wires (and some intermediate wires) are expected to increase with decreasing wire pitch. The signal delay time for global wires will continue to increase with technology scaling primarily due to the increasing resistance of the wires and their increasing lengths (delay for a non-repeated wire increases with the square of wire length). Power distribution at constant voltage through equipotential wires to all V_{dd} bias points requires increasingly lower resistance global wires to avoid the voltage drop problem. The reason for this is the increasing power supply current, related to the decreasing V_{dd}, is causing an increased voltage drop between power supply and the bias point, for fixed global wire resistance. Consequently, this requirement demands increasingly lower resistance paths from the power supply to the V_{dd} bias points. This need is being partially addressed by the introduction of ball-grid-array packaging technology that distributes power feeds across the area of the chip, eliminating much of the on-chip lateral power feeds through relatively high-resistance global wires. Interconnect nets for distributing clock signals and power can dissipate up 40–50 % of the power on the chip, which may exceed 120 Watts.

SYSTEM LEVEL INTEGRATION

System level integration encompasses the physical and functional assembly of a system's macro functions to achieve its desired operating characteristics. Assembly of individual functional components (such as bare chip or block functions on a single chip) into the system must comprehend all the performance and reliability requirements imposed on the system. These requirements currently are met through the distinctly separate functions of on-chip interconnect, packaging and board-level technologies. Solutions currently being pursued in these domains are described in this chapter and in the *Design* and the *Assembly & Packaging* chapters. Potential solutions in which traditional package or intra-chip interconnect functions are being merged in the package also will be identified. However, as cost, bandwidth, thermal and pin-out requirements become even more demanding, revolutionary new interconnect/packaging solutions must be sought. These new solutions may completely merge interconnect, package and (perhaps) board functions into fully integrated systems. These approaches will include both system-on-package (SoP) and system-on-a-chip approaches.

CROSSCUT ISSUES

DESIGN AND MODELING & SIMULATION

Significant synthesis and verification challenges for design and modeling & simulation will arise from technology scaling and the associated increases in functional density, along with new SoC requirements. Designers must compensate for the increasing importance of inductance and crosstalk as well as increased power dissipation. Joule heating and current crowding in complex wiring systems must be carefully assessed as current densities rise. New simulation techniques are needed that incorporate improved performance and reliability methods. Signal and clock delays in global wiring have been identified as the primary performance limiter for interconnects. While selective use of repeaters can optimize critical speed paths, new design architectures are needed to mitigate the global delay. Closer coupling between process capability, manufacturing variability, technology modeling, synthesis, physical design, and design verification will be required to meet the ITRS density, performance, and reliability challenges for interconnects (see *Design* and *Modeling & Simulation* chapters).

METROLOGY

Feature size reduction, new materials, and damascene structures present metrology challenges for the development and production of the interconnect portion of chips. Critical dimension measurements are needed for very high aspect ratio features and ultra-thin barriers. Dedicated wafers for metrology and the use of non-revenue monitor wafers will give way to in-process measurement of product wafers. Metrology integrated into cluster tools as either a metrology station or with *in situ* sensors, along with control software, is a trend that should benefit interconnect. Techniques must be developed to accommodate the increased complexity of the wiring levels of future chips. Other metrology challenges include measuring resistivity and dielectric constant at high frequency, adhesion, and mechanical properties. Additional details can be found in the *Metrology* chapter.

Table 49 Interconnect Metrology Needs and Potential Solutions

KEY AREAS	SUMMARY OF NEEDS	POTENTIAL SOLUTIONS
New materials	Measurement of dielectric constant at high frequency	Extend current capability to > 40 MHz and develop test structures suitable for <100 nm nodes
	Measurement of pore size and volume on low κ insulators	Acoustic, ellipsometric and positron annihilation spectroscopy
	Contamination monitoring	Rapid TXRF and VPD DSE/TXRF
	Verify hydrophobicity of porous low κ materials	Infrared measurement of water content
Dimensional control	Control of planarization processes for reduced dishing and erosion	*In situ* sensors and profilometry are potential measurement solutions
	Control low κ thickness and uniformity	Spectroscopic ellipsometry
Aspect ratios for fill and etch	CD control of dual damascene features	Develop model based CD measurement

TXRF—total X-ray fluorescence spectroscopy   VPD DSE/TXRF—vapor phase deposition droplet scanning etch

DEFECT REDUCTION

As the wiring density and number of interconnect levels increases, improvements in defect detection and reduction are required to maintain product yield. Real time detection and analysis of defects is also required for yield improvement and process control to maintain factory product flow. Defects associated with high aspect ratio damascene structures will be difficult to identify in patterned multi-layer low κ dielectrics. New techniques for defect detection and analysis, as well as improved defect reduction approaches, will be needed to support future interconnect manufacturing processes (see *Defect Reduction* chapter).

ENVIRONMENTAL SAFETY AND HEALTH

Interconnect technologies carry unique environmental, safety, and health (ESH) challenges (see Table 50). The performance-driven need for new materials (low κ dielectrics, high κ dielectrics, copper conductors and barriers, and others) and processes (electrochemical deposition, CVD metal/dielectric deposition, Cu/barrier CMP, low κ/high κ etch/clean, and others) brings numerous ESH concerns, especially considering the rapid pace of insertion. Continuous improvement is needed in methods for treating and recycling CMP slurries and copper electrochemical deposition baths. Both wet and dry processes will continue and require appropriate abatement; the introduction of new metal and dielectric materials adds to these ESH challenges. Closed-loop control and replenishment are potential solutions for wet processes. The new materials, precursors, and processes that will be required for future low κ dielectrics and CVD conductor/barrier depositions must also be carefully screened for ESH issues during the early phase of development. Reaction product emissions, health and safety properties, materials compatibility with equipment and other chemical components, flammability and reactivity must be predetermined to ameliorate ESH impact. The industry must also strive to reduce chemical emissions and waste (copper plating solutions, CMP slurries, acids/solvents, PFCs, water use) through process optimization, use of alternative chemistries, recycling, and/or abatement.

Table 50 Interconnect ESH Needs and Potential Solutions

KEY AREAS	SUMMARY OF NEEDS	POTENTIAL SOLUTIONS
Advanced metallization and dielectric materials	Utilize lowest ESH impact deposition processes Increased chemical utilization efficiency	Use lowest ESH impact solvents for spin-on processes Develop "zero waste" deposition methods Identify ESH issues with CVD precursors Develop safe precursor delivery systems Develop emissions models for vapor phase systems Utilize lowest ESH impact process chemistries for CVD Improve chemical utilization efficiency through endpoint detection and reactor design
Planarization	Lowest volume of chemicals and water used and disposed in CMP and post-CMP cleans processes Utilize lowest ESH impact chemistries for CMP and post-CMP cleans processes Low-energy and low-chemical consumption methods for removal of Cu from wastewater Water reclaim and reuse	Decrease amount of slurry required for CMP Develop slurry recycling methods Develop alternatives to slurry-based CMP processes Develop non-chemical consuming planarization methods Reduce water consumption Develop more efficient techniques for post-CMP rinsing Develop water recycling systems to reuse CMP and post-CMP wastewater Develop lowest ESH impact CMP and post CMP cleans chemistries

Table 50 Interconnect ESH Needs and Potential Solutions (continued)

KEY AREAS	SUMMARY OF NEEDS	POTENTIAL SOLUTIONS
Electrochemical deposition of Cu	Reduce generation and handling of hazardous waste Lowest ESH impact process chemistries Reduce employee exposure to chemicals	Extend Cu plating bath life using monitoring and replenishment Develop techniques for bath recycle Minimize quantity of rinse water Develop and utilize lowest ESH impact plating chemistries Develop "zero waste" copper deposition processes Design process tools which minimize exposure to chemicals
Plasma processes	Lowest ESH impact process chemistries Reduce power consumption	Optimize chamber clean and etch processes to increase utilization efficiency of PFCs Develop low CoO abatement and recycle systems for PFCs Develop lowest ESH impact alternative etch chemistries and chamber cleaning processes that do not emit high global warming potential by-products (PFCs) Develop predictive plasma emissions models Monitor and optimize tool systems (energy-efficient pumps, idle energy usage, recycle waste heat) Reduce RF plasma energy consumption and develop alternate low-energy plasma generating systems Develop new heat transfer methodologies in vacuum systems

CONCLUSION

Managing the rapid rate of materials introduction and the concomitant complexity represents the overall interconnect challenge. For the long term, material innovation with traditional scaling will no longer satisfy performance requirements. The delay associated with global wiring and the management of crosstalk and noise must be addressed with increased development activity. System-on-a-chip may alter the picture or technology timing because chip functionality can be traded for scaled density in the marketplace. Ultimately, interconnect innovation with optical, RF or vertical integration combined with accelerated efforts in design and packaging will deliver the solution.

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS
1999 EDITION

FACTORY INTEGRATION

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FACTORY INTEGRATION[31]

SCOPE

The transition to 300 mm wafers now underway affords the most significant opportunity in the history of the semiconductor industry to collectively and systematically control and lower manufacturing costs. Preserving the decades-long trend of 30% per year reduction in cost per function in the face of this major transition requires capturing every possible cost reduction opportunity.

The unparalleled economic behavior resulting from Moore's Law has been sustained by several factors: continuous reduction in feature sizes; improvement in yields to near 100%; increasing wafer size; and *improved manufacturing performance*. Factories have maintained a constant historical cost per unit area, and technology has delivered ever-increasing numbers of transistors per area. As a result, the industry has flourished.

Continuation of this remarkable record now faces several challenges that threaten to slow the industry's growth. Lithography and CMOS scaling are well documented as key technology risks, as are design limitations. Manufacturing risks are decreasing productivity trends, wafer size conversion[32] inefficiencies, and the inability to meet cost targets.

To deal with these manufacturing risks, the following fundamental attributes of semiconductor manufacturing must be vigorously pursued: maintaining constant cost per area, decreasing time to ramp to high volume production, and increasing flexibility to adapt to new business models.

Maintaining cost per unit area—Manufacturing cost per unit area is a measure of capital productivity. The cost of a factory has grown significantly each year, from $10M in the 1980s, to almost $2B in 1999.[33] Although the number of wafers processed per unit time has not changed, significant improvements in the performance of equipment combined with larger wafers have enabled a constant cost per unit area. Even with yield maximized and wafer size generations extended, the factory must continue to control cost. This must continue notwithstanding the upward cost pressure of technological advancements.

Decreasing ramp time—Recent work has shown that decreasing time to ramp a factory to production has more impact economically than most reductions in static operating costs.[34] New factories must be built and ramped to mature production much faster than today. Similarly, existing factories must be upgraded faster and with a minimum impact on ongoing production.

Increasing flexibility to business needs—Business opportunities and efforts to control costs have led to globalization of manufacturing enterprises. With the decrease in cost of electronic components, new markets continue to open, and the new business models developing in response to this market diversity are challenging responsiveness of factories.

From these considerations arise the difficult challenges for the factory. These are described in the following section as managing complexity; optimizing the factory in the midst of constantly changing requirements; and increasing extendibility, flexibility, and scalability (EFS). To elaborate these difficult challenges and identify potential solutions, the body of the chapter is divided into *thrusts* roughly matching the functional organization of a semiconductor factory. These thrusts are *Factory Operations*, *Production Equipment*,

[31] Factory integration is the combination of factory operations, production equipment, facilities, material handling and factory [software] systems working in a synchronized way to profitably produce complex products for a time-sensitive market.

[32] Because of the high cost of a wafer diameter conversion, the time between conversions is increasing, so that the annualized cost reduction due to this factor has now dropped to 2–3% for the 300 mm generation.

[33] Strategies for determining or dealing with the upper limit of factory cost are beyond the scope of this chapter.

[34] Robert Leachman, John Plummer, Nancy Sato-Misawa, "Understanding Fab Economics," University of California at Berkeley, *Engineering Systems Research Center Report ESRC 99-05 (CSM-47)*, (June 1999).

Material Handling, Factory Systems, and *Facilities*. *Factory Operations* is portrayed as a context for issues and actions of the other thrusts. Similarly, *Complexity Management* is portrayed as a context for *Factory Optimization* and *EFS*. Figure 36 illustrates the relationships between thrust areas and difficult challenges.

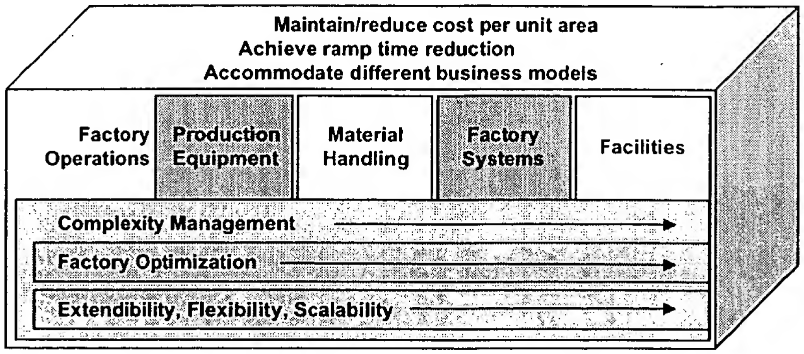


Figure 36 Schematic Showing the Factory Integration Thrusts and Difficult Challenges

FACTORY FOCUS AREAS

High-volume factories historically push the manufacturing technology envelope and are the focus of this chapter. The differing requirements between high-product-mix and low-product-mix factories are also addressed.[35]

As shown in Figure 37, a semiconductor "factory" extends across several manufacturing domains. As indicated, the scope of the current chapter is limited to wafer-level manufacturing of integrated circuits.[36]

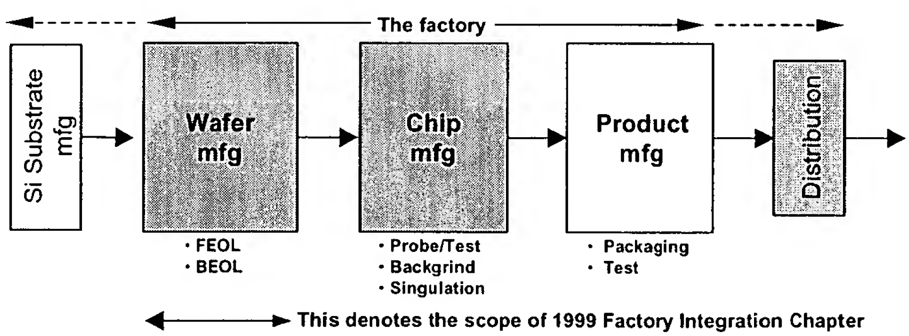


Figure 37 Factory Integration Scope

Note: For this year's roadmap, the scope of factory integration has intentionally been kept narrow, as shown above, to ensure the limited topics addressed are not compromised in terms of content and quality. The factory integration roadmap will be broadened in future periodic updates.

[35] Subsequent editions of the ITRS' factory integration chapters will address a broadened scope of semiconductor manufacturing.

[36] Although the ITRS technology nodes are stylistically maintained in this chapter, factory improvements are generally ongoing or are synchronized with major re-capitalization, such as wafer size transitions.

DIFFICULT CHALLENGES

Difficult challenges associated with factory integration have been grouped into three categories spanning multiple technology nodes and cutting across the five factory thrust areas. Responses to these challenges are often linked to the technology introductions as a matter of industry convenience to minimize disruptions to operating factories.

Management of factory complexity—Complexity management is the management of the different factory, process, and product elements and their inter-relationships. Since the number of these elements continues to increase rapidly, management of factory complexity is becoming increasingly important and more difficult.

Optimization of factory elements—Factory optimization refers to the processes that enable sound and timely business decisions to be made in a resource-constrained environment. This environment is subjected to rapidly changing and uncertain business and technology conditions.

Factory extendibility, flexibility and scalability (EFS)—These relate to maximizing capital productivity and prolonging useful factory life. Factory extendibility (leveraging factory usage across several technology nodes), factory flexibility (adaptability to change), and factory scalability (inherent ability to sustain greater than specified capacity) refer to the need for continuous and nondisruptive factory operation in the face of significant operational changes.

A summary of issues corresponding to these three Difficult Challenges is found in Table 51, with additional details discussed below.

Table 51 Factory Integration Difficult Challenges

DIFFICULT CHALLENGES	*SUMMARY OF ISSUES*
Complexity Management	Rapidly changing business needs and globalization trends • Increasing rate of new product and technology introductions • Globally disparate factories run as single "virtual factory" • Need to meet regulations in different geographical areas Increasing process and product complexity • Explosive growth of data collection/analysis requirements • Increasing number of processing steps • Multiple lots in a carrier Larger wafers and carriers driving ergonomic solutions • Increasing expectations for material handling automation systems Increased reliance on factory systems • Multiple system interdependencies • Co-existence of new factory systems with existing (legacy) systems
Factory Optimization	Meet customer ontime delivery • Balanced throughput and cycle time • Reduce time to ramp factories, products, and processes Improve Overall Factory Effectiveness (OFE) • Improve all Factory Integration thrust areas Improve factory yield • Control production equipment and factory processes to reduce parametric variation Reduce product and operation cost • Minimize waste and scrap and reduce the number of nonproduct wafers Satisfy all local, state and federal regulations.
Extendibility, Flexibility, and Scalability	Reuse of building, production and support equipment, and factory systems • Across multiple technology nodes • Across a wafer size conversion Factory designs that support rapid process and technology changes and retrofits • Understand up-front costs to incorporate EFS • Determine which EFS features to include and not to include • Minimize downtime to on-going operations Comprehend tighter ESH/code requirements Comprehend increased purity requirements for process and materials

COMPLEXITY MANAGEMENT

Complexity is a measure of the combinations of interrelated physical and operational steps and interfaces required for the fabrication and delivery of semiconductor components. Such complexity arises from both external influences such as business and economic climate, and competitive pressures and internal influences such as decisions based on prevailing business models, technology opportunities, and legacy systems.

External factors include globalization of facilities and suppliers; changing business demands and business models; introduction of new technologies; and increasingly segmented and uncertain semiconductor markets. Internal factors include more complex processes; larger factories; integration of more process steps; and a higher degree of process and product mix within the factories. For example, the number of process steps needed to fabricate an IC is projected to more than double by 2012, thereby increasing the complexity.

There are multiple levels of manufacturing complexity. Distinctions are often made between enterprise, factory, area, and equipment levels. Integration of complexity management between these levels offers the greatest leverage, since this globally improves factory performance, rather than just improving local conditions.

Effective management of semiconductor factories will require efficient accommodation of increasing manufacturing complexity.

FACTORY OPTIMIZATION

Maximizing the following must be done to optimize factory operations:

- Customer ontime delivery
- Product quality and reliability
- Overall factory efficiency

This requires minimizing

- Variation,
- Product cost per layer, and
- Waste, scrap, and environmental impact

While continuing to

- Provide a safe work environment;
- Satisfy all local, state, and federal regulations; and
- Demonstrate continuous improvement.

Very often, such optimization requires choosing options that may conflict with one another.

A significant obstacle to optimizing factory operations is operational variation. For example, reducing variation in equipment performance is a central issue as it affects yield, product reliability, planning, cycle time, customer delivery, overall factory effectiveness, and wafer cost. If equipment performance is inadequate then the risk of scrap or equipment unavailability increases, which results in an increase in ontime delivery variation and schedule slippage. Hence, one needs to identify, understand, evaluate, and minimize sources of variation to improve factory optimization.

Other factors inhibiting optimization include legacy system management, the lack of adequate data management capabilities and understanding of important cause-effect relationships, inadequate decision-making time, and conflicting polices or procedures.

Given a business model, a factory manager must make decisions involving tradeoffs and compromises under resource and time constraints. This is the fundamental reality of factory optimization, since there is never enough time, resources, or information to avoid making difficult choices.

EXTENDIBILITY, FLEXIBILITY, AND SCALABILITY (EFS)

EFS relates to the need to extend the useful life of facilities, equipment and factory systems under a widely varying set of business conditions.

Extendibility—Extendibility refers to prolonging the useful life of the factory across several process generations. The challenge is to introduce new technologies or business models into older factories with a minimum of new capital equipment, learning and training, while limiting major retrofits, re-engineering, and factory disruption.

Flexibility—Flexibility is the ability of the factory and its sub-components to adapt to change. Flexibility consists of two components, "versatility" and "agility." Versatility is how *far* a factory's capability can be stretched (in other words, can a DRAM factory be changed to a logic factory, or vice-versa, in a cost-effective manner?). Agility refers to how *fast* a factory can change from one operational model to another (such as from high-volume/low-mix to high-volume/high-mix product loading.)

Scalability—Scalability refers to a system's intrinsic capacity; how much stretching of the base system is possible? For example, can a 5,000 wafer start-per-week factory software system be scaled up to handle 7,000 or 8,000 wafer starts per week? What systems are affected, and what effort will be needed to achieve the stretch? What are the limiting or critical factors, and can these be adapted without significant problems?

EFS is not free. Its value is company dependent and determined by such business drivers as market segment served, product diversity, volatility of demand, and the company's tolerance for risk.

EFS has the potential to significantly expand the capability and extend the useful life of the factory.

TECHNOLOGY REQUIREMENTS

To evaluate the technology requirements needed to achieve the primary goals described above, and subsequently to identify potential solutions to the difficult challenges that must be met, one can regard the factory as comprising five inter-related and complementary functional areas. These are:

Factory operations covers the set of policies and procedures that are used to control production within a factory.

Production equipment covers both process and metrology equipment and their interfaces to other elements in the factory.

Material handling systems covers transport, storage, identification, tracking and control of direct and indirect materials in a factory.

Factory systems covers computer hardware and software, and includes manufacturing execution and decision support systems. It integrates factory operations such as scheduling, control of equipment and material handling systems, and advanced process control.

Facilities covers the infrastructure of buildings, utilities, and monitoring systems.

The relationship between each technology requirement and each difficult challenge and other related technology thrusts are given in the supplemental material to this chapter.

FACTORY OPERATIONS

Table 52 Factory Operations Technology Requirements

YEAR TECHNOLOGY NODE WAFER DIAMETER	1999 180 nm 200 mm	2002 130 nm 300 mm	2005 100 nm 300 mm	2008 70 nm 300 mm	2011 50 nm 300 mm	2014 35 nm 450 mm
High Volume/Low Mix Factory Requirements						
Factory cycle time per mask layer (non-hot lot) [1, 2]	1.75 days	1.5 days	1.4 days	1.3 days	1.2 days	1.1 days
Factory cycle time per mask layer (hot lot) [1, 2]	1.2 days	1.0 day	1.0 day	1.0 day	1.0 day	1.0 day
Number of lots per carrier	One lot	One lot	One lot	One lot	One lot	One lot
High Volume/High Mix Factory Requirements						
Factory cycle time per mask layer (non-hot lot) [2,3]	1.8 days	1.6 days	1.4 days	1.3 days	1.2 days	1.1 days
Factory cycle time per mask layer (hot lot) [2,3]	0.9 days	0.85 days	0.8 days	0.75 days	0.7 days	0.65 days
Number of lots per carrier	Single lot [4]	Multiple lots	Multiple lots	Multiple lots	Multiple lots	Multiple lots
Common Requirements across Both Factory Types						
Groundbreaking to first full loop wafer out	< 18 months	< 16 months	< 14 months	< 12 months	< 11.5 months	< 11 months
Total number of operators and technicians in the factory	N	0.9×N	0.8×N	0.7×N	0.6×N	0.5×N
Product/ process change-over time	12 weeks	10 weeks	8 weeks	6 weeks	5 weeks	4 weeks

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Notes for Table 52 for Factory Operations Requirements

[1] Assume number of hot lots in the factory is less than 3 % of all lots

[2] Average number of wafers per hot lot ranges between 5 and 10

[3] Assume number of hot lots in the factory is less than 10 % of all lots

[4] Assumes variable number of wafers per lot

Explanation of items

Item	*Explanation*
Factory cycle time per mask layer	*A key metric of time to money. For example, if a process has 20 masking layers, and cycle time per mask layer is 1.5, then total factory (fabrication+sort) cycle time is 20×1.5 = 30 days.*
Number of lots per carrier	*Number of lots in each carrier that needs to be tracked, monitored, and processed at each production equipment. It is also a measure of the extent of "recipe cascading" needed to enable production equipment to run in a continuous (non-stop) mode between lots in the same carrier and between sequential carriers.*
Groundbreaking to first full loop wafer out	*A key metric of new factory ramp-up time. This is the time elapsed in months from groundbreaking start to first full loop wafer out.*
Total number of operators and technicians in the factory	*It is expected the number of factory operators will decrease over time on a relative basis.*
Process/product changeover time	*The time in weeks for a new product or process to be implemented in a working factory (production equipment carry-in to first lot out). About 80% of the current equipment is reused and 20% is new. Furnace and wet process equipment are not replaced.*

The factory operations policy best suited for a particular company is a function of several factors. These include the company's business strategy, the type of factory (high-volume/high-mix or high-volume/low-mix), specific product mix, maturity of the technology employed and product designs, the type of material handling system employed, and the information systems used. While each manufacturer must develop operations policies that fit its individual business model, additional theoretical development is needed to derive and analyze general operational policies. These policies and the related models are needed to capture various combinations of operating points (equipment mix, product mix, process flow, demand volume,

dispatch policy). These models would also help to examine and benchmark a factory's performance in the context of its business model for wafer and product volume (high product mix versus low product mix), factory size (mega-factory versus incremental capacity factory), extended factory and equipment life versus capital replacement.

The principal requirements for factory operations, as listed in Table 52 include reduced cycle time; greater lot assignment flexibility including use of multiple lots per carrier; faster ramp of both new factories and product/process change-overs; and reduction in personnel.

PRODUCTION EQUIPMENT

Table 53 Production Equipment Technology Requirements

YEAR *TECHNOLOGY NODE* *WAFER DIAMETER*	*1999* *180 nm* *200 mm*	*2002* *130 nm* *300 mm*	*2005* *100 nm* *300 mm*	*2008* *70 nm* *300 mm*	*2011* *50 nm* *300 mm*	*2014* *35 nm* *450 mm*
Relative capital cost [1]		<1.3×200 mm [2]	< 98% of previous node	<98% of previous node	<98% of previous node	< 1.3×300 mm
Relative consumables, gases, chemicals, exhaust, emissions, and utilities		<1.0×200 mm	10% less than previous node	10% less than previous node	10% less than previous node	10% less than previous node
Bottleneck production equipment OEE [3] (SEMI E79) [37]	75%	87%	89%	91%	92%	92%
Average production equipment OEE [3] (SEMI E79)	55%	65%	71%	78%	80%	82%
Relative equipment footprint		<1.0×200 mm	<98% of previous node	<98% of previous node	<98% of previous node	<1.0×of 300 mm
Relative maintenance and spares cost		<1.0×200 mm	<98% of previous node	<98% of previous node	<98% of previous node	< 120% of previous node
Overall factory non-product wafer usage (per wafer start)		< 16% of production	< 12% of production	< 11% of production	< 10% of production	< 9% of production
% Capital equipment reused from one process node to next	> 70%	> 0%	> 80%	> 80%	> 80%	>20%
Wafer edge exclusion [4]	3 mm	2 mm	1 mm	1 mm	1 mm	1 mm
Production equipment lead time (months from order to full throughput capability) [5]	< 9 months	< 8 months	< 7 months	< 6 months	< 5 months	<5 months
Production equipment installation, including hook-up and qualification cost as a % of capital cost	< 6%	< 0.95× of cost of previous node	< 0.95× of cost of previous node	< 0.95× of cost of previous node	< 0.95× of cost of previous node	< 0.95× of cost of previous node
Process equipment availability [6] (SEMI E10) [38]	> 85%	> 90%	> 93%	> 95%	> 95%	> 95%
Metrology equipment availability [6] (SEMI E10)	> 90%	>95%	>95%	>98%	>98%	>98%
Number of process recipes per carrier	Single	Multiple	Multiple	Multiple	Multiple	Multiple

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Notes for Table 53 for Production Equipment Requirements

[37] SEMI. E79-0299 – *Standard for Definition and Measurement of Equipment Productivity.*

[38] SEMI. E10-0699E – *Standard for Definition and Measurement of Equipment Reliability, Availability, and Maintainability (RAM).*

[1] Moore's law requires 29% cost reduction per function per year. Lithography improvements contribute 15 to 20 % cost reduction per year. A significant part of the remainder must be made up by improvements in factory productivity through better operational efficiency, lower costs and cycle time reductions. This is very important for production equipment since it is the largest component of factory cost.

[2] See References for a discussion of the basis for the 1.3 ratio. [39,40].

[3] Reused from 1998 Roadmap. [41]

[4] Relevant to basic equipment processing capability only.

[5] This line is intended to drive increasingly better awareness of supply chain management.

[6] Equipment availability includes all components. Examples: process chambers, load ports, wafer handling systems, embedded controllers, mini-environment.

Explanation of Items

Item	*Explanation*
Relative capital cost	*For 130 nm node, it is the ratio of (300 mm equipment capital cost/300 mm throughput in wafers per hour) divided by (200 mm equipment capital cost/200 mm throughput in wafers per hour). For the 100 nm node and beyond capital cost is 98% of previous node assuming the same throughput.*
Relative consumables, exhaust, emissions, and utilities	*For the 130 nm node, relative consumables is a ratio of (300 mm consumables/300 mm throughput in wafers per hour) divided by (200 mm consumables/200 mm throughput in wafers per hour). The same methodology applies for gases, chemicals, exhaust, emissions, and utilities. For the 100 nm node and beyond consumables is 90% of previous node assuming the same throughput. Global warming and general ESH initiatives may force additional tightening of this requirement.*
Bottleneck production equipment OEE	*Overall equipment effectiveness of the bottleneck production equipment. Typically, the bottleneck is the most expensive machine group in the factory. (Refer to SEMI E79 for OEE definition.)*
Average production equipment OEE	*Overall equipment effectiveness of the average production equipment. Typically, the bottleneck is the most expensive machine group in the factory. (Refer to SEMI E79 for OEE definition.)*
Relative equipment footprint	*For the 130 nm node, it is ratio of (300 mm equipment footprint/300 mm throughput in wafers per hour) divided by (200 mm equipment footprint/200 mm throughput in wafers per hour). For the 100 nm node and beyond, footprint is 98% of previous node assuming the same throughput. [Refer to SEMI E72.* [42] *The footprint used here infers to the cost footprint in the SEMI standard.]*
Relative maintenance and spares cost	*For the 130 nm node, it is ratio of (300 mm maintenance and spares cost/300 mm throughput in wafers per hour) divided by (200 mm maintenance and spares cost/200 mm throughput in wafers per hour). For the 100 nm node and beyond it is 98% of previous node assuming the same throughput.*
Overall factory non-product wafer usage (per wafer start)	*Ratio of total non-production wafer consumption divided by total production wafer started for the same period. Typical nonproduct wafers include test wafers, monitor wafers, calibration wafers, dummy wafers.*
% Capital equipment reused from one process node to next	*% of capital (production) equipment quantity that is reused from node N to N+1. Example: if X number of production equipment of node N can be reused for node N+1 and the total number of production equipment for node N+1 is Y, then equipment reuse % is defined as X/Y.*
Wafer edge exclusion	*Dimension in millimeters measured from wafer edge that is not used for printing saleable chips.*
Production equipment lead time (months from order to full throughput in factory)	*Time elapsed between when a purchase order has been placed for a production equipment until the time the equipment has been installed in the factory and qualified to run wafers at the quoted throughput (wafers per hour).*
Production equipment installation, hookup and qualification cost as a % of capital cost	*Ratio of (installation cost + hook-up cost + qualification cost) divided by the capital cost of the production equipment, expressed as a percentage.*
Process equipment availability	*Availability is 100% minus (scheduled downtime % + unscheduled downtime %) of the production equipment. Scheduled downtime and unscheduled downtimes are defined in SEMI E10.*
Metrology equipment availability	*Metrology equipment availability as defined by SEMI E10. This is 100% minus (scheduled downtime % + unscheduled downtime %) of the metrology equipment.*
Number of process recipes per carrier	*Indicates a requirement on all single wafer processing equipment to incorporate the ability to automatically change recipe and process parameters between any two wafers in a carrier and to do so in a continuous manner without interruption or manual intervention.*

[39] SEMATECH. *I300I Factory Guidelines: Version 4.1.* 97063311E-ENG. Austin, TX: SEMATECH. July 15, 1999.

[40] Daniel Seligson, "The Economics of 300 mm Processing," *Semiconductor International*, vol. 21, number 1, January 1998, pages 52-58.

[41] Semiconductor Industry Association. "National Technology Roadmap for Semiconductors: 1998 Update." Austin, TX:SEMATECH, 1999.

[42] SEMI. E72-0699 – *Provisional Specification and Guide for 300 mm Equipment Footprint, Height, and Weight.*

Production equipment includes equipment unit, realtime process control, overall equipment effectiveness, and all factory interfaces including loadports. The scope of production equipment thrust includes process equipment and metrology (both inline and offline) equipment.

Effective design and control of production equipment is central to maintaining, and possibly reducing, the cost of processing each unit area of silicon. Additionally, the rate at which factory costs are increasing must be reduced. The industry will not sustain its historical rate of increasing capitalization costs and, at the same time, maintain historical growth rates. The industry's growth rate will not be sustainable in the future, if increasing capitalization cost trends continue without significant improvement in productivity.

- Reducing "relative or normalized equipment cost" (the rate at which equipment cost increases vis-à-vis requirements for process capability)
- Increasing equipment reliability, availability and utilization, and overall equipment effectiveness
- Reducing variation within and between equipment; attaining chamber matching
- Improving inter-operability by improving compliance to physical and data interface standards
- Extending equipment lifetime to support multiple process generations
- Achieving more effective use of utilities and consumables (including nonproduct wafers) while reducing environmental impact.
- Ability of production equipment mini-environment capability to operate with high yields in Class 100-1000 (ISO Class 3-5) factory environments (refer to the Facilities Technology Requirements Table 56).

MATERIAL HANDLING SYSTEMS

Table 54 Material Handling Systems Technology Requirements

YEAR TECHNOLOGY NODE WAFER DIAMETER	1999 180 nm 200 mm	2002 130 nm 300 mm	2005 100 nm 300 mm	2008 70 nm 300 mm	2011 50 nm 300 mm	2014 35 nm 450 mm
Material handling total capital cost as a % of total capital cost	< 5%	< 3% [1]	< 2% [2]	< 2%	< 2%	< 3%
Transport system types within a factory	Interbay and intrabay	Interbay and intrabay	Some inter/intrabay and some direct (one integrated system)	One integrated system	One integrated system	One integrated system
MTTR (minutes) (SEMI E10)	30	20	15	15	12	10
Failures per 24 hour day over total system (SEMI E10)	<1	<1	<0.5	<0.5	<0.5	<0.5
System throughput						
Interbay transport (moves/hour)	1000	1200	1500	2000	2200	2500
Intrabay transport (moves/hour)	150	170	200	n/a	n/a	n/a
Stocker (moves/hour)	200	240	300	360	360	360
Stocker cycle time (seconds)	18	15	12	10	10	10
Factory wide carrier delivery time (in minutes)	Average=10 Maximum=20	Average=10 Maximum=20	Average=8 Maximum=15	Average=5 Maximum=15	Average=5 Maximum=15	Average=5 Maximum=10

Solutions Exist   *Solutions Being Pursued*   *No Known Solution*

Notes for Table 54 for Material Handling Requirements

[1] Year 2002—High throughput transportation
[2] Year 2005—Direct transportation and fewer stockers

Explanation of Items

Item	*Explanation*
Material handling total capital cost as a % of total capital cost	*Ratio of total capital cost of material (wafer and reticle, inter and intrabay) handling hardware divided by the total capital cost for production equipment and the building, expressed a percentage. For example, if the material handling cost is $30M, and the factory (capital equipment and building cost) is $1000M, then this ratio is 30/1000 = 3%.*
Transport system types within a factory	*Transport system types used in a factory for handling wafer carriers. Typically, today these are interbay and intrabay transport systems. In the future, there is a need to have one system that performs both the interbay and the intrabay transport functions. This does not mean one system from one supplier. This system maybe composed of interoperable sub-systems from multiple (best of breed) suppliers.*
MTTR	*Mean Time To Repair, in minutes, for the fully-integrated system. This means the mean unscheduled downtime (defined by SEMI E10) while repairing any system component.*
Failures per 24 hour day (over total system)	*Number of system component failures allowed throughout the system in a 24 hour day (or period). (Refer to SEMI E10 for more details on failure definition.)*
System throughput	*Number of material handling moves per hour by the sub-system. A move is defined as a carrier move from either a stocker storage bin to a production equipment load port or a carrier move from a production equipment to a stocker storage bin or a carrier move from Stocker X storage bin to Stocker Y storage bin or a carrier move from one stocker port/storage bin to the another storage bin/port of the same stocker.*
Stocker cycle time	*Time required, in seconds, for the stocker internal robot to travel to a carrier at a port or storage bin, pickup the carrier, and deliver it to another port or storage bin within the same stocker.*
Factory-wide carrier delivery time	*Time required, in minutes, to transport a carrier from one production equipment to any other production equipment in the factory. The time begins at the request for carrier movement and ends when the carrier arrives at the load port of the receiving equipment. Maximum delivery time is considered the peak performance capability defined as the average plus two standard deviations.*

Ergonomic and safety issues coupled with the need for efficient and rapid material transport will be the major drivers in defining material handling systems for the 300 mm wafer generation and beyond. The sheer weight of a carrier containing twenty-five 300 mm wafers (8 kilograms) will require that material handling systems be fully automated. Further, these systems should have acceptable Return on Investment (ROI) and must interface directly with all inline production equipment. Given the importance of operator safety, operator interface with the material handling system will be a key focus area.

Table 54 is based on the premise that as demands on the material handling system increase, interbay and intrabay systems need to be combined into an integrated unit, known as a direct or tool-to-tool transport system. Failures must be reduced by one half, while the time to repair each failure is similarly reduced. Throughput must be increased substantially and achieved with reduced delivery time. Furthermore, the material handling system needs to be designed so that it can accommodate the extendibility, flexibility, and scalability demands on the factory. The material handling system will also need to provide for manual backup movement capability (such as personal guided vehicles) and rapid error recovery.

FACTORY SYSTEMS

Table 55 Factory Systems Technology Requirements [1]

YEAR *TECHNOLOGY NODE* *WAFER DIAMETER*	*1999* *180 nm* *200 mm*	*2002* *130 nm* *300 mm*	*2005* *100 nm* *300 mm*	*2008* *70 nm* *300 mm*	*2011* *50 nm* *300 mm*	*2014* *15 nm* *450 mm*
Factory systems cost including integration (% of capital)	< 3%	< 3%	< 2%	< 2%	< 2%	< 3%
MTBF for mission critical applications (months)	> 6	> 6	> 9	> 9	> 12	> 24
Mean Time to Recover for mission critical applications (minutes)	90	45	30	15	5	0
Factory system reuse	> 80%	> 80% of previous node	> 80% of previous node	> 80% of previous node	> 80% of previous node	> 80% of previous node
% of equipment to factory systems interface standards defined [2]	75% 300 mm	100% 300 mm	100% 300 mm	100% 300 mm	80% 450 mm	100% 450 mm
% conformance: equipment to factory systems interface standards [2]	100% 200 mm	100% 300 mm	100% 300 mm	100% 300 mm	100% 300 mm	100% 450 mm
% of factory systems to factory systems interface standards defined [2]	15% 300 mm	100% 300 mm	100% 300 mm	100% 300 mm	80% 450 mm	100% 450 mm
% Conformance: factory systems to factory systems interface standards [2]	0%	75% 300 mm	100% 300 mm	100% 300 mm	100% 300 mm	100% 450 mm
Time to install/upgrade a mission critical application in a working factory (minutes)	< 60	< 30	< 15	0	0	0
Time to install/upgrade a mission critical database in a working factory (hours)	< 24	< 24	2	2	< 1	< 1
Number of process recipes per carrier	Single	Multiple	Multiple	Multiple	Multiple	Multiple

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Notes for Table 55 for Factory Systems Requirements

[1] Supply chain management standardization and conformance needs to be addressed in future editions of this roadmap.

[2] Standardization for 450 mm must occur five years prior to high volume production (one year for Global Joint Guidelines (GJG), two years for standards, and two years for development and validation). [43] [44]

Explanation of Items

Item	*Explanation*
Factory systems cost including integration	*Percentage of overall factory cost spent on factory systems. Initial investment for factory only. Does not include software maintenance and yearly operating costs. Includes computer hardware, software application development, software license, network, and integration.*
MTBF for mission critical applications	*Mean Time Between Failure (MTBF) for mission critical application (unscheduled) downtime. Mission critical applications within the factory systems are those that are required to keep the entire wafer factory operational (documented in the supplemental material). MTBF is measured in months and on a per installation basis.*
Mean time to recover for mission critical applications	*Mean time to recover a mission critical application following an unscheduled downtime. Mission critical applications within the factory system are those that are required to keep the entire wafer factory operational. Mean time to recover is measured in minutes per incident.*
Factory system reuse	*Percentage of factory systems (both computer hardware and software) that is reused from process technology node to process technology node measured in cost.*

[43] International 300 mm Initiative and Japan 300 mm Semiconductor Technology Conference (J300). "Global Joint Guidance for 300 mm Semiconductor Factories, version 1." July 1997.

[44] SEMATECH. *CIM Global Joint Guidance for 300 mm Semiconductor Factories: Release Four.* 98063534C-ENG. Austin, TX:SEMATECH, declassed, July 30, 1999.

% of equipment to factory systems interface standards defined	*Percentage of equipment embedded controller to factory systems interfaces that have defined industry standards for each technology node as required by the Roadmap.*
% conformance: equipment to factory systems interface standards	*Percentage of equipment that comply with industry standard interfaces to factory systems for each technology node as required by the Roadmap.*
% of factory systems to factory systems interface standards defined	*Percentage of factory systems to factory systems interfaces that have defined industry standards for each technology node as required by the Roadmap.*
% conformance: factory systems to factory systems interface standards	*Percentage of factory systems that comply with industry standard interfaces to factory systems for each technology node as required by the Roadmap.*
Time to install/upgrade a mission critical application in a working factory (minutes)	*Down time, in minutes, to install or upgrade a mission critical application while the factory is in production. This includes the time to upgrade hardware, software, and database portions of an overall factory application. Note that database upgrades assume no change to the database schema nor updates to the database contents itself. These scenarios are covered in the metric below, "Time to install/upgrade a mission critical database in a working factory (hours)."* *Frequency of required upgrades should be <1 per year. More frequent upgrades at user request.*
Time to install/upgrade a mission critical database in a working factory (hours)	*Down time, in hours, to install or upgrade a mission critical database while the factory is in production. This includes the time to upgrade and reconfigure the database portions of an overall factory application.* *Frequency of required upgrades should be <1 per year. More frequent upgrades at user request.*
Number of process recipes per carrier	*Indicates a requirement on factory systems to incorporate the ability to automatically change recipe and process parameters between any two wafers in a carrier on production equipment and to do so in a continuous manner without interruption or manual intervention. Also includes the ability to track and control multiple lots per carrier.*

Factory systems development is responding to several key business drivers. With the advent of 300 mm wafer manufacturing, factory systems must integrate substantially greater amounts of automated data collection and processing in order to improve factory productivity. This shift in manufacturing methodology will require better integration of equipment control with automated schedulers, dispatchers and material handling systems. Factory systems will need to provide data acquisition and interact with advanced process control systems to prevent process excursions, improve yield, reduce cycle time due to rework, and reduce equipment calibration and maintenance. In addition, high-product-mix factories will require multiple products/lots per carrier supported by wafer-level material tracking and control.

As shown in Table 55, increased reliance on factory control systems will place greater emphasis on system reliability. Mean time between failure (MTBF) for mission-critical operations will be increased from six months to two years. Backup systems will be needed that eliminate recovery time when a failure occurs.

System flexibility is required that permits very high levels of reuse of these systems when processes and technologies are upgraded in the factory. Furthermore, time to install or upgrade mission-critical factory systems and databases must have minimum impact on the factory operation.

Achieving these goals will require very stringent conformance to industry interface standards. Specific tool- and/or manufacturer-defined standards will not be acceptable.

FACILITIES

Facilities include the overall physical infrastructure in which semiconductor manufacturing operations are performed. Design of these facilities, while not directly linked to a specific technology node, are affected by equipment design, manufacturing goals, environmental, safety and health (ESH) considerations, building codes and defect-reduction targets. Both initial construction costs and operating costs are important cost factors for facilities. Environmental and operational flexibility considerations significantly impact initial construction costs, while the operating costs are driven more by the consumption of utilities, gases and chemicals.

As described in Table 56, facilities must be increasingly flexible, extendable, and reliable, come on line more quickly, and be more cost effective. Rapidly changing process technologies will drive the need to install and remove production equipment efficiently and with minimum interruption to the factory operation. Adoption of integrated mini-environment capability on production equipment will enable the facility to operate at

reduced cleanliness levels. However, increasingly stringent ESH regulations will require innovative, cost-effective point-of-use solutions and factory-wide abatement and reclaim/recycle technologies.

Table 56 Facilities Technology Requirements

YEAR *TECHNOLOGY NODE* *WAFER DIAMETER*	*1999* *180 nm* *200 mm*	*2002* *130 nm* *300 mm*	*2005* *100 nm* *300 mm*	*2008* *70 nm* *300 mm*	*2011* *50 nm* *300 mm*	*2014* *35 nm* *450 mm*
Factory construction cost per cleanroom area ($\$/m^2$) [1]	**1999 factory costs**	**95% of previous node**	**95% of previous node**	**95% of previous node**	**95% of previous node**	**95% of previous node**
Factory construction time (months)	**12**	**11**	**10**	**10**	**10**	**9.5**
Facilities services reliability (%)	**99 %**	**99.5%**	**99.9%**	**99.9%**	**99.9%**	**99.9%**
Cleanroom cleanliness class [2]	**ISO Class 3–5 (Class 1–100)**	**ISO Class 3–5 (Class 1–100)**	**ISO Class 5–6 (Class 100–1000)**	**ISO Class 5–6 (Class 100–1000)**	**ISO Class 5–6 (Class 100–1000)**	**ISO Class 5–6 (Class 100–1000)**

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Notes for Table 56 for Facilities Requirements

[1] In this table, the 1999 cost entries represents the current required levels for the 1999 180 nm technology node.

[2] It is generally believed that achieving ISO Class 6 (Class 1000) results in significant cost savings in facilities and building systems However, the industry must comprehend the ability of production equipment to operate in this environment.

Performance requirements enabling facilities to prevent defects and maintain process critical fluids and materials purity requirements are discussed in the Defect Reduction Chapter.

Performance requirements affecting facilities involving natural resources conservation are discussed in the ESH chapter and involving gases, chemicals, exhaust, emissions, and utilities usage are discussed in the Process Equipment section of this chapter.

Performance requirements affecting facilities involving production equipment installation are discussed in the Process Equipment sections of this chapter.

Explanation of Items

Item	*Explanation*
Factory construction cost per cleanroom area ($\$/m^2$)	*Factory construction cost includes all site work, design, construction and construction management costs for the construction of a semiconductor factory. This includes construction of the factory building shell, office space, factory cleanroom, support spaces, central utility pad or building, mechanical systems, ultrapure water systems, wastewater treatment systems, bulk gas and chemical systems, life-safety systems, control systems, and electrical systems. This excludes costs for land, production equipment, and gas/chemical distribution systems typically included in production equipment installation.*
Factory construction time (months)	*Factory construction time is defined by the formula as the period in months from first concrete pour to the time the first piece of production equipment is ready for qualification. The term "first concrete pour" is equivalent to the term "groundbreaking" used in Table 52 for Factory Operations Technology Requirements.*
Facilities services reliability (%)	*Facilities services reliability is defined as [(total hours/year of operation)-(total hours/year of utility interruption) (outage or out of specification)] divided by [(total hours/year of operation)]. Facilities Services include all utilities for which the facilities organization is responsible (such as power, water, fuel, house gases and wastewater). Interruptions include both utility outages and out-of-specification conditions. Utility performance specifications are established by process engineering typically using industry standards for the device size geometries being produced.*
Cleanroom class	*Cleanliness class of wafer factory cleanroom as defined by ISO 14644-1 (and Fed Std. 209E).* [45]

[45] Federal Standard 209E (FED-STD-209E). *Airborne Particulate Cleanliness Classes in Cleanrooms and Clean Zones.*

POTENTIAL SOLUTIONS

The principal goals of factory integration are maintaining constant cost per unit area; decreasing time to ramp to high volume production; and increasing flexibility to adapt to new business models. The three difficult challenges—complexity management, factory optimization, and extendibility, flexibility and scalability—must be addressed to achieve these goals. Potential solutions are identified for Factory Operations, Production Equipment, Material Handling Systems, Factory Systems, and Facilities in Figures 38–42. Note that the bars containing wafer diameter represent potential solutions that are wafer-size specific.

The relationship between each potential solution and each affected technology requirement is given in the supplemental material.

FACTORY OPERATIONS

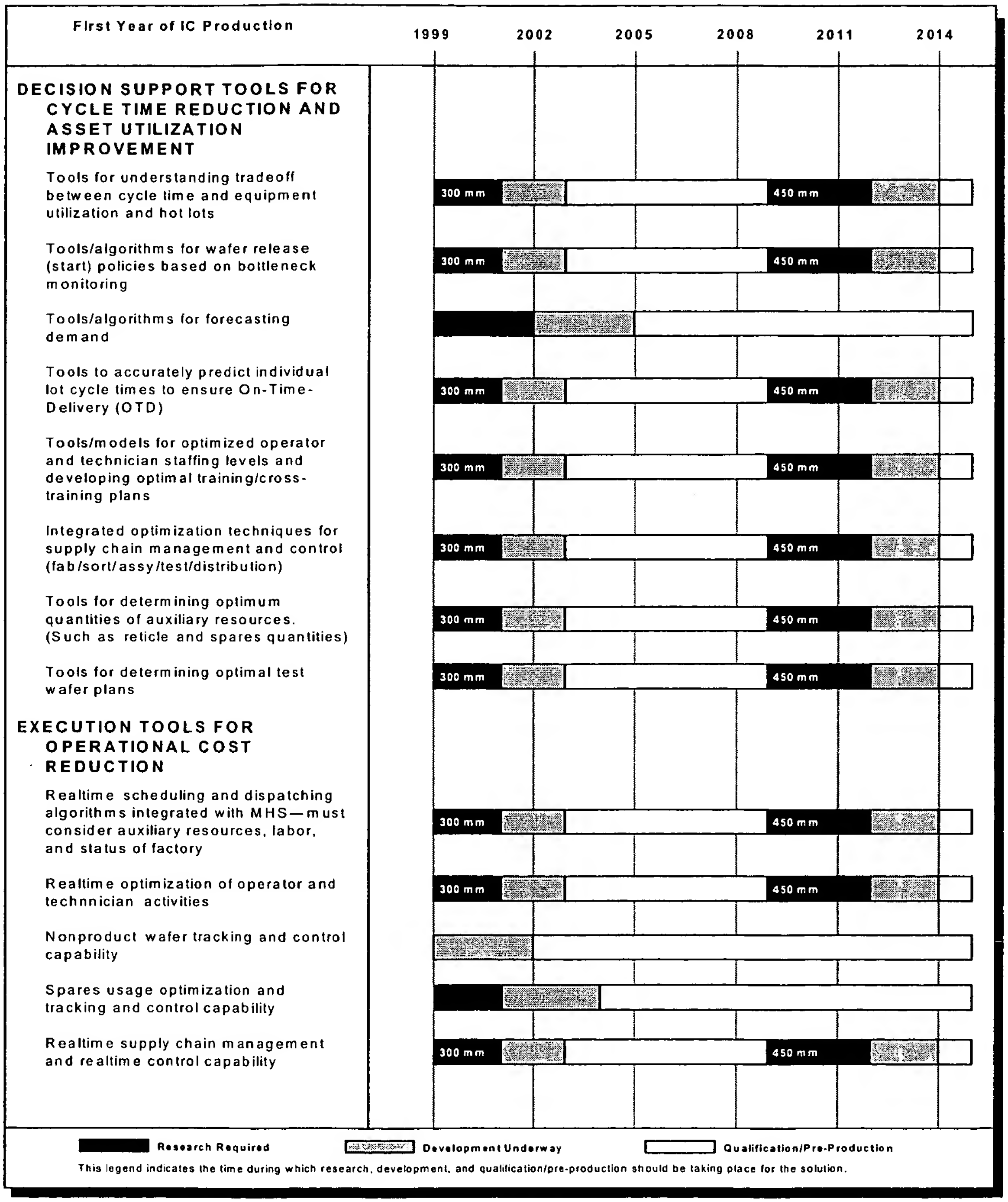


Figure 38 Factory Operations Potential Solutions

PRODUCTION EQUIPMENT

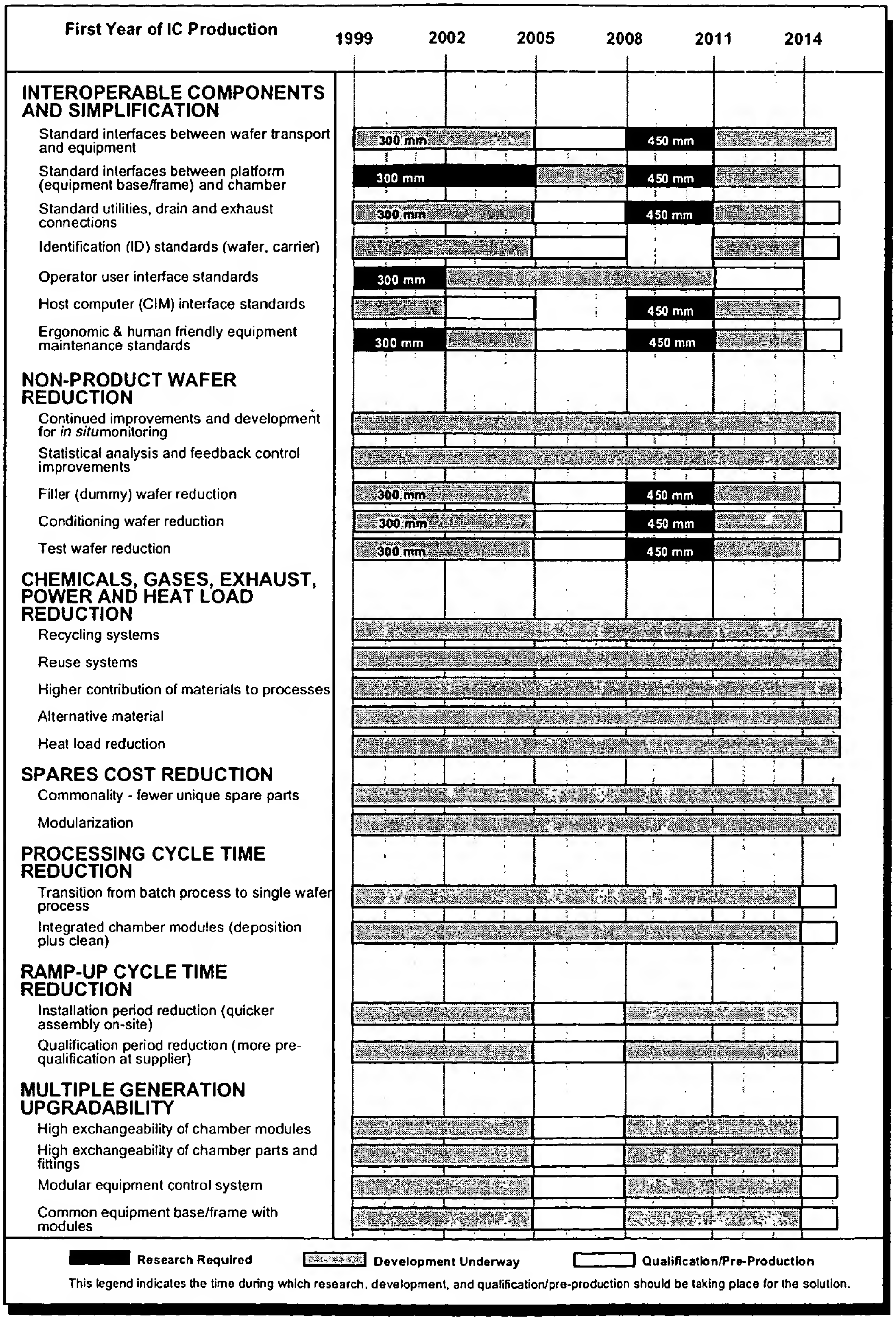


Figure 39 Production Equipment Potential Solutions

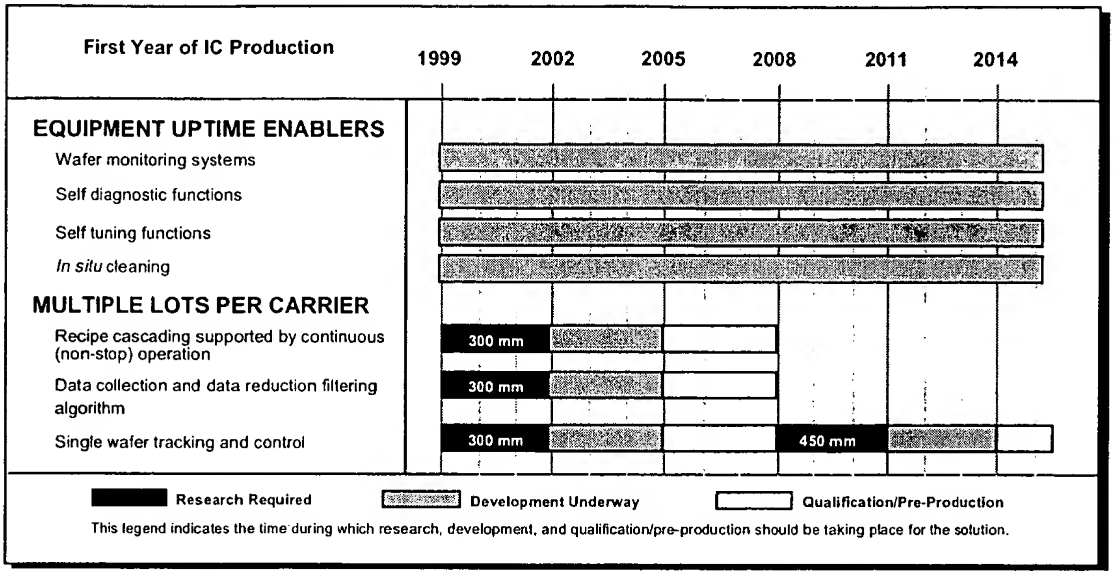


Figure 39 Production Equipment Potential Solutions (continued)

MATERIAL HANDLING SYSTEMS

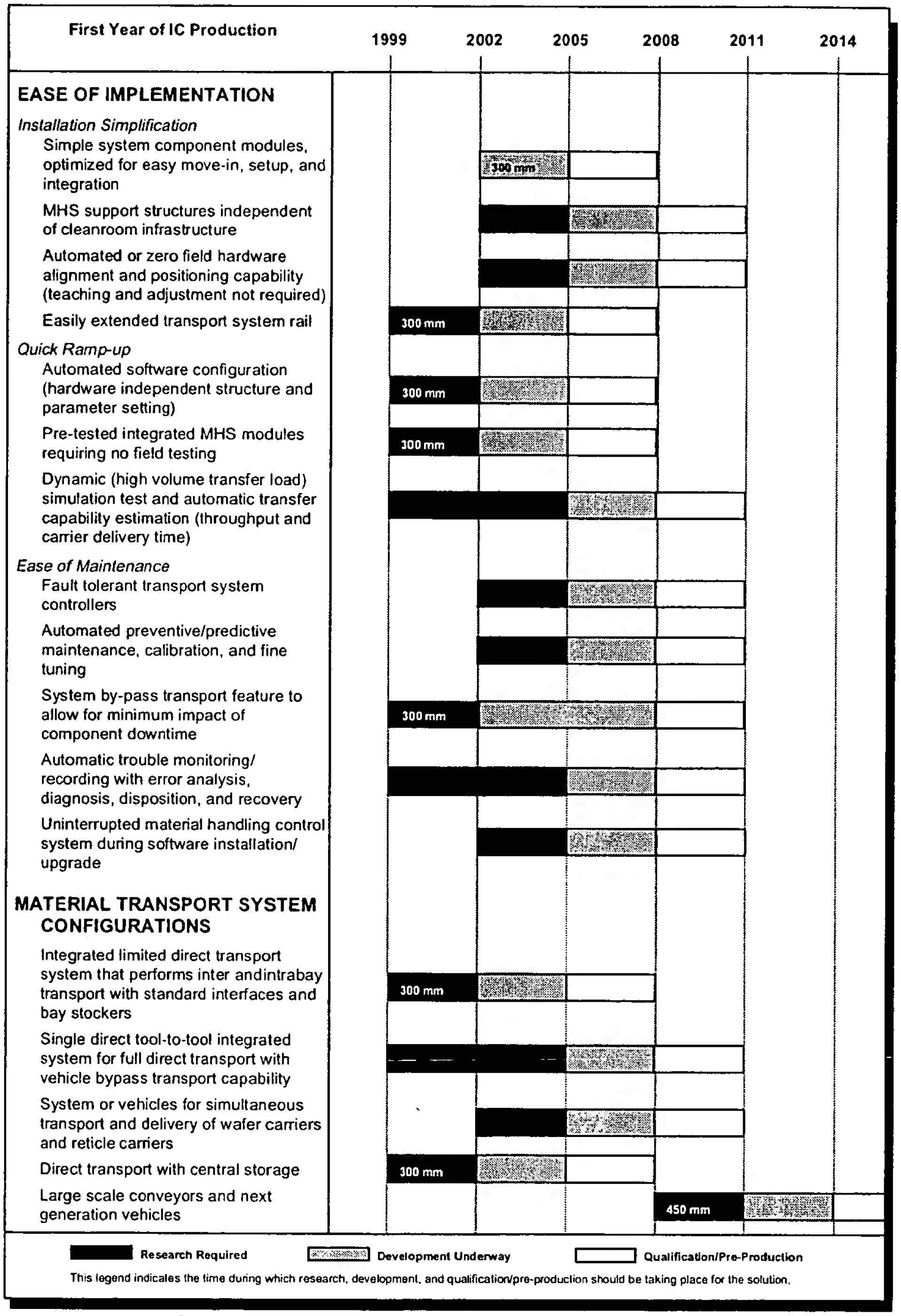


Figure 40 Material Handling Systems Potential Solutions

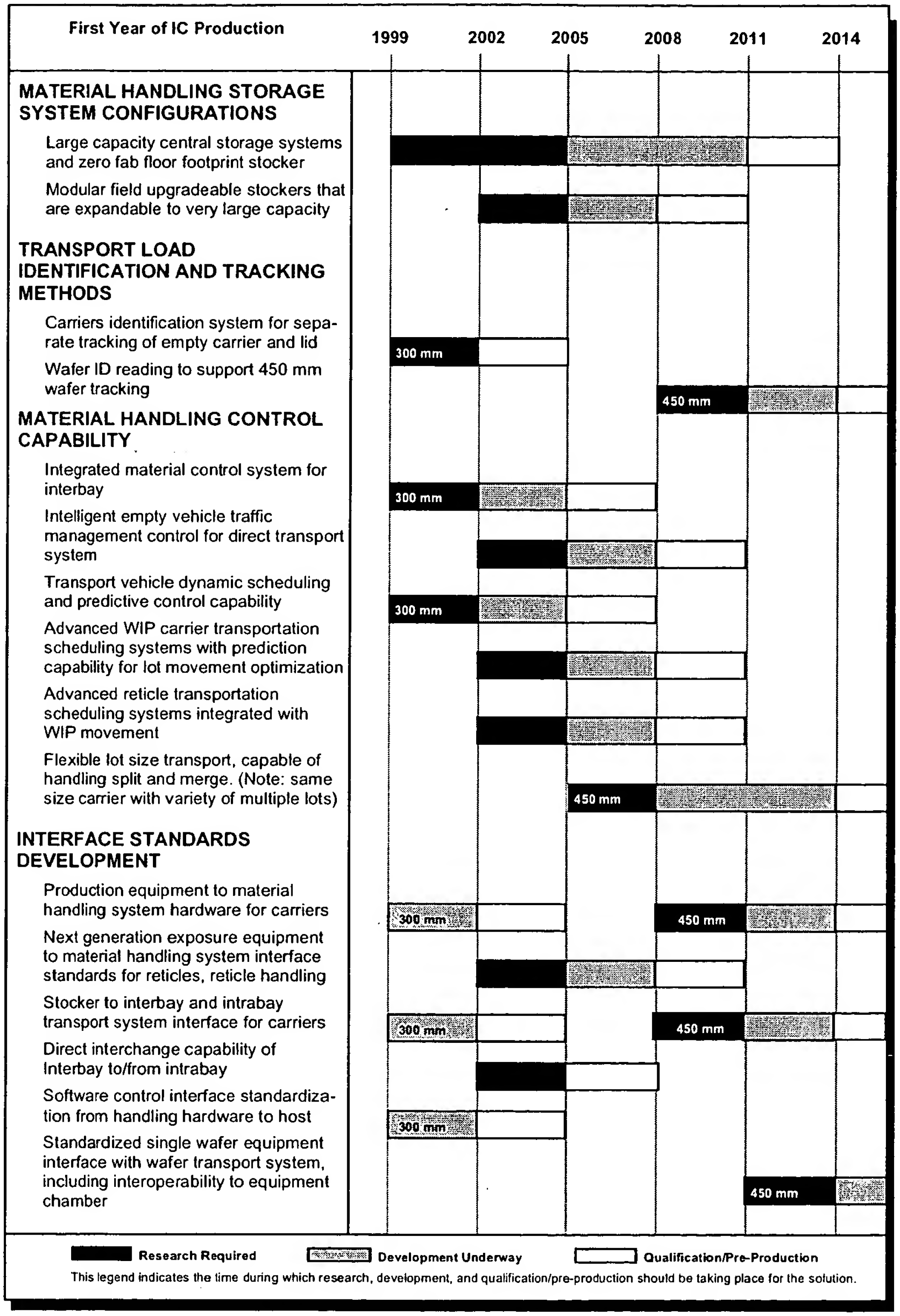


Figure 40 Material Handling Systems Potential Solutions (continued)

FACTORY SYSTEMS

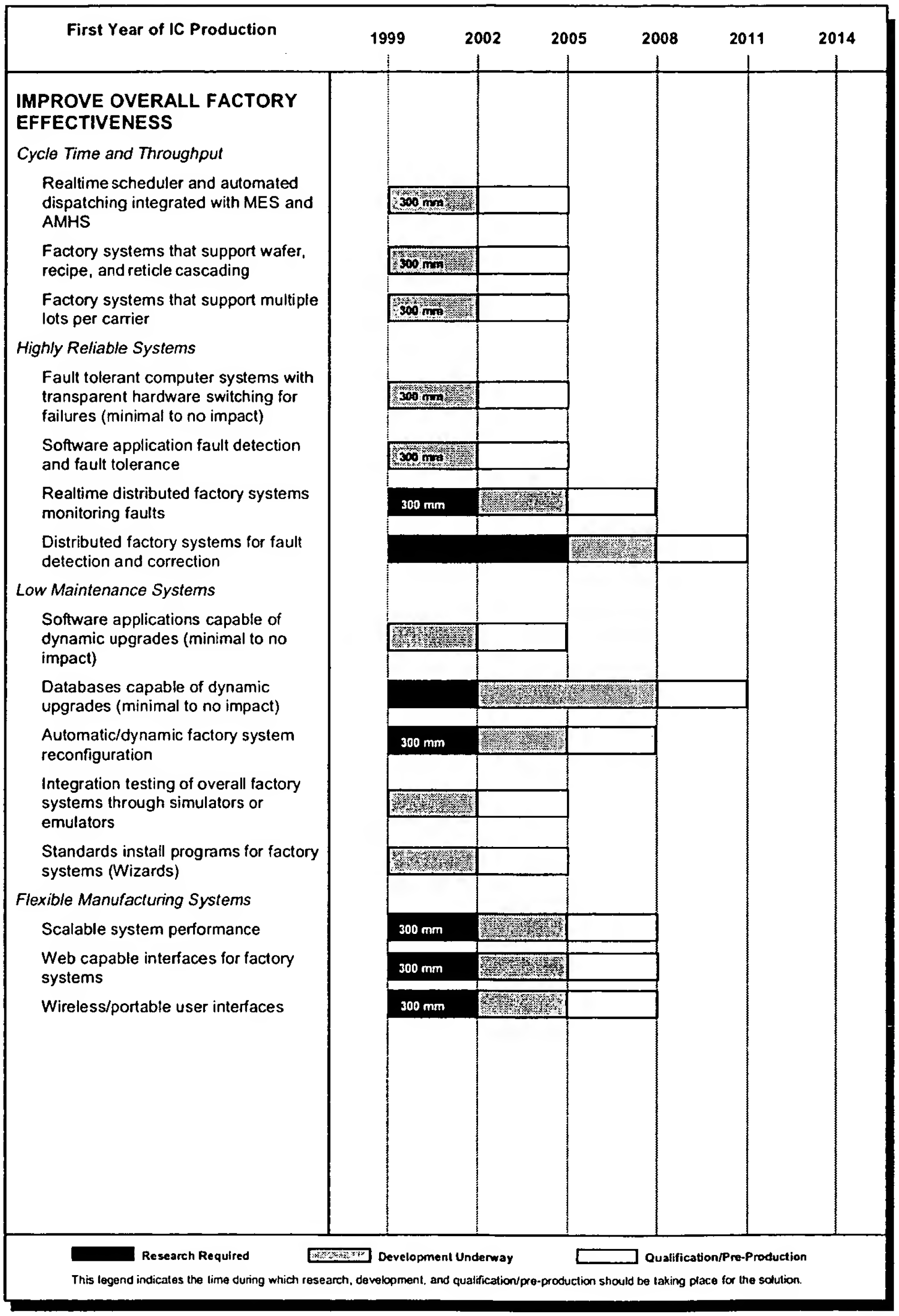


Figure 41 Factory Systems Potential Solutions

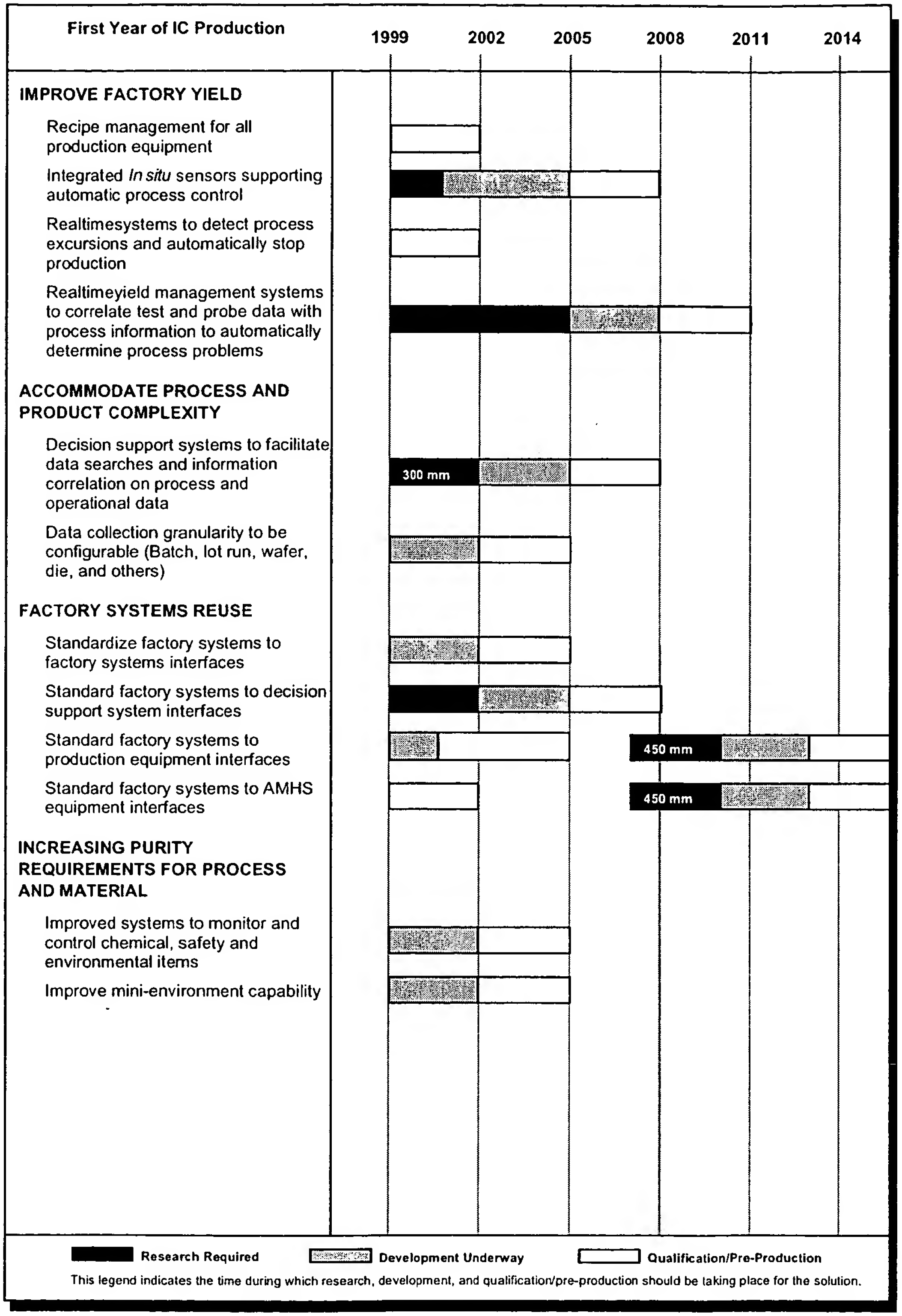


Figure 41 Factory Systems Potential Solutions (continued)

FACILITIES

First Year of IC Production	1999	2002	2005	2008	2011	2014
FACILITIES CAPITAL COST REDUCTION AND OPERATIONS COST CONTAINMENT						
Use benchmarking activities to develop standard performance metrics and best practices for facilities construction, operation, reliability and equipment installation	200 mm	300 mm				450 mm
Develop standard facilities design specifications that reduce unique customer factory designs	300 mm				450 mm	
Develop strategies for extending factory lifetime including layout flexibility, incremental addition of facilities service capacity and reuse of older facilities	300 mm				450 mm	
Develop and implement global standards for building, fire and life-safety codes as well as risk management practices	300 mm				450 mm	
Ensure that production equipment complies with industry guidelines and standards for facilities services and utility consumption	300 mm				450 mm	
HIGHER FACILITIES SERVICES RELIABILITY						
Use benchmarking activities to develop industry reliability metrics and best practices	200 mm	300 mm				450 mm
Use reliability engineering principles and standards in facilities systems design	300 mm				450 mm	
Use total productive maintenance methodologies in the operation and maintenance of facilities systems	300 mm					
Implement voltage sag (dip) immunity standards for production equipment, facilities services, and utilities	300 mm					
Improve control system reliability through use of more robust system design, hardware, and software	300 mm					
MORE EFFICIENT PRODUCTION EQUIPMENT INSTALLATION						
Use benchmarking activities to develop standard production equipment installation metrics and best practices	200 mm	300 mm				450 mm
Use flexible factory layouts that allow for easier installation, removal, and reconfiguration of production equipment over the life of a factory	300 mm				450 mm	
Drive use of SEMI standards for production equipment installation	300 mm					
Improve existing standards and develop new equipment specification standards to reduce complexity and customization of production equipment installation		300 mm			450 mm	
FACILITIES SOLUTIONS FOR ESH REQUIREMENTS						
See potential solutions table in ESH chapter for other solutions involving facilities design and operation						

Research Required — Development Underway — Qualification/Pre-Production

This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

Figure 42 Facilities Potential Solutions

CROSSCUT ISSUES

ENVIRONMENTAL, SAFETY AND HEALTH

ESH plays an ever-more important role in semiconductor factory design and operation. Decisions made at the earliest stages of factory planning will have a dramatic impact on the ability of that factory to meet rigorous safety and environmental requirements economically. Early consideration of safe and environmentally responsible design is essential to develop factories that comply with ESH requirements while achieving rapid start-up schedules and avoiding costly redesign and retrofits.

A plan for continuous improvement of safety in future factories must be established. A thorough understanding of safety risks associated with automated equipment will lead to standards that assure safe working conditions for both people and product. These standards must be directed at the integrity of automated systems, the tools with which they interface, and the interfaces as well.

Our industry faces increasing environmental limitations. The availability of adequate water supplies already places restrictions on the size and location of factories. The goal is to build factories that minimize resource consumption and maximize resource reclamation. Effluents of environmentally toxic materials need to be reduced to near zero—perhaps to zero levels.

While much of the responsibility for these programs rests with the equipment suppliers, application of advanced resource management programs will have a significant impact. ESH standardization and design programs can be greatly enhanced through training programs established for and by the industry. Consideration of ESH standards in equipment design, maintenance, decommissioning and final disposition will reap substantial rewards in ESH performance as well as cost.

DEFECT REDUCTION

Development of good defect reduction strategies reduces costs and investment risks. A factory defect reduction yield model defines typical operational performance and permits a Pareto of performance and yield detractors. A factory model based on experimental mapping of process parameters and process control strategies reduces the need for increased metrology tools and monitor wafers. It is also critical to determine the variational tolerances of process parameters and interactions between processes to reduce reliance on end-of-line inspections.

Factory models should also be capable of handling defect reduction inputs to assure efficient factory designs for rapid construction, rapid yield ramp, high equipment utilization, and extendibility to future technology nodes. Table 57 outlines defect reduction needs.

Table 57 Defect Reduction Potential Solutions

KEY ISSUES	POTENTIAL SOLUTIONS
Variational Tolerances of Critical Process Parameters	
Process control enablers and extendability	Experimental mapping of the parameter space for each process and correlation to device performance
Root cause analysis of performance detractors	
Process Interactions	
Wafer state analysis	Short loop modeling and experimental mapping of parameter state variations
Initial equipment state consistency	Component wear and lifetime studies
Impact of contamination on OEE	
Process Critical Fluids and Materials Purity Requirements	
Point of Use contamination monitoring	Industry test structure for each node on roadmap
Materials reliability and consistency	Process parameter studies
Reduce End Of Line Inspection And Monitor Wafers	
Nonvisual defect detection	*In situ* process control
Metrology for <.08 µm defects	
Rapid Yield Ramp	
Process specific yield models	Inline inspection metrology
Process control	Correlation of parameter space variation and defects
Facilities Impact to Yield	
Electromagnetic interference	Short loop models
Vibration	Data/metrics standards
Molecular contamination	

MODELING AND SIMULATION

Models today make a major contribution to factory operations. Planning and scheduling models, equipment, process, device and circuit simulators, facility layout models, all contribute to increased factory productivity. Achieving solutions to the Factory Integration difficult challenges will require not only that these models be continually improved, but, perhaps more importantly, that they be integrated both operationally and functionally.

Facility planning and scheduling models should be integrated. Advanced Process Control (APC) should be coupled with equipment and process models to improve both throughput and yield. *In situ* equipment and process monitors will then eliminate the need for look-ahead and non-product wafers and greatly reduce non-productive equipment qualification time.

Integration of equipment and process models with device and circuit simulators will facilitate communication between the factory and product designers, resulting in designs more compatible with process capabilities. In order for them to work together effectively, much faster models will be needed. The benefit of integration of these models into a comprehensive planning suite will enable a new factory, or a new technology, to come on-line with minimal delay.

Models of this sophistication will place increased reliance on sensors, particularly *in situ* equipment and process monitors. Sensor reliability will be correspondingly more important, but improved reliability alone will not be sufficient. Models will be used to understand the relationships between measured parameters, identify defective signals, and calculate most-likely values for monitoring and control. This will reduce their dependence on sensor reliability.

An effective suite of models should integrate data based, empirical models with physics-based, first-principle models and statistical models. Compact and behavioral models are required to speed processing without losing predictive accuracy. Development of such modeling techniques as genetic algorithms, neural

networks, fractal geometry, chaos theory, kernel estimators and wavelet analysis provide a greatly enhanced capability in complex system modeling.

Database mining techniques should be applied. Huge volumes of data generated in the factories will preclude manual intervention in much of the preliminary analyses. Computer models will analyze and filter much of this data by continually monitoring the factory's condition. The goal is to identify improvement opportunities to guide manufacturing to the most productive use of resources.

New modeling languages should increase the productivity of factory modelers. Models should be assembled, Lego-style, from template libraries to achieve significant improvements in development and validation times. User interfaces configurable to a wide variety of factory users and modelers are required so as to increase user acceptance of this enabling capability.

METROLOGY INTEGRATION

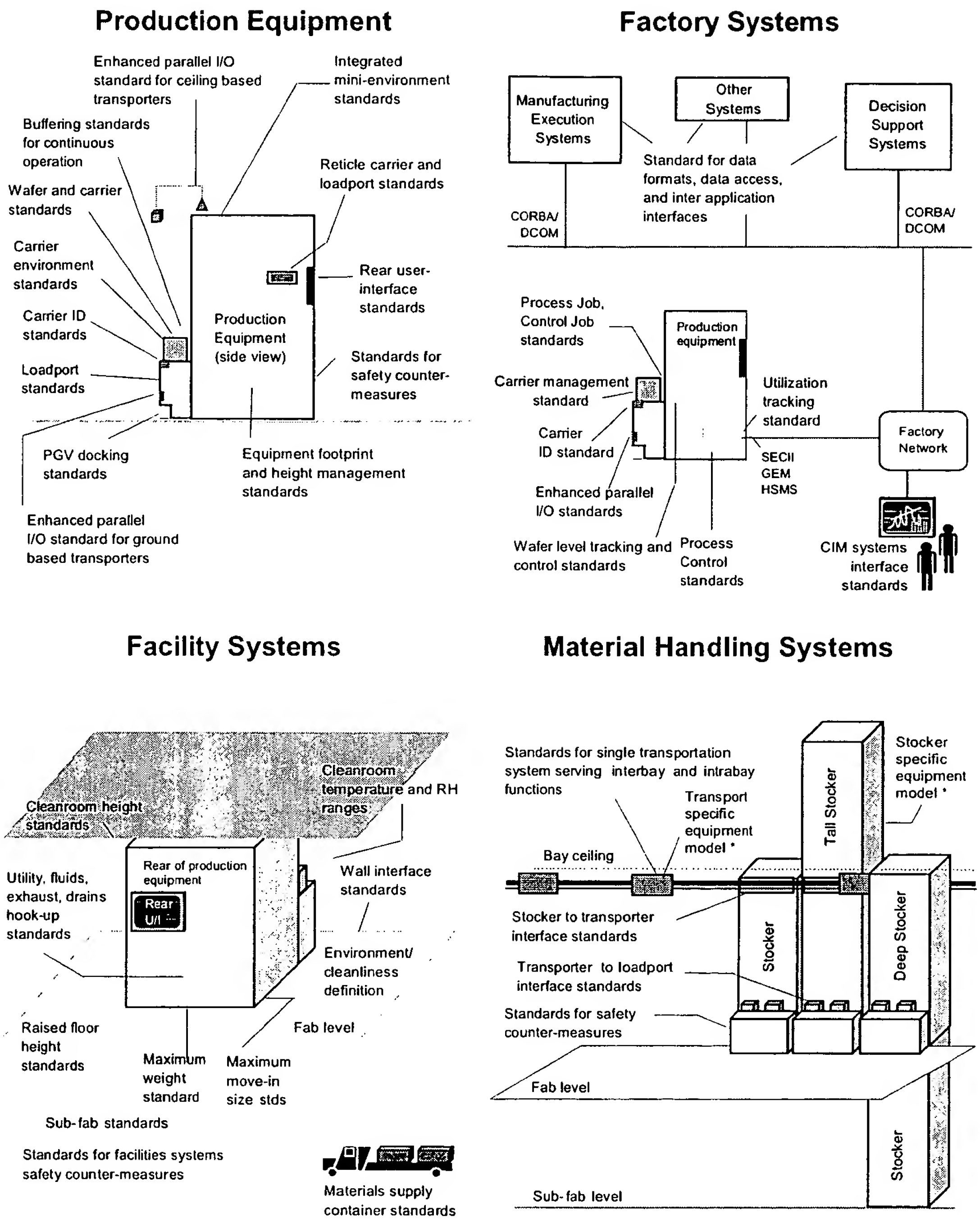
As wafer size increases and required measurement resolution shrinks, both data volumes and data rates will increase dramatically. To use this huge volume of data effectively, metrology systems must be fully integrated into the factory and enterprise level communication and control systems so that data may be associated with other data as well as with wafer tracking information. This data-to-information capability should exist as early as possible in a factory's history to minimize the time spent qualifying equipment and ramping the factory to production. The scope of measurement data sources will extend from key suppliers, (masks and silicon wafers) through assembly and final test, and it should encompass other factories in the enterprise. In addition to measurement data, *per se*, analysis results built on this data, such as defect sources or spatial signatures, will be maintained with the same level of information integrity and connectivity. In 300 mm factories, review and classification tools may eventually appear in clusters or integrated clusters to create a more efficient factory interface. Some 300 mm process equipment will include integrated measurement capability. A manifestation of this increasing metrology integration will be improved capability for APC.

FACTORY INTERFACE STANDARDS REQUIREMENTS

During the planning phase for 300 mm conversion, there has been significant cooperation among IC manufacturers and equipment suppliers in the area of non-proprietary factory integration standards. This is one way to minimize equipment development time, reduce the enormous cost/risk of process development, and better manage complexity. Past experience indicates standards work best when applied to pre-competitive areas, and when there is a benefit to all participants.

Figure 43 shows current efforts for 300 mm standardization and where continued efforts are needed in the future. The concept covers the four basic elements of the factory which have maximum benefits from global cooperation—production equipment, facility systems, material handling systems, and factory systems. Successful development, implementation, and testing of these non-proprietary standards have major ramifications on the ability of the factory to come online and ramp to full volume in a rapid and cost-effective manner.

Standardization of inter-operating elements, especially interfaces between different systems in a factory, will contribute significantly to managing increasing levels of complexity in the factory. Progress to date in interface standardization is reflected in this roadmap.



** Specific equipment model that defines equipment behaviorial characteristics*

PGV—personnel guided vehicle	*CORBA—common object request broker architecture*
DCOM—distributed components object model	*SECII—semiconductor equipment communication standard*
GEM—generic equipment model	*HSMS—high speed messaging standard*
RH—relative humidity	*U/I—user interface*

Figure 43 Areas Where Nonproprietary Interface Standards Reduce Factory Cost and Risk

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

1999 EDITION

ASSEMBLY AND PACKAGING

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ASSEMBLY & PACKAGING

SCOPE

Assembly & Packaging is the bridge between silicon and the electronics system. There is an increased awareness in the industry that assembly and packaging is becoming a differentiator in product development. Package design and fabrication are increasingly important to system applications. It is no longer just a means of protecting the integrated circuit (IC), but also a way for the systems designer to ensure form, fit, and function for today's products—spanning consumer products to high end workstations.

Packaging must perform more than a protective function. It must satisfy the ever-increasing need for performance, high reliability, thermal, and power management at an affordable cost. Packaging design tradeoffs can no longer be made independently of the chip and system; they must be considered concurrently in a system-level approach so as to minimize suboptimization. Packaging capabilities that are as advanced as those used in IC design and fabrication will be necessary to provide the cost-performance advances to satisfy and bridge the silicon to system needs. Increasing demand for chip function is stressing the chip and packaging interconnect requirements. The interface is blurring, and it is becoming more important to consider the chip, package, and printed wiring board together.

The Assembly & Packaging chapter addresses key challenges and proposed activities needed to develop processes, materials, and designs. If successfully implemented, it will contribute to the increased competitiveness of packaged electronic products consistent with the goals of the International Technology Roadmap for Semiconductors (ITRS).

Since the 1997 publication, the scope of the Assembly & Packaging chapter has been expanded to include:

- New sections
  - System-on-a-chip (SoC) packaging
  - Wafer level packaging
  - Flip chip electromigration
- Updated sections
  - Mixed-signal and radio frequency (RF)
  - Multi-chip packaging (MCP)
  - Single chip packages (SCP)
  - Flip chip interconnect (direct chip attach [DCA])
  - Bonding/chip/package/wiring board design
  - Chip carrier substrates
  - Thermal/power/ground management
  - Electrical performance characterizations

Burn-in and known good die (KGD) are important testing issues that are critical to few chip and multi-chip packaging, but they are not addressed in this chapter. Crosscut technology requirements are highlighted in this chapter for the following categories: Environment, Safety, & Health, Metrology, and Modeling & Simulation.

Many of the Assembly & Packaging roadmap attributes are driven by the electronics products and board/substrate industries, and many of the challenges have system solutions. As a result, the solutions to

certain packaging challenges are outside of the scope of this roadmap. To ensure that the needs of the semiconductor community are met and to better understand system needs the Assembly & Packaging Technical Working Group (TWG) continues to strive for:

- Membership of the TWG to include representatives from electronic systems and board/substrate industries
- Partnerships with organizations developing roadmaps for systems with the National Electronics Manufacturers Initiative (NEMI) and board/substrate industries with the Institute for Interconnecting and Packaging Electronic Circuits (IPC). The span of these respective roadmaps has been identified.
- Synchronization of the systems, board/substrate, and packaging roadmaps

The following market applications categorize the information in this roadmap and are consistent with NEMIs roadmap product sector definitions:

- Low-cost: <$300 consumer products, microcontrollers, disk drives, displays
- Hand-held: <$1000 battery-powered products; mobile products, hand-held cellular telecommunications, other hand-held products
- Cost-performance: <$3000 notebooks, desktop personal computers, telecommunications
- High-performance: >$3000 high-end workstations, servers, avionics, supercomputers, most demanding requirements
- Harsh: under-the-hood and other hostile environments
- Memory: DRAMs, SRAMs

These application areas encompass the majority of the product stream of the semiconductor industry. The technology addressed in the roadmap provides at least 80% of the revenue in each application area (in other words, the revenue center of gravity) with the exception of high-performance.

DIFFICULT CHALLENGES

The most difficult challenges facing the assembly and packaging industry are presented in Table 58. These challenges are intended to provide a mechanism to allow the research community to focus resources in the areas of greatest need.

Table 58 Assembly & Packaging Difficult Challenges

FIVE DIFFICULT CHALLENGES *≥ 100 nm / THROUGH 2005*	*SUMMARY OF ISSUES*
Improved organic substrates for high I/O area array flip chip	T_g compatible with Pb free solder processing ε_r approaching 2.0 Improved area array escape wireability at low cost Lower CTE* approaching 6.0 ppm/°C Low moisture absorption High density substrate test
Improved underfills for high I/O area array flip chip Reliability limits of flip chip on organic substrates	Improved manufacturability (fast dispense/cure), better interface adhesion, lower moisture absorption, flow for dense bump pitch Reliability up to 170°C for automotive Comprehensive parametric knowledge of packaging components (chip size, underfill, substrate, heat sink, UBM/bump**)
Coordinated design tools and simulators to address chip, package, and substrate complexity	Physical design Thermal/thermo-mechanical Electrical (power disturbs, EMI†, signal integrity associated w/higher frequency/current, lower voltage, mixed-signal co-design) Commercial EDA‡ supplier support
System reliability impact of Cu/low κ on packaging	Bump and underfill technology to assure low κ dielectric integrity Mechanical strength of dielectrics Interfacial adhesion
Cost effective cooling for cost-performance and high-performance sectors	Meeting 40°C above ambient temperature Localized on-chip power density
DIFFICULT CHALLENGES < 100 nm / BEYOND 2005	
Close the gap between the substrate technology and the chip	Low-loss, low ε_r materials Cost/unit area constant (cost/layer decreasing) Interconnect density scaled to silicon System level solution that optimizes reliability and cost
"System level" view of integrated chip, package, and substrate needs	Commercial EDA supplier support
Ultra high frequency design for high density digital and mixed-signal packaging	Efficient design and simulation tools Integrated analog to digital design tools
Manufacturability and reliability of large body packages	Substrate flatness Co-planarity of chip-to-package and package-to-board

* *CTE—coefficient of thermal expansion*
** *UBM—under bump metallurgy*
† *EMI—electromagnetic interference*
‡ *EDA—electronic design automation*

TECHNOLOGY REQUIREMENTS

Packaging technology continues to change rapidly. Assembly and packaging needs are driven as much by market application requirements as by silicon technology. Cost will drive technology tradeoffs for all market segments. The key single chip package (SCP) technology requirements have been updated by the domestic and international TWGs as shown in Table 59a. Although assembly and packaging costs are expected to decrease over time on a cost per pin basis, the chip and package pincount is increasing more rapidly than cost per pin is decreasing. This explosion in pincount is increasing not only the absolute cost of assembly and packaging on a per-chip basis, but also the substrate and system-level costs, unless the chip count for the system is reduced. To satisfy the requirements for the increasing numbers of pins needed to leverage silicon productivity more fully, the industry must implement affordable new assembly and packaging technologies more independent of pincount.

PACKAGE DESIGN REQUIREMENTS

Package design complexity (chip-to-module and chip/module-to-board) and scope are continuously increasing while the market intensifies the demand for design cycle time reduction and high design confidence. Physical, electrical, thermal, mechanical, assembly, and manufacturability considerations, in addition to cost and availability, confront the package designer. The package design process requires continuous improvements in design and analysis tools. The tools for layout, wiring, electrical, mechanical, and thermal design tasks must enhance usability and minimize interface incompatibilities if design cycle reductions are to be realized. The goal is an integrated design system within the next decade. The scope of this integrated design system must include or be coordinated with chip design so that efficient chip/package co-design is feasible. Ideally, it should be linked to the system design so as to incorporate those requirements and tradeoffs.

PACKAGE RELIABILITY REQUIREMENTS

Performance, cost, and the trend toward "light, thin, short, and small" product design will increase the complexity of package technology, resulting in the use of new materials and packaging formats. These changes will introduce new reliability risks. Market cycle time compression and market segmentation will drive changes and time compression in package reliability qualification procedures and requirements. Successful introduction of these new package technologies requires the understanding of the fundamental physical and chemical properties of these materials; their ability to form reliable interfaces with other package materials; and resultant failure mechanisms and activation energies.

Table 59a Assembly & Packaging Technology Requirements—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
Cost (Cents/Pin) [A]							
Low cost	0.40–0.90	0.38–0.86	0.36–0.81	0.34–0.77	0.33–0.73	0.31–0.70	0.29–0.66
Hand-held	0.50–1.30	0.48–1.24	0.45–1.17	0.43–1.11	0.41–1.06	0.39–1.01	0.37–0.96
Cost-performance	0.90–1.90	0.86–1.81	0.81–1.71	0.77–1.63	0.73–1.55	0.70–1.47	0.66–1.40
High-performance	3.10	2.95	2.80	2.66	2.52	2.40	2.28
Harsh	0.50–1.00	0.48–0.95	0.45–0.90	0.43–0.86	0.41–0.81	0.39–0.77	0.37–0.74
Memory	0.40–1.90	0.38–1.71	0.36–1.54	0.34–1.39	0.33–1.25	0.31–1.12	0.29–1.01
Chip Size (mm^2)							
Low cost	53	55	57	59	61	63	65
Hand-held	53	55	57	59	61	63	65
Cost-performance	170	170	170	191	214	225	235
High-performance	450	450	450	509	567	595	622
Harsh	53	55	57	59	61	63	65
Memory	132	139	145	152	159	167	174
Power: Single-Chip Package (Watts) [B]							
Low cost	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Hand-held	1.4	1.6	1.8	2.0	2.2	2.3	2.4
Cost-performance	48	54	61	75	81	88	96
High-performance	90	100	115	130	140	150	160
Harsh	14	14	14	14	14	14	14
Memory	0.8	1.0	1.2	1.4	1.6	1.8	2
Core Voltage (Volts)							
Low cost	1.8	1.8	1.8	1.5	1.5	1.2	1.2
Hand-held	1.5–1.8	1.5–1.8	1.2–1.5	1.2–1.5	1.2–1.5	0.9–1.2	0.9–1.2
Cost-performance	1.8	1.8	1.8	1.5	1.5	1.2	1.2
High-performance	1.8	1.8	1.8	1.5	1.5	1.2	1.2
Harsh	5.0	3.3	3.3	2.5	2.5	2.5	2.5
Memory	1.8	1.8	1.8	1.5	1.5	1.2	1.2
Package Pincount [C]							
Low cost	80–290	86–313	90–338	101–365	109–395	118–426	127–460
Hand-held	128–368	138–397	149–429	161–464	174–501	188–541	203–584
Cost-performance	370–740	400–821	432–912	466–1012	503–1123	544–1247	587–1384
High-performance [D]	1600	1792	2007	2248	2518	2820	3158
Harsh	40–240	40–259	40–280	40–302	40–327	40–353	40–381
Memory	44–128	44–128	44–128	44–144	44–144	48–160	48–160
Overall Package Profile (mm)							
Low cost	1.7	1.7	1.2	1.2	1.2	1.0	1.0
Hand-held	1.2	1.2	1.0	1.0	1.0	0.8	0.8
Cost-performance	1.2–1.7	1.2–1.7	1.0–1.2	1.0–1.2	1.0–1.2	0.8–1.0	0.8–1.0
High-performance	n/a	n/a	N/a	n/a	n/a	n/a	n/a
Harsh	1.4	1.4	1.0	1.0	1.0	1.0	1.0
Memory	1.2	1.2	1.0	1.0	1.0	0.8	0.8

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 59a Assembly & Packaging Technology Requirements—Near Term (continued)

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
Performance: On-Chip (MHz) [E]							
Low cost	300	350	415	460	510	570	633
Hand-held	300	350	415	460	510	570	633
Cost-performance	600	660	727	800	890	989	1100
High-performance	1200	1321	1454	1600	1724	1857	2000
Harsh	25	40	60	60	60	60	60
Memory (D/SRAM)	133/300	133/330	150/362	150/400	150/445	150/495	150/550
Performance: Chip-to-Board for Peripheral Buses (MHz)							
Low cost	75	75	100	100	100	100	100
Hand-held	75	75	100	100	100	100	100
Cost-performance [F]	133/300	133/330	150/362	150/400	150/445	150/495	150/550
High-performance [G]	600	660	727	800	862	928	1000
Harsh	25	40	60	60	60	60	60
Memory (D/SRAM) [F]	133/300	133/330	150/362	150/400	150/445	150/495	150/550
Junction Temperature Maximum (°C) [H]							
Low cost	125	125	125	125	125	125	125
Hand-held	115	115	115	115	115	115	115
Cost-performance	100	95	90	85	85	85	85
High-performance	100	95	90	85	85	85	85
Harsh	155	155	155	155	155	155	175
Memory	100	100	100	100	100	100	100
Operating Temperature Extreme: Ambient (°C) [H]							
Low cost	55	55	55	55	55	55	55
Hand-held	55	55	55	55	55	55	55
Cost-performance	45	45	45	45	45	45	45
High-performance	45	45	45	45	45	45	45
Harsh	-40 to 150	-40 to 150	-40 to 150	-40 to 150	-40 to 150	-40 to 150	-40 to 170
Memory	55	55	55	55	55	55	55

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 59b Assembly & Packaging Technology Requirements—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
Cost (Cents/Pin) [A]			
Low cost	0.25–0.57	0.22–0.49	0.19–0.42
Hand-held	0.32–0.82	0.27–0.70	0.23–0.60
Cost-performance	0.57–1.20	0.49–1.03	0.42–0.88
High-performance	1.95	1.68	1.44
Harsh	0.32–0.63	0.27–0.54	0.23–0.46
Memory	0.25–0.74	0.22–0.54	0.19–0.39
Chip Size (mm^2)			
Low cost	72	81	90
Hand-held	72	81	90
Cost-performance	270	308	351
High-performance	713	817	937
Harsh	72	81	90
Memory	200	229	262
Power: Single-Chip Package (Watts) [B]			
Low cost	n/a	n/a	n/a
Hand-held	2.5	2.6	2.7
Cost-performance	104	109	115
High-performance	170	174	183
Harsh	14	14	14
Memory	2.5	3.0	3.5
Core Voltage (Volts)			
Low cost	0.9	0.6	0.5–0.6
Hand-held	0.6–0.9	0.5–0.6	0.3–0.6
Cost-performance	0.9	0.6	0.5–0.6
High-performance	0.9	0.6	0.5–0.6
Harsh	2.5	2.5	2.5
Memory	0.9	0.6–0.9	0.5–0.6
Package Pincount [C]			
Low cost	160–580	201–730	254–920
Hand-held	256–736	322–927	406–1167
Cost-performance	740–1893	932–2589	1174–3541
High-performance [D]	4437	6234	8758
Harsh	40–480	40–604	40–761
Memory	48–182	48–200	48–220
Overall Package Profile (mm)			
Low cost	1.0	1.0	1.0
Hand-held	0.65	0.65	0.5
Cost-performance	0.65–0.8	0.65–0.8	0.5–0.65
High-performance	n/a	n/a	n/a
Harsh	1.0	1.0	1.0
Memory	0.65	0.65	0.5

Solutions Exist | *Solutions Being Pursued* | *No Known Solutions*

Table 59b Assembly & Packaging Technology Requirements—Long Term (continued)

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
Performance: On-Chip (MHz) [E]			
Low cost	840	1044	1250
Hand-held	840	1044	1250
Cost-performance	1400	1800	2200
High-performance	2500	3000	3600
Harsh	100	100	100
Memory (D/SRAM)	175/700	200/900	225/1100
Performance: Chip-to-Board for Peripheral Buses (MHz)			
Low cost	125	125	150
Hand-held	125	125	150
Cost-performance [F]	175/700	200/900	225/1100
High-performance [G]	1250	1500	1800
Harsh	100	100	125
Memory (D/SRAM) [F]	175/700	200/900	225/1100
Junction Temperature Maximum (°C) [H]			
Low cost	125	125	125
Hand-held	115	115	115
Cost-performance	85	85	85
High-performance	85	85	85
Harsh	185	185	185
Memory	100	100	100
Operating Temperature Extreme: Ambient (°C) [H]			
Low cost	55	55	55
Hand-held	55	55	55
Cost-performance	45	45	45
High-performance	45	45	45
Harsh	-40 to 180	-40 to 180	-40 to 180
Memory	55	55	55

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Notes for Table 59 for Assembly and Packaging Requirements

[A] All costs do not include silicon, heat sinks, or test; substrate cost should not exceed 30–50% of total cost.

[B] Solutions are being pursued for cost-performance ≥ 65 W and for high-performance ≥ 110 W due to cost-driven thermal management issues. Cost-performance data is for desktop applications; notebook applications are limited to 14 W maximum in 1999 The memory power is for the SRAM chip.

[C] Reflects package/substrate cost issues. RAMBUS and other serialized memories are not addressed.

[D] The high-performance IC may be classified into two categories. The application-specific integrated circuit (ASIC) has a high number of signal I/O pins. The total number of voltage/ground pins is about one half of the number of signal I/O pins. The microprocessor has signal I/O pins much less than that of the ASIC; however, the power consumption of the microprocessor is much higher than that of the ASIC. Even with such a high number of voltage/ground pins, the effective overall inductance is still very high. On-chip de-coupling capacitance is needed. Ideally, one may want to place an on-chip de-coupling capacitance, C(de-coupling) ≈ 9 Power / {f(on-chip) × [Core Voltage]^2}. Such consideration also applies to many of the high power cost-performance applications.

[E] > 450 MHz reflects need for improved impedance control.

[F] xx/yyy refers to system memory and peripheral bus speed (xx) and to processor cache memory data transfer (yyy) for high end of cost-performance category. Memory performance must match the requirements of processor buses and may require new architectures at the device or array level, such as reduced-width multiplexed buses that run at the on-chip frequency.

[G] > 1000 MHz reflects need for improved impedance control.

[H] Uncertain materials solutions. Reflects package/substrate cost issues.

POTENTIAL SOLUTIONS

INTEGRATED DESIGN ENVIRONMENT

Figure 44 shows potential solutions for an integrated design environment. Many of these solutions involve modeling and simulation capabilities that will be embodied in packaging computer aided design (CAD) systems. Design tools are required to manage the complexity of packaging that is being pushed to its performance limits. In the short term a major focus of these tools will involve flip chip/area array substrates. In the long term an integrated design system with expert capabilities is a potential solution. The time required for these features to migrate from concept to commercially viable tools must be shortened significantly. This acceleration of the tool development cycle will require close partnerships between the universities and the electronic design automation (EDA) suppliers. The long range implementation of the integrated design environment includes interface with chip design systems to permit co-design of chip and package.

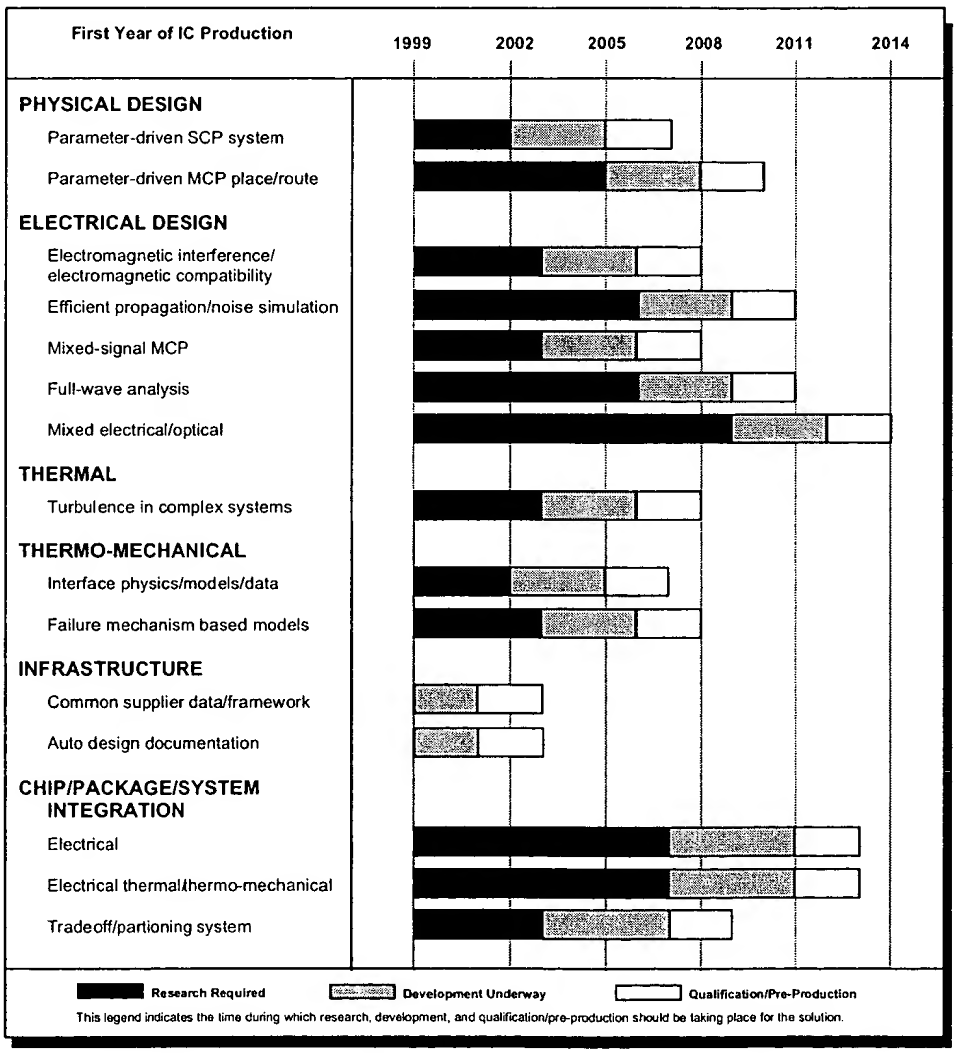


Figure 44 Integrated Design Environment Potential Solutions

THERMAL MANAGEMENT

The task of dissipating the heat from integrated circuits while maintaining acceptable junction temperatures has been a significant challenge for semiconductor and system manufacturers. Power, wattage, and junction temperature requirements are shown by market segment in Table 59. These ITRS projections indicate that the thermal management challenge will significantly increase in the future due to increasing power, decreasing junction temperatures, and a continuing need to have cost-effective solutions.

In the hand-held market segment, power availability is limited by battery power. The power dissipation is currently limited by the user (the heat sink is the hand or lap), and cooling is usually accomplished without forced air. Challenges increase from the desire to use higher power devices; with the increasing convergence of computing with communication (driving higher performance and power in this market); and with an increasing need for system level cooling (more than one hot device). Solutions could include use of higher thermal conductivity materials; reduction in internal thermal resistance; and potentially in more novel approaches to manage cooling while not discomforting the user. Cooling needs to be an integral part of the product design.

Desktop processors for the cost-performance market have required forced air cooling for the system, and have represented a wide spectrum of electronic products. With area array flip chip, the backside of the chip provides a direct heat path for cooling. The packaging challenge has been to create an interface with the chip that provides very low thermal resistance, is cost effective, reliable, and also enables system level solutions. System cooling design must also be acceptable in this market, with implications to cost, acoustic noise, reliability, and high volume manufacturing. As Table 59 shows, power is expected to continue to increase while target junction temperatures decrease. In 2002 this equates to a Delta-T of 45° (and shrinking over time) with the ambient. At an expected power of 75 Watts (and growing over time), this becomes a significant challenge for acceptable solutions in the cost-performance market, and further highlights the need for complete, integrated, chip-to-system solutions. Some of the key developments and innovations are: more advanced/efficient air cooling, boundary layer control, engineered surfaces, and cost-effective alternative cooling systems.

Notebook computing products are also in the cost-performance market segment. While they may not push the highest power levels while on battery operation, they do pose significant cooling requirements based on form factor, weight, and ergonomic issues (maintaining comfortable outer case temperatures for the user). Additional developmental areas here would include redirection of internal thermal resistance, engineered surfaces, new novel cooling systems, and solutions that allow multiple and different power levels for the product.

The high-performance market sector has experienced a dramatic increase in power over the different generations. Air cooling has been the preferred option to keep costs within bounds. In addition to managing total chip power requirements in excess of 100 Watts, solutions to manage power density and internal hot spots are necessary. Assuming identical junction and ambient temperatures, the higher power levels in this sector will demand a 40%–50% reduction in junction to ambient thermal resistance compared with the cost-performance segment. Current solutions are already focused on complete integration from the chip through the system, and this approach will need to continue. Significant engineering development will be needed for power increases at each technology generation, with capabilities needed equivalent to closed-loop cooled systems. Solutions must of course also be acceptable to the end-use customers. A major additional challenge will be to ensure that thermal management does not impede the migration path of products from this sector into the cost-performance market.

WAFER BUMPING

Wafer bumping is a key element to the successful implementation of flip chip technology as required by the ITRS. Eutectic Sn/Pb bumps on organic substrates represent the target against which potential solutions should be benchmarked. There are several challenge areas to implementation and proliferation including: cost, density, manufacturability, availability, and compatibility with on-chip Cu/low κ materials. Potential solutions to reduce soft error upset from alpha particle emissions could include moving to low alpha Pb and

Pb-free solders during the timeframe of this roadmap. Cost for bumping a wafer (on a per chip basis, including the under bump metallurgy and the bump deposition) needs to decrease continuously over the period through process simplification. Any lower cost process must preserve reliability, quality, and yield. Bump pitch will decrease from 200 µm or greater today, to 150 µm by the end of the period for high I/O and high power chips. This will increase the wireability requirements for the substrate significantly. For low I/O chips in low cost and handheld applications, the bump pitch will reduce continuously as to be discussed later, and illustrated in Table 61a. Bumped wafers and chips must become generally available at a cost below packaged devices but at an equal quality level.

Test has the greatest technical challenge to achieve the quality goal. Test contactor reliability must be achieved at elevated temperatures without inducing bump damage. The flip chip must be, and be perceived to be, equivalent to a packaged device. Achieving this perceived equivalence is the greatest short term challenge and needs greater industry focus for success.

ELECTROMIGRATION LIMITS OF 63SN/37PB FLIP CHIP SOLDER BUMPS

The electromigration limits of 63Sn/37Pb solder must be incorporated into flip chip design rules to assure reliable operation. As the bump size is reduced, the allowable current per bump is also reduced. The Mean Time to Failure (MTTF) of the 63Sn/37Pb solder bump is a function of the passivation opening, average bump temperature, and current. Table 60 lists the recommended maximum current per bump in mA to achieve a 100,000 hour MTTF for the size solder bumps required over the period of this roadmap. The Weibull slope has been shown to typically range from 4 to 6. A typical flip chip has many power and ground bumps in parallel and this needs to be accounted for in predicting the reliability of the actual device. For example, at the 100 nm generation in 2005, the cost-performance microprocessor has an average current of 80 A (96 Watts at 1.2 volts). With a bump pitch of 150 µm and a passivation opening of 65 µm, the current limit is 95 mA per bump at 80°C and 45 mA at 100°C chip temperature. The voltage and ground current will require 840 bumps each for a total of 1680 bumps for the supply current if the operating temperature of the chip is 80°C, and 3550 bumps if the operating temperature is 100°C. Note that for a cost-performance chip at 170 mm^2, The maximum number of area array pads is limited to about 7200 bumps. This is marginal in 2005 and definitely not acceptable in the future. For example, at the 50 nm generation in 2011, the cost-performance microprocessor has an average current of 182 A (109 Watts at 0.6 volt), which is 2.3× increase in current. Such an average current would require 3820 bumps (80°C operating temperature) or 8070 bumps (100°C operating temperature) for the voltage and ground connections. Other chip-to-package interconnection solutions, such as the alternative solders, should be investigated.

Table 60 Current Limits of 63Sn/37Pb Flip Chip Solder Bumps

		Current Limits for 100,000 hour MTTF at Average Bump Temperatures of		
Bump Pitch	Passivation Opening	100°C	90°C	80°C
250 µm	85 µm	75 mA	110 mA	165 mA
200 µm	80 µm	66 mA	97 mA	145 mA
150 µm	65 µm	45 mA	65 mA	95 mA

WAFER LEVEL PACKAGING

The wafer level packaging process (WLP) is a new technology in which all of the IC packaging is performed at the wafer level. A WLP technology can, for the first time, maintain the cost of the IC packaging as a constant percentage of the total wafer cost. This is possible because WLP reduces the cost of packaging the individual chips. By definition a WLP technology requires that when the chip size shrinks in later years, all of the package interconnects will continuously be located within the chip outline (it must be a fan-in design). From a systems perspective, the limitation on WLP is how many I/O can be placed under the chip and still have a board design that can be routed. The primary application market for WLP technology is projected to be low to moderate I/O density applications, as typified by high yield DRAM, Flash, and other ICs with ≤

100 total I/O and adequate silicon area. A key enabling technology to take full advantage of a WLP will be the development of wafer level test and burn-in. Most WLPs with I/O pitch equal to or greater than 0.5 mm do not require the use of underfill and can therefore be directly implemented into a customer's standard surface mount technology (SMT) process flow.

CHIP-TO-NEXT LEVEL INTERCONNECT

Table 61 and Figure 45 show the chip-to-next level interconnect potential solutions. The values for wire bond in this table are for inline pad pitches, although a staggered bond pad configuration could achieve an effective pitch denser than the value shown. The flip chip connection requires fan-out wiring on the package. Signal leads are usually placed on the outer several rows together with many of the voltage and ground leads for easy fan-out and minimum package inductance. The inner regions of the area array may be used for voltage and ground connection to minimize the on-chip resistive voltage drop across the IC chip. The area array pad pitch is 200 µm now, and reduces to 150 µm for the 100 nm technology generation and beyond for cost-performance and high-performance market segments, where the signal I/O and chip power are very high. The infrequent change of the pad pitch is adopted to minimize the cost of the test probe head. This results in many long fan-out wires. Excessive crosstalk noise between parallel signal wires should be carefully assessed at the design stage. For some of the hand-held applications where the size and power of the chip are small, one may need area array pad pitch much smaller than that used for the cost-performance and high-performance market segments. This is shown in a separate row in Table 61. For the applications with low supply current, the anisotropic conductive adhesives may be used for the area array connections.

Table 61a Chip-to-Next Level Interconnect Potential Solutions—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
Chip Interconnect Pitch (µm)							
Wire bond—ball	**50**	**49**	**47**	**45**	**42**	**41**	**40**
Wire bond—wedge	**45**	**44**	**42**	**40**	**37**	**36**	**35**
TAB*	**50**	**50**	**40**	**40**	**40**	**40**	**30**
Flip chip (area array) for cost-performance and high-performance	**200**	**200**	**200**	**200**	**200**	**200**	**150**
Flip chip for handheld, low cost, and harsh	**180**	**165**	**150**	**130**	**120**	**110**	**100**

Table 61b Chip-to-Next Level Interconnect Potential Solutions—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
Chip Interconnect Pitch (µm)			
Wire bond—ball	**40**	**40**	**40**
Wire bond—wedge	**35**	**35**	**35**
TAB*	**30**	**30**	**30**
Flip chip (area array) for cost-performance and high-performance	**150**	**150**	**150**
Flip chip for handheld, low cost, and harsh	**70**	**50**	**35**

TAB—tape automated bonding

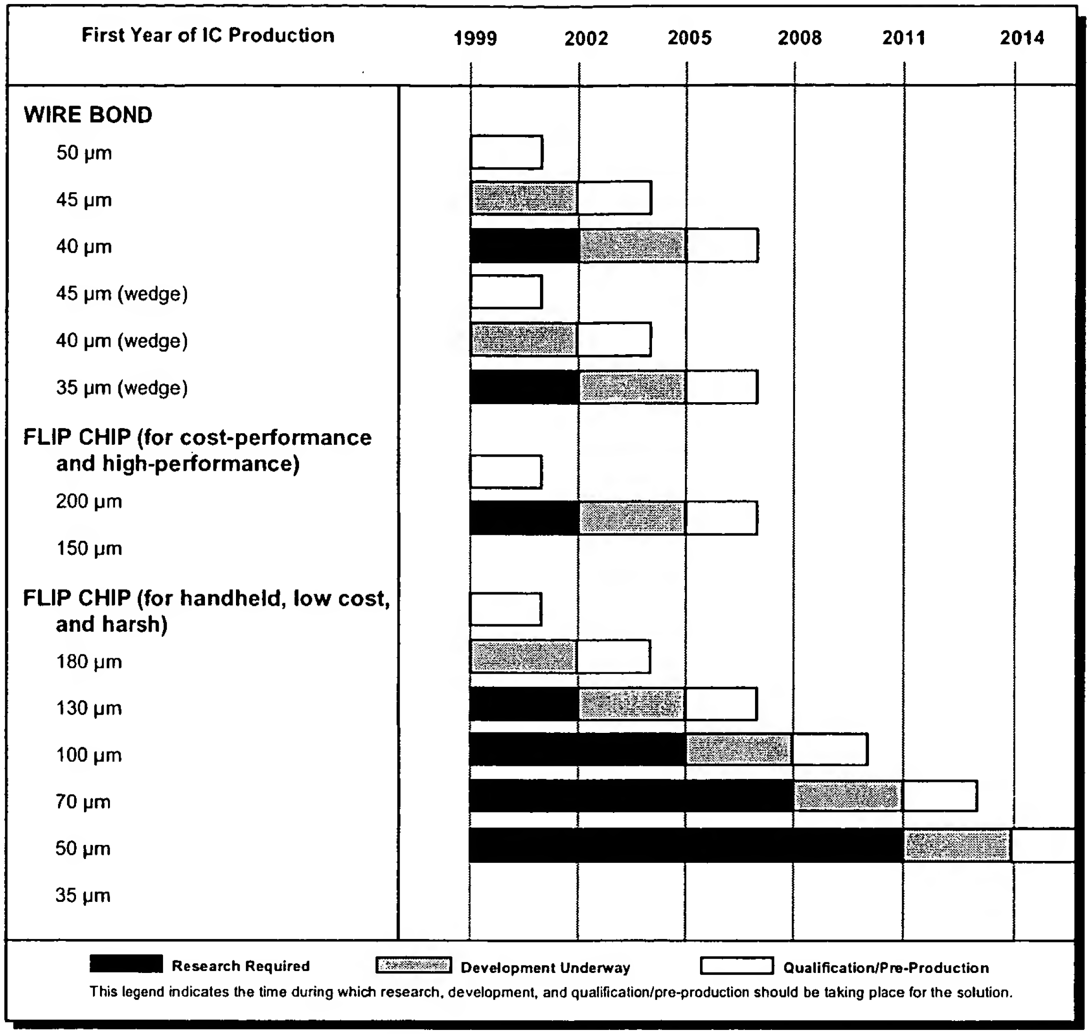


Figure 45 Chip-to-Next Level Interconnect Potential Solutions

To satisfy the high pincount and performance requirements in Table 59a, flip chip will become the predominant technology for chip-to-next level interconnect. Wire bond technology will continue to evolve and will be the dominant interconnect for low-cost products until flip chip costs become favorable. The use of flip chip for low I/O, but high frequency, RF packaging will be discussed in a later section. Size, weight, and performance driven products will need flip chip interconnect with area array I/O at a pitch of 200 µm or less. This interconnect approach will require compatible underfill and substrate technologies to be available at the necessary performance and cost. A level of interconnect can be eliminated with this technology. Material, process development, and metrology technology improvements will also be required to support flip chip implementation. Flip chip interconnect technology at area array pitches ≤ 150 µm will put extreme pressure on substrate density for I/O escape beneath the chip site. Substrate redesign is usually necessary to accommodate flip chip interconnect chip shrinks.

ENCAPSULATION AND UNDERFILL

To achieve rugged, low-cost packaging and meet electrical and thermal requirements, ball grid array (BGA) packages will need lower cost, low-stress, low-viscosity, high T_g mold compounds. To address the CTE mismatches between the chip and substrate, flip chip interconnect on organic substrates will require underfills that exhibit improved reliability, manufacturability (faster dispense/cure), better interface adhesion, and lower moisture absorption. Underfill solutions must be compatible with standard surface mount processes and equipment without increasing cycle time.

SINGLE-CHIP PACKAGES

BALL GRID ARRAY PACKAGES

For many applications in the 200+ pincount range, BGA packages will provide potential solutions. Many BGAs will utilize a wire bond interconnect on the periphery of the ICs. Area array flip chip connections to BGAs will be needed for high I/O or high power chips. Plastic ball grid arrays (PBGAs) will require the use of liquid encapsulants as underfills to reduce the shear stress load on the flip chip interconnections, due to the large difference in the CTE between the silicon IC and the organic substrate. The bending of the encapsulated flip chip on PBGAs may become excessive for large chip sizes and could impact the thermal cooling path. The space transformation between the tight pad pitch on the IC chip and the relatively large pitch between the plated through hole (PTH) on the substrate is totally contained in the PBGA package. The area array solder balls beneath the BGA package have the same pitch as that of the PTH or PTH pad on the substrate. To minimize the number of signal layers on the wiring board, the signal leads underneath the BGA can be confined to the outer several rows. The inner rows are taken by the IC chip and wire bond interconnections for the cavity-down BGA. For the cavity-up BGA, the inner rows are either not used or are restricted for voltage and ground connections. Table 62 shows the maximum possible pincount for potential BGA package solutions with respect to the solder ball array pitch. The inner one third of solder ball rows are excluded from the pincount calculation in this table. If necessary, these inner rows may be used for voltage and ground connections without adding substrate complexity.

Table 62a Single Chip Packages: Ball Grid Array Packages—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
*BGA **solder ball** Pitch (mm)*							
Low cost	1.27	1.27	1.27	1.27	1.00	1.00	1.00
Hand-held	1.27	1.27	1.00	1.00	1.00	1.00	1.00
Cost-performance	1.27	1.27	1.00	1.00	1.00	1.00	1.00
High-performance	1.00	0.80	0.80	0.80	0.80	0.80	0.65
Harsh	1.27	1.27	1.27	1.27	1.00	1.00	1.00
BGA Possible Pincount							
Low cost	312	312	392	392	420	512	512
Hand-held	392	420	512	512	512	576	684
Cost-performance	840	840	1012	1012	1200	1352	1568
High-performance	1680	1860	2112	2380	2664	2964	3280
Harsh	312	312	392	392	420	512	512

A = integer (BGA size/pitch); R = integer (A/3); pincount = (A-R) × R × 4; body sizes rounded to nearest JEDEC size

Table 62b Single Chip Packages: Ball Grid Array Packages—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
BGA solder ball Pitch (mm)			
Low cost	**1.0**	**0.8**	**0.8**
Hand-held	**0.8**	**0.8**	**0.65**
Cost-performance	**0.8**	**0.8**	**0.65**
High-performance	**0.65**	**0.5**	**0.5**
Harsh	**1.0**	**0.8**	**0.8**
BGA Possible Pincount			
Low cost	**684**	**800**	**968**
Hand-held	**800**	**968**	**1200**
Cost-performance	**2112**	**2664**	**3612**
High-performance	**3612**	**6844**	**8448 ***
Harsh	**684**	**800**	**968**

A = integer (BGA size/pitch); R = integer (A/3); pincount = (A-R) × R × 4; body sizes rounded to nearest JEDEC size

** This is the I/O limit for the 50 mm BGA package, and is not sufficient for the 8758 pins shown in Table 59a.*

FINE PITCH BGA /CHIP SCALE PACKAGES

Fine pitch BGA/chip scale packages (FBGA/CSP) provide a potential solution where low weight and small size are requirements. These packages are only slightly larger than the chip itself, and are available in a variety of configurations and materials combinations. The size may range from 4 to 21 mm. The 21 mm FBGA/CSP is for the high lead count applications. Table 63 shows examples of the maximum possible pincount for depopulated area array FBGA/CSP solutions with respect to the 10 and 21 mm package sizes, array I/O pitch, and number of rows. For these packages the solder ball pitch is a fraction of the PTH on the printed wiring board (PWB). Fan-out wiring connections are required on the PWB to reach the PTH. To minimize the fan-out requirements, only a few of the outer rows of the area array connections are used. FBGA/CSPs at 0.5 mm pitch will put pressure on the PWB interconnect density for I/O escape to reach the inter-level vias or the PTH in the PWB. When the number of rows accessed is four or higher, a build-up layer on the PWB will be needed.

These packages provide potential advantages of higher performance, higher density, and chip shrink transparency. For applications where FBGA/CSPs are redesigned to the minimum size possible each time the chip size is reduced, this redesign will drive a corresponding redesign of the PWB onto which the packages are assembled.

Table 63a Single Chip Packages Potential Solutions: FBGA/CSP—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
FBGA/CSP area array pitch (mm)	**0.5**	**0.5**	**0.4**	**0.4**	**0.4**	**0.4**	**0.4**
FBGA/CSP size (mm/side)	**10**	**10**	**10**	**10**	**10**	**10**	**0.4**
# Rows/# leads (one fan-out layer)	**3/192**	**3/192**	**3/252**	**3/252**	**3/252**	**3/252**	**3/252**
# Rows/# leads (two fan-out layers)	**4/420**	**4/420**	**4/320**	**4/320**	**4/320**	**4/320**	**5/380**
FBGA/CSP size (mm/side)	**21**	**21**	**21**	**21**	**21**	**21**	**21**
# Rows/# leads (one fan-out layer)	**3/456**	**3/456**	**3/576**	**3/576**	**3/576**	**3/576**	**3/576**
# Rows/#leads (two fan-out layers)	**4/592**	**4/592**	**4/752**	**4/752**	**4/752**	**4/752**	**5/920**

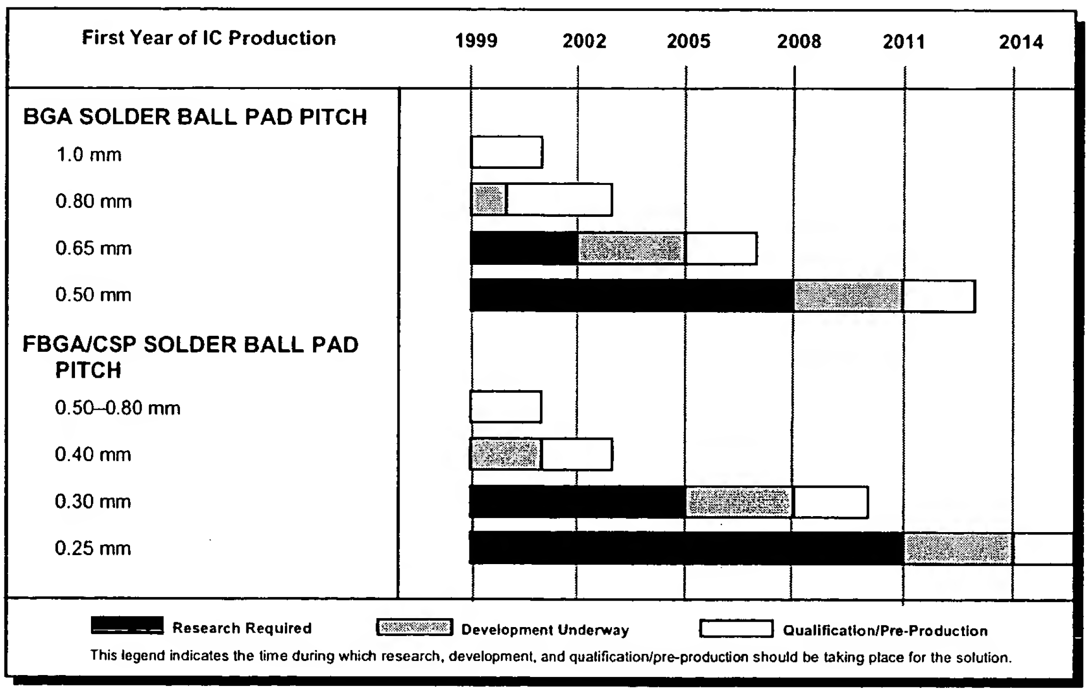
A = integer (CSP size/pitch-1); R = # rows, # leads = (A-R) × R × 4

Table 63b Single Chip Packages Potential Solutions: FBGA/CSP—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
FBGA/CSP area array pitch (mm)	0.3	0.3	0.3
FBGA/CSP size (mm/side)	10	10	10
# Rows/# leads (one fan-out layer)	3/348	3/348	3/432
# Rows/# leads (two fan-out layers)	5/540	6/624	6/792
FBGA/CSP size (mm/side)	21	21	21
# Rows/# leads (one fan-out layer)	3/792	3/792	3/960
# Rows/# leads (two fan-out layers)	5/1280	6/1512	6/1840

A = integer (CSP size/pitch-1); R = # rows, # leads = (A–R) x R x 4

Figure 46 illustrates polymer single chip packaging BGA and FBGA/CSP solutions as a function of area array pitch.



* *FBGA packages have solder balls at a pitch that is a fraction of the PWB PTH pitch. Fan-out wiring is needed on the surface of the PWB*

Figure 46 Potential PWB Solutions for BGA and FBGA/CSP Packages

HIGH DENSITY PACKAGE SUBSTRATES AND PRINTED WIRING BOARDS (PWBS)

To accommodate BGA packages in 1999 for the high-performance market segment, the PWB should have PTH at 1.00 mm pitch, with a sufficient number of signal layers to access 14 outer rows underneath the BGA package. The PTH pitch on the PWB should reduce with time as indicated in Table 63 and Figure 46.

To accommodate FBGA/CSP solutions in 1999, the metal wiring on the top layer of the PWB needs to access the three outer rows. This means that the PWB should be capable of placing two signal lines between the two adjacent pads at 0.5 mm pitch as indicated in Table 64. Build-up layers may be used to access the fourth and higher rows, which are included in Table 63.

Table 64a Potential PWB Solutions for BGA and FBGA/CSP Package—Near Term

YEAR *TECHNOLOGY NODE*	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*
FBGA/CSP solder ball pad pitch (mm)	**0.5**	**0.5**	**0.4**	**0.4**	**0.4**	**0.4**	**0.4**
Pad size (µm)	**200**	**200**	**160**	**160**	**160**	**160**	**160**
Line width (µm)	**60**	**60**	**48**	**48**	**48**	**48**	**48**
Line spacing (µm)	**60**	**60**	**48**	**48**	**48**	**48**	**48**
# Rows accessed	**3**	**3**	**3**	**3**	**3**	**3**	**3**

Table 64b Potential PWB Solutions for BGA and FBGA/CSP Package—Long Term

YEAR *TECHNOLOGY NODE*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
FBGA/CSP solder ball pad pitch (mm)	**0.3**	**0.3**	**0.25**
Pad size (µm)	**120**	**120**	**100**
Line width (µm)	**36**	**36**	**30**
Line spacing (µm)	**36**	**36**	**30**
# Rows accessed	**3**	**3**	**3**

The most stringent needs are for substrates that are compatible with flip chip solutions for the cost-performance and high-performance applications. Table 65 illustrates key substrate features shown as a function of the flip chip pad pitch, pad size, and line width/spacing. When the outermost row of chip pads are de-populated by 50%, one may place three lines between the pads at a two-pitch distance. For example, in 1999, one may place three 42.5-µm lines between the two pads at the 400 µm center-to-center distance. This gives 4 lines per 2 pitches, resulting in the equivalence of accessing 2.0 rows per fan-out layer, or 4 rows per two fan-out layers for the cost-performance applications. Similarly, one may place five 27-µm lines between these two pads, and achieve the equivalence of accessing 3.0 rows per fan-out layer as shown in Table 65.

All of the signal I/O pads and some of the voltage and ground pads are assumed to locate on a few of the outer rows, as shown in the Table 65. Each of these outer row pads requires a fan-out redistribution wire on the top side of the package substrate to reach a through via or PTH on the substrate. The via or PTH then connects to the global wiring, if this is a few chip packaging substrate or it is connected to a solder ball underneath, constituting a BGA package. The numbers of leads shown in Table 65 are equal to or greater than the pincount shown in Table 59, but very often less than the pad count numbers on the IC. These additional voltage and ground pads needed are located in the inner rows, and connected to voltage and ground pads in the outer rows. When the IC chip size is shrunk to optimize wafer productivity, substrate redesign is usually necessary to accommodate chip shrink.

Table 65 addresses substrate escape wiring only. The large number of outer rows accessed reaches 17 rows at 150 µm pitch for the 50 nm generation. This means that some of the fan-out wire could reach a length of 2.55 mm or longer underneath the IC, plus additional length beyond the IC but still on the package substrate. Crosstalk noise between two parallel fan-out wires on the package substrate should be carefully assessed at the design stage.

Global wiring solutions are addressed in the *"National Technology Roadmap for Electronic Interconnections"* (available from the IPC)[46] and in the *"National Electronics Manufacturing Technology Roadmap"* (available from NEMI).[47] These wiring geometries are not sufficiently dense to support moving on-chip wiring onto the substrate. Substrate cost should not exceed 30–50% of the total assembly and packaging cost (cents/pin) shown in Table 59. A possible process for the development of the future high density substrate materials is summarized in Figure 47. The high T_g material is needed to meet the multiple cycles of high temperature reflow during the chip-to-package assembly. It is important for the large chip to have CTE matching between chip and package, and desirable between large packages and PWB. A low dielectric constant material will reduce the capacitance load to meet the electrical performance needs. The low dielectric loss material is needed for the RF applications. And the low moisture absorption will improve the package reliability. Figure 47 illustrates the BGA, fine pitch BGA/CSP, and flip chip interconnect compatible high density substrate solutions as a function of pitch, line width, and line spacing.

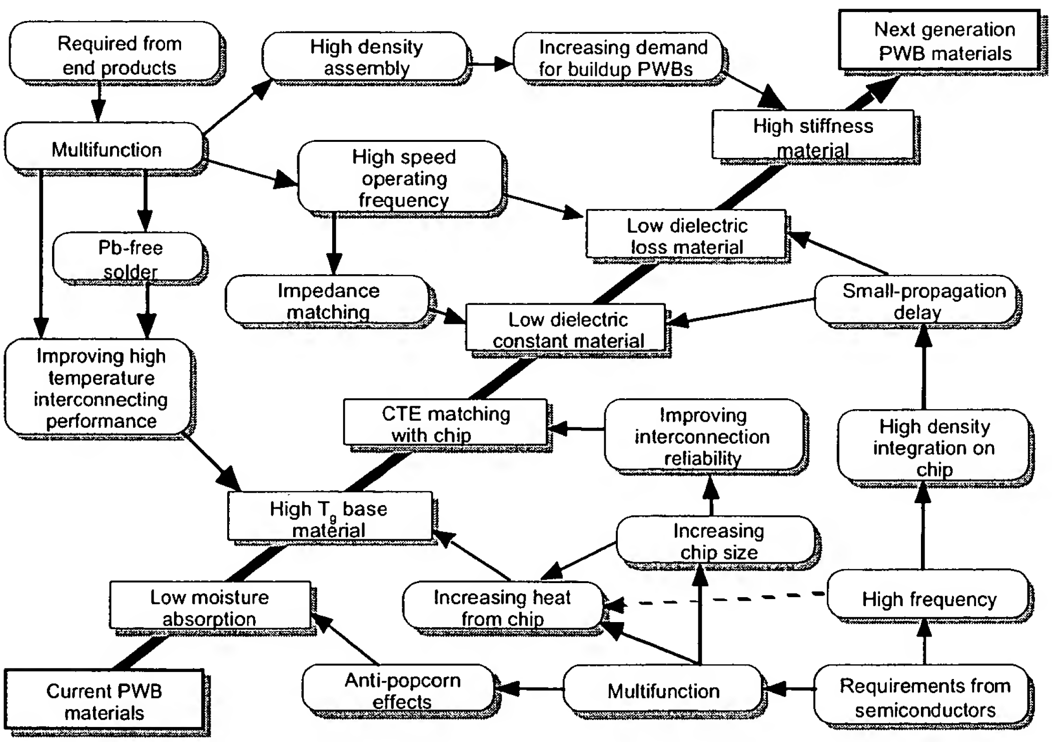


Figure 47 A Potential Procedure for the Development of the High Density Substrate Materials

[46] The Institute for Interconnecting and Packaging Electronic Circuits (IPC). "National Technology Roadmap for Electronic Interconnections." Northbrook, Illinois:IPC, 1997.

[47] National Electronic Manufacturing Initiative, Inc. (NEMI). "National Electronic Manufacturing Technology Roadmaps." Herndon, VA:NEMI, 1998.

Table 65a Flip Chip Substrate Top-side Fan-out Potential Solutions—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
Flip Chip Pad Pitch (µm)	**200**	**200**	**200**	**200**	**200**	**200**	**150**
Pad Size (µm)	**100**	**100**	**100**	**100**	**100**	**100**	**75**
Chip Size (mm/side)							
Cost-performance	**12**	**12**	**12**	**12**	**12**	**12**	**12**
High-performance	**17**	**17**	**17**	**17**	**17**	**17**	**17**
Array size = # pads along chip edge							
Cost-performance (maximum)	**59**	**59**	**59**	**59**	**59**	**59**	**79**
Cost-performance (needed)	**51**	**56**	**51**	**56**	**53**	**58**	**75**
High-performance (maximum)	**84**	**84**	**84**	**84**	**84**	**84**	**112**
High-performance (needed)	**73**	**81**	**79**	**79**	**79**	**81**	**107**
# Outer Rows Accessed (will determine # fan-out layers needed)							
Cost-performance	**4**	**4**	**5**	**5**	**6**	**6**	**5**
High-performance	**6**	**6**	**7**	**8**	**9**	**10**	**8**
Effective Total Wiring Density for Fan-out Need (cm/cm²)							
Cost-performance	**200**	**200**	**250**	**250**	**300**	**300**	**333**
High-performance	**300**	**300**	**350**	**400**	**450**	**500**	**533**
Wiring Substrate (Three or more lines replacing one depopulated pad—accessing 2.0 or more rows per fan-out layer)							
Line width (µm)	**42.5**	**42.5**	**33.0**	**33.0**	**27.0**	**27.0**	**25.0**
Line spacing (µm)	**43.1**	**43.1**	**33.6**	**33.6**	**27.5**	**27.5**	**25.0**
Wiring Substrate (Five or more lines replacing one depopulated pad—accessing 3.0 or more rows per fan-out layer)							
Line width (µm)	**27.0**	**27.0**	**23.0**	**20.0**	**17.5**	**15.5**	**15.0**
Line spacing (µm)	**27.5**	**27.5**	**23.1**	**20.0**	**17.7**	**16.0**	**15.0**
# Leads Accessed							
Cost-performance	**752**	**832**	**920**	**1020**	**1128**	**1248**	**1400**
High-performance	**1608**	**1800**	**2016**	**2272**	**2520**	**2840**	**3168**

A = array size, R = # rows, # leads = (A-R) × R × 4; via pitch must be ≤ pad pitch

Table 65b Flip Chip Substrate Top-side Fan-out Potential Solutions—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
Flip Chip Pad Pitch (µm)	**150**	**150**	**150**
Pad Size (µm)	**75**	**75**	**75**
Chip Size (mm/side)			
Cost-performance	**12**	**12**	**12**
High-performance	**17**	**17**	**17**
Array size = maximum # pads along chip edge			
Cost-performance (maximum)	**79**	**79**	**79**
Cost-performance (needed)	**75**	**75**	**78**
High-performance (maximum)	**112**	**112**	**112**
High-performance (needed)	**112**	**109**	**111**
# Outer Rows Accessed (will determine # fan-out layers needed)			
Cost-performance	**7**	**10**	**14**
High-performance	**11**	**17**	**26**
Effective Total Wiring Density for Fan-out Need (cm/cm²)			
Cost-performance	**467**	**667**	**933**
High-performance	**733**	**1133**	**1733**
Wiring Substrate (Six or more lines replacing one depopulated pad—accessing 3.5 or more rows per fan-out layer)			
Line width (µm)	**17.0**	**11.5**	**8.0**
Line spacing (µm)	**17.5**	**12.1**	**8.6**
Wiring Substrate (Ten or more lines replacing one depopulated pad—accessing 5.5 or more rows per fan-out layer)			
Line width (µm)	**10.5**	**6.5**	**4.0**
Line spacing (µm)	**10.9**	**7.1**	**4.8**
# Leads Accessed			
Cost-performance	**1904**	**2600**	**3584**
High-performance	**4444**	**6256**	**8840**

A = array size, R = # rows, # leads = (A-R) × R × 4; via pitch must be ≤ pad pitch

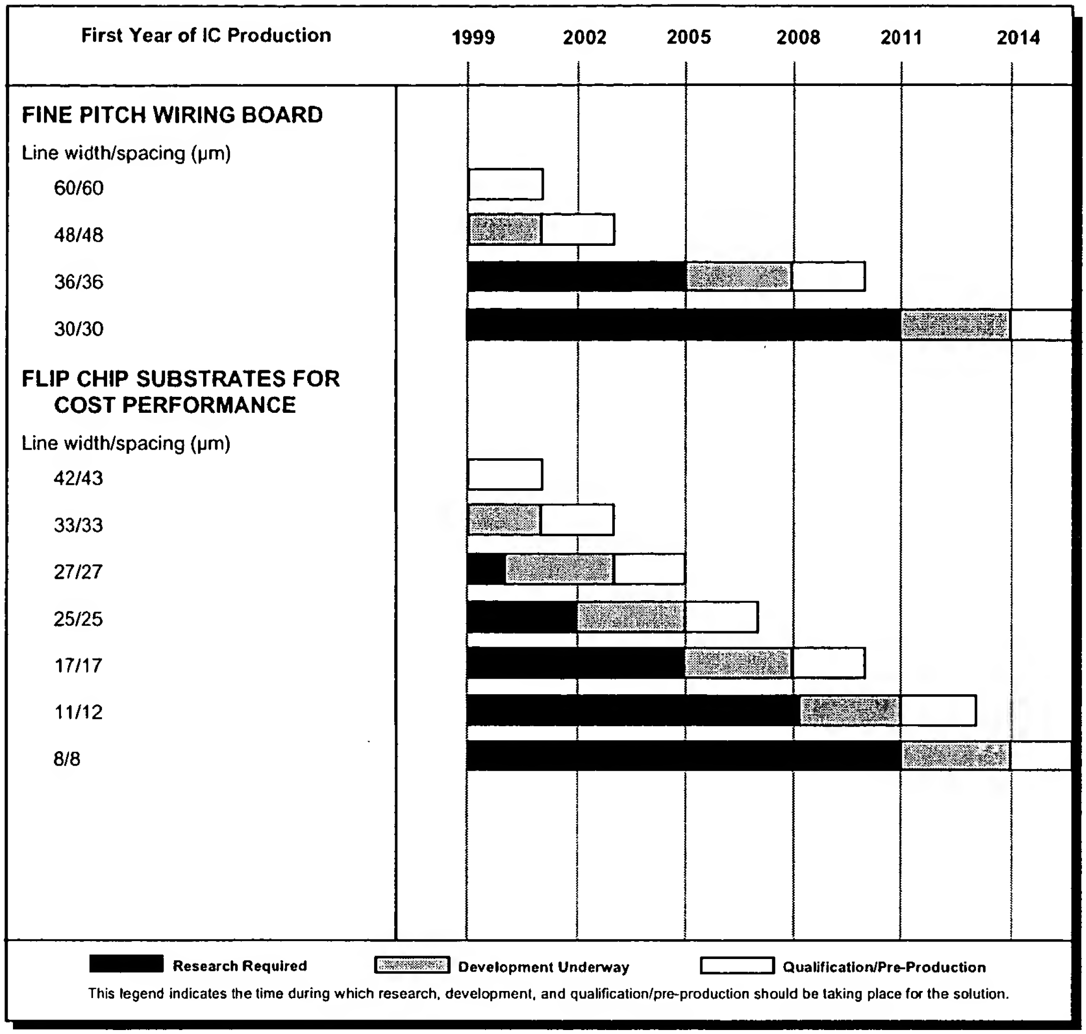


Figure 48 High Density Polymer Substrate Potential Solutions

SYSTEM-ON-A-CHIP PACKAGING

The ever-increasing CMOS density is a very important driving force for SoC in low-cost and hand-held applications. For example, when the lithography feature size improves in the succeeding generation, the chip size of a standalone micro-controller core may be limited by the pad pitch and pad count, and will not reduce accordingly. Very often, the combination of a controller core plus a DSP core may result in a chip I/O count less than either the controller or the DSP core alone and may still fit in such an I/O pad-limited chip area. In other words, the cost of two packages is replaced by one of equal or less cost (the package cost becomes less than one half), and the PWB area being occupied is reduced. This also eliminates many of the off-chip driver circuits and the associated delay time and power consumption. Furthermore, the availability of on-chip wiring may allow substantial increase in the data bandwidth between these two cores, thus improving the performance. Similar benefit may also be achieved by the integration of A/D and D/A converters into the DSP and controller cores after one more technology generation. In some applications, programmability is essential, which may be achieved by a small embedded-Flash memory.

The main challenges in SoC packaging are in maintaining signal integrity and verification. Techniques like de-coupling, shielding, better grounding will be necessary to handle mixed analog and digital signals in a minimum size package. Design emulation and verification of intent will require early packaging involvement in SoC design. The complexity of testing at both the wafer probe and package levels should be considered at the design stage.

In some applications, the chip size is not limited by the I/O pads, even when it should decrease in the succeeding generation. The reduction in chip size will decrease the chip cost. The integration of two cores into one chip may impact the chip yield and increase the overall chip cost. The replacement of two packages by one of equal or less I/O leads may cut the packaging cost by more than a factor of two. The cost of chip plus package may decrease or increase, depending on the individual application. However, the elimination of the off-chip driver delay and power consumption, the reduction in the wiring board area, and the possibility of improved bandwidth between the two cores, may become important considerations for the adoption of the performance-oriented SoC applications.

RF AND MIXED-SIGNAL PACKAGING

The challenges in this area will become increasingly important as low-cost mobile and high bandwidth products drive across several market segments. The increasing performance of silicon IC will enable lower cost solutions in the frequency domain below 2.5GHz. GaAs and increasingly SiGe ICs will be used for higher frequency applications. Signal integrity and cost issues become dominant. Flip chip attachment to package and embedded passives on the package will be key enabling technologies to package level performance. Low inductance and high-density packages like FBGA/CSP will enable designers to use lower cost partitioning solutions than the traditional ceramic modules.

Integrated modeling and simulation tools are required to drive down design cycle time to acceptable levels. Performance, physical size, and cost driven integration will continue to arrive at a single chip radio that combines memory, processor and mixed-signal functions, as discussed above. Fast design cycle time and accurate simulation at both the chip and package levels are enablers of this integration. High-speed test and higher level of functional test at the package level also become development challenges. Microelectromechanical Systems (MEMS) will be used in the fabrication of filter, switch, oscillator and other components in the next 2–4 years. They offer the benefit of small size, low insertion loss, low power consumption, integration with ICs, and the potential of low cost with batch fabrication. Reliability, potential temperature sensitivity, and hermetic/vacuum packaging of MEMS devices are key development challenges.

MULTI-CHIP PACKAGES / MULTI-CHIP MODULES / SYSTEM-IN-A-PACKAGE (SIP)

The production volumes of MCMs have lagged behind expectations in the marketplace but tracked the acceptance of the flip chip bump technology by the system houses. However, few-chip modules (2–3 chips) are in volume production, and by extending the definition of MCPs to include RF and mixed-signal products, it is now expected that 4–5 chips (or more complex) modules will be common in the next few years. The MCP is often referred to as the system-in-a-package (SiP), which addressed the time-to-market needs. As the SoC becomes feasible, technically and economically, the number of ICs on the MCP will reduce to realize product cost and size reduction.

For certain limited volume, high-performance products using classical (complex) MCMs will be the system technology of choice because they provide the best cost and performance package solution. Very often, tens of logic and memory chips with high I/O leads are placed at close proximity to minimize the time-of-flight delay between chips. In fact, the wiring capacity needed to implement such systems on ceramic MCMs is one order of magnitude larger than the plastic MCM technology can support today. The important considerations are the overall system cost, the system performance needs, and the reliability of the CMOS based system, not the cost of the packaging alone. Because the DCA for extremely high I/Os is available for MCMs now, and is expected for the plastic MCMs in the future, the whole system can be placed in a very small area that permits the lowering of the junction temperature through standard refrigeration techniques. This capability increases the reliability of the CMOS chips by 3–5 times and the performance of the CMOS

chips by up to 15%. Since the drive for better system reliability is expected to increase in the future, more extended used of MCMs in the system design will follow.

In general, MCP/MCM/SiP will be driven by densification and cost reduction for low-end products, and by densification and performance for high end products. It is likely that the flip-chip technology will pervade the MCP/MCM/SiP technology (whether few chip MCP or classical MCM) so that the enabling solutions for flip-chip technology (such as underfill) become among the enabling solutions for MCP/MCM/SiPs. Other enabling solutions for MCP/MCM/SiPs are 1) special physical design tools that facilitate performance-driven place-and-route for simple or complex MCP/MCM/SiPs, 2) high density substrate and metallization technology, and 3) low-cost, available known good die. Chip reworkability and module testing will be major factors in determining the feasible complexity of multi-chip modules.

RELIABILITY ISSUES

Factors compounding the increase in packaging complexity brought by new materials and package formats include the introduction of copper as a replacement for aluminum as the chip interconnect, the replacement of SiO_2 as the interlevel dielectric material, the introduction of direct chip attach, and area array interconnect. These multiple changes represent an increased risk to packaged device reliability. It is essential that materials characterization data be available before new materials are introduced.

New package designs, materials, and technologies will not be capable of reliable performance in all market applications. More in-depth knowledge of the relevant failure mechanisms coupled with knowledge of the market use conditions will be required to bring new package technologies to the marketplace. Guidelines for environmental expectations for market application segments would facilitate package development tailored to the market needs and help ensure consistent reliability performance among suppliers as well as between suppliers and customers. More research emphasis on physical and thermo-mechanical models of failure mechanisms is needed to support this trend.

Co-development of package/interconnect technologies with their fault isolation tools is needed to help accelerate technology introduction. Conception and development of tools for rapid and non-artefactual electrical and physical fault isolation of package and interconnect technologies is critical. Faster techniques are needed to execute statistically significant studies of material bulk and interface properties. Developing extensions of current fault isolation and package analytical technologies (such as X-ray, acoustic, and Moire) needs to be balanced with development of new technologies for small defect visualization (such as X-ray tomography). Organic chemical interface analysis techniques are growing in importance with the introduction of new organic materials. Low alpha materials need to be considered during the timeframe of the ITRS to reduce errors induced by alpha radiation. Measurement techniques and standards for alpha radiation effects are not adequate to support the increased alpha sensitivity anticipated for advanced technology processes.

Interfacial delamination will continue to be a critical reliability hazard that is worsened by the trend to larger chips and new materials. Standard methods and acceptance criteria for interfacial adhesion are lacking. Fundamental work is needed to establish adhesion strength and degradation rate versus environmental factors (temperature, relative humidity) as well as a function of interfacial physical (such as roughness, composition) and chemical (van der Waals, dipole, covalent) properties. The CTE mismatch between the chip and the substrate should be reduced to mitigate large chip packaging-related reliability issues.

New electrostatic discharge (ESD) test methods and equipment are required to comprehend increasing pincount and shrinking interconnect pitch. Improved handling solutions for bare chip and packaged devices will help ESD related reliability issues.

CROSSCUT NEEDS

ENVIRONMENT, SAFETY, AND HEALTH

Assembly & Packaging must consider potential risks or challenges that may be passed onto the interim buyer and the final consumer. Materials used should allow for hazard-free handling and eventual disposal or recycling. Because the majority of assembly and packaging is located offshore, multiple jurisdictions and regulatory bodies must be considered.

Table 66 Assembly & Packaging ESH Needs and Potential Solutions

ISSUES AND CHALLENGES	*POTENTIAL SOLUTIONS*		
	1-5 YEARS	*5-10 YEARS*	*10-15 YEARS*
Regulatory pressure to reduce use of Pb in lead finish and flip-chip solder bump application by 20% (elimination for European automotive application)	Ensure that alternative material does represent overall improvement from ESH perspective	Reduce use of Pb in lead finish and flip chip solder bump application by 80%	Elimination of Pb for lead finish
Several chemicals currently used in assembly/packaging processes represent potential risks to workers and the environment	Improved management of current set of hazardous chemicals used in plating processes to reduce potential risks to workers, including plating baths for: -Cu -Ni -Au -Co -Pb	Ensure that all hazardous chemicals used in flip chip and bump technology (and other new packaging technologies) undergo evaluation through application of DFESH* tools to ensure continuous improvement in ESH maintains pace with new process developments and effectively screens out undesirable chemicals and processes	Identify and implement processes that use ESH-benign materials
Eliminate use of Kr-85 for fine leak tests	Replace with processes using He or other inert material		
Need to integrate ESH considerations into equipment design	SEMI S2/S8 applied to assembly/packaging tools; tool ESH evaluations ensure that no single point failure may result in life threatening risk	SEMI S2/S8 applied to 100% of all assembly/packaging tools performed by 3rd party evaluation	
Eliminate use of cadmium (such as rust protector)	Find suitable alternative		
Eliminate use of antimony-trioxide as flame retardant in mold compound	Find suitable alternative		
Elimination of brominated flame retardants	Find suitable alternative		
Elimination of beryllium as substrate material			Find suitable alternatives

Table 66 Assembly & Packaging ESH Needs and Potential Solutions (continued)

ISSUES AND CHALLENGES	POTENTIAL SOLUTIONS		
	1–5 YEARS	5–10 YEARS	10–15 YEARS
Pressure to reduce water consumption in plating and other processes	Implement water recycling/reuse programs reducing overall consumption by 20%	Implement water recycling/reuse programs reducing overall consumption by 50%	
Pressure to reduce energy consumption	Improve efficiency of mold presses, furnaces, and other high energy consumption equipment to reduce overall energy uses by 20%	Improve efficiency of mold presses, furnaces, and other high energy consumption equipment to reduce overall energy uses by 50%	
Pressure to reduce chemical usage and consumption	Improved recycling of chemicals in plating operations; reduce overall usage by 20%	Improved recycling of chemicals in plating operations; reduce overall usage by 50%	Improved recycling of chemicals in plating resulting in zero-discharge operation
Minimize waste mold compound material		Thermo-plastic versus thermo-set to optimize use of mold compound (reduce unused trim material or runners	
Product take back			ESH benign chip packages that can be returned to manufacturer or reprocessor for reuse

* *DFESH—design for ESH*

METROLOGY

SCOPE

Assembly and packaging will continue to play a significant and increasing role in the size, performance, and cost of future electronic systems. This section summarizes the metrology challenges associated with assembly and packaging. This is not an exhaustive summary, but it attempts to highlight the most critical areas of interest.

CURRENT TECHNOLOGY STATUS AND FUTURE NEEDS

Table 67 Assembly & Packaging Modeling and Metrology Crosscut Issues

ASSEMBLY AND PACKAGING METROLOGY NEEDS	SUMMARY OF ISSUES
Coordinated electrical modeling and simulation tools for chip, package and system	Runtime and input preparation efficiency (results in minutes, not days) Efficient noise modeling and simulation, including radiated noise SPICE-compatible time domain simulation capability utilizing mixed RLCG-active device frequency domain models Simulation-efficient modeling algorithms and techniques that allow extraction of either element values or frequency domain models and subsequent network or order reduction Efficient full-wave analysis techniques that generate models instantiated as "stamps" in time domain simulators Integration of electrical, thermal and cost modeling, and simulation tools

Table 67 Assembly & Packaging Modeling and Metrology Crosscut Issues (continued)

ASSEMBLY AND PACKAGING METROLOGY NEEDS	SUMMARY OF ISSUES
Improved interpretation of accelerated stress tests for process and product qualification	Modeling and simulation of accelerated stress test techniques needed to qualify manufacturing processes, and to improve the lifetime and successful operation of the product
Modeling and simulation of interfaces (thermal performance, reliability, yield, and cost are driven by understanding of interfaces)	Need to model, design, and control the basic mechanisms (physical, chemical, mechanical) for interface bond strength (adhesion)
Thermal and mechanical simulation models of packages and assemblies	Comprehensive thermal and mechanical model tools fully supported by "real life" materials data
Material parameters	Measurement, collection, and dissemination of materials properties of packaging materials for the sizes, thicknesses, and temperatures of interest
Material application and assembly process control	Improvements in the online measurement of solder systems, solder alternatives, underfills, encapsulants, attachment materials, in the manufacture of packages and bumped chips

MODELING AND SIMULATION

Assembly & Packaging technologies are driven to simultaneously meet very demanding requirements in the areas of performance, power, junction temperature, and package geometries. Therefore, advanced modeling tools are needed that cover electrical, thermal, and mechanical aspects.

These phenomena can no longer be described independently. Major advances are needed in the individual tools and in their integration to achieve a self-consistent solution and to integrate or coordinate with chip design software. To move to 3 GHz chip-to-board speeds, the modeling of electrical signal propagation, noise, and radiation needs to be improved substantially both in computational (run time) and input efficiency, and in ability to address realistic complexity, configurations, and conductor density. Mechanical stresses need to be coupled between chip and package level. The introduction of low κ dielectrics with low thermal conductivity will increase the need for accurate thermal simulation, which needs to be solved consistently with electrical behavior given the higher power dissipation levels.

ELECTRICAL SIMULATION MODELS OF PACKAGES AND SYSTEMS

Modeling the electrical behavior of systems of chips packaged individually or collectively in single or multi-chip packages is pushing the practical limits of what can be done in a cost and time effective manner, even at existing clock frequencies. Extension of modeling and simulation techniques to higher clock frequencies and higher densities will require significant research in order to provide useful design capability. Other reduction techniques, either time-domain or frequency-domain, will be required to achieve useable run times. Full-wave simulation tools will be required in order to deal with some complex structures, and they must be computationally efficient. Integration or interfacing of package- and chip-level design and simulation systems will be a necessity as the options for interconnect placement (on-chip or on-substrate) occur. Integrated chip, electrical (architecture), mechanical, thermal, and cost modeling tools will be a useful tool for integrated design and manufacturing teams, with potential for cycle time reduction.

THERMAL AND MECHANICAL SIMULATION MODELS OF PACKAGES AND ASSEMBLIES

The industry continues to increase power dissipation, junction temperature, and reliability expectations that push the cooling and mechanical strength limits of electronic products. More comprehensive thermal and mechanical model tools fully supported by "real life" materials data correlated with physical measurements are needed. Examples include fluid and solid models for air flow characteristics, stress predictions in accelerated tests and power cycles, micro-models for interface fracture behavior, and macro structure models for package dynamics behavior including vibration and mechanical shock. These model methods are also

being applied to manufacturing and assembly processes such as adhesive/underfill flow or BGA rework. Better experimental capability for measurement of *in situ* properties, location, and characterization of defects and failures are needed. Key is development of *in situ* model mechanism elucidation and validation tools such as micro-Moire, nano indentation techniques, and interface fracture toughness techniques.

MEASUREMENT AND MODELING OF INTERFACES

Assembly and packaging thermal performance, reliability yield, and cost are driven by the understanding of interfaces and ability to characterize, control, and strengthen them. The ability to accurately qualify, and perhaps design and control the interface performance, will remain crucial to future cost-effective development and manufacturing. The key is to fully characterize the basic mechanisms (physical, chemical, mechanical) for interface bond strength (adhesion) between metal/polymer, polymer/polymer, and metal/inorganic dielectric materials, as well as to quantitatively qualify the very low levels of complex organics present at these interfaces through manufacturing processes. This understanding will be crucial to improve the interface integrity.

International Technology Roadmap for Semiconductors
1999 Edition

Environment, Safety, and Health

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ENVIRONMENT, SAFETY, & HEALTH

SCOPE

BACKGROUND

The semiconductor industry views responsible performance in environment, safety and health (ESH) as critical to success. Continued ESH improvement is a major consideration for semiconductor manufacturers, whose business approach to ESH employs strategies that are integrated with manufacturing technologies, products, and services. This approach is structured around the belief that good business stewardship includes an active awareness and commitment to responsible environmental, safety, and health practices. Addressing these areas aggressively has resulted in the industry being an ESH leader as well as a technology leader. Now, as a result of global collaboration, the first International Roadmap for ESH in the Semiconductor industry has been developed. This roadmap identifies R&D challenges that may impact ESH as new technology requirements are identified.

EXPECTATIONS

For both engineers and research scientists, this roadmap identifies ESH R&D challenges that occur as new design, wafer processing and assembly technologies are created. Technology requirements are listed in Tables 69–73. It also proposes possible technology and management solutions to meet the challenges, as illustrated in Figures 49–53.

By giving direction to research centers, suppliers and semiconductor manufacturers, this roadmap focuses the search for solutions. ESH integration into manufacturing and business practices is clearly a priority. A high expectation of success and improvement requires that ESH must be integral to the thoughts and actions of process, equipment, and facilities engineers, and to university researchers. These improvements must meet local, national, and international needs, with positive impact on cost, technical performance and product timing, and minimization of risk, public and employee health effects, and environmental impact. Solutions must be timely, yet far reaching, to assure long-term success. The combined efforts of international initiatives and other notable ESH-focused entities sponsored by the semiconductor industry, universities and government will be a result of the internationalization of this roadmap.

DIFFICULT CHALLENGES

Five global ESH challenges essential to a synergistic ESH strategy and that must be integrated into the technical thrust areas are: *Chemicals, Materials, and Equipment Management, Climate Change Mitigation, Workplace Protection, Resource Conservation, and ESH Design and Measurement Methods. Chemicals, Materials, and Equipment Management* must provide timely ESH information to equipment design engineers and equipment users regarding the environmental, safety and health characteristics of potential new process chemicals and materials. This information is essential to the selection of optimal chemicals and materials for function and ESH impact with respect to reaction product emissions, health and safety properties, materials compatibility with both equipment and other chemical components, flammability and reactivity while minimizing unnecessary business impact after processes are developed and in production. *Climate Change Mitigation* is a major consideration because it potentially could limit the use of energy and chemicals essential to the manufacturing process. *Workplace Protection* is always among the top priorities for our industry. As more is known about potential work environment impacts on health and safety, technology improvements need to be made in facilities, equipment, personal protective equipment, and training. *Resource Conservation* (water, energy, chemicals, and materials) will grow in importance with respect to availability, cost reduction, manufacturing location, sustainability, and waste disposal. To address the above issues in a cost-effective and timely way, improved *ESH Design and Measurement Methods* are needed to enable a greater number of people to make sound, balanced, choices and decisions.

Table 68 ESH Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥ 100 *nm / BEFORE 2005*	*SUMMARY OF ISSUES*
Chemicals, Materials and Equipment Management	*Chemical Data Collection* Need to document and make available environment, safety, and health characteristics of chemicals. *New Chemical Assessment* Need for quality rapid assessment methodologies to ensure that new chemicals can be utilized in manufacturing, while protecting human health, safety, and the environment without delaying process implementation. *Environment Management* Need to develop effective management systems to address issues related to disposal of equipment, and hazardous and non-hazardous residue from the manufacturing process.
Climate Change Mitigation	*Reduce Energy Use Of Process Equipment* Need to design energy efficient larger wafer size processing equipment. *Reduce Energy Use Of The Manufacturing Facility* Need to design energy efficient facilities to offset the increasing energy requirements of higher class clean rooms. *Reduce High Global Warming Potential (GWP) Chemicals Emission* Need ongoing improvement in methods that will result in emissions reduction from GWP chemicals.
Workplace Protection	*Equipment Safety* Need to design ergonomically correct and safe equipment. *Chemical Exposure Protection* Increase knowledge base on health and safety characteristics of chemicals and materials used in the manufacturing and maintenance processes, and of the process byproducts; and implement safeguards to protect the users of the equipment and facility.
Resource Conservation	*Reduce Water, Chemicals And Materials Use* Requirements for large amounts of water, chemicals, and materials limit sustainable growth. *Waste Recycle* Increase in resource use as the result of increasing process complexity will require that efficient waste recycling methods be developed.
ESH Design and Measurement Methods	*Evaluate and Quantify ESH Impact* Need integrated way to evaluate and quantify ESH impact of process, chemicals, and process equipment, and to make ESH a design parameter in development procedures for new equipment and processes.

Table 68 ESH Difficult Challenges (continued)

FIVE DIFFICULT CHALLENGES < 100 nm / BEYOND 2005	SUMMARY OF ISSUES
Chemicals, Materials and Equipment Management	*Chemical Use Information* Rapid introduction of chemicals and materials into new process requires the understanding of process fundamentals in order to reduce ESH impacts.
Climate Change Mitigation	*Reduce Energy Use* The importance of reducing energy use for climate change will grow. *Reduce High GWP Chemicals Emissions* No known alternatives and international regulatory pressure to reduce emissions of GWP chemicals.
Workplace Protection	*Equipment Safety* Need ergonomic principles integrated into the processing and wafer moving equipment for both operation and maintenance aspects, and into the overall manufacturing facility.
Resource Conservation	*Reduce Water, Energy, Chemicals And Materials Use* Need resource efficient processing and facility support equipment and improved water reclaim and recycling methods. Emphasis on resource sustainability will grow.
ESH Design and Measurement Methods	*Evaluate and Quantify ESH Impact* Need integrated ESH design in development of new equipment and processes.

ESH TECHNOLOGY REQUIREMENTS AND POTENTIAL SOLUTIONS

CHEMICALS, MATERIALS AND EQUIPMENT MANAGEMENT

Risk assessment—Prior to employing a new chemical material, it is necessary to accurately and quickly evaluate the safety, health danger and environmental load/impact. A decision is then made whether to employ the chemical, based on the quantity to be used, the method to be employed and the risk assessment. Operator and maintenance worker exposure to the chemical material must be reduced for safety and health reasons, and emissions must be controlled to minimize environmental load/impact.

Safety and environmental load/impact evaluation of new materials and new chemicals—The safety, health hazards, and environmental load/impact of new materials and chemicals must be evaluated.

It is necessary to identify the path by which the environmental load/impact material is emitted (including the control of waste material), to find alternative materials, or to develop recovery/treatment technology.

Reduction of environmental load/impact materials and chemicals—Efforts have been made to find alternative materials, especially for greenhouse gases and ozone-depleting substances. Alternative materials for bromine and antimony used as fire resistant materials in plastic packages, and lead used for soldering and tinning, are being developed.

Environment management—It is necessary to control the chemicals and materials in each plant to reduce the quantity used and their emissions. Therefore, a material balance control system is needed. A system for automatically collecting data will be needed as the number of target chemicals and materials expands. Life Cycle Analysis (LCA) on materials is currently performed using manual data collection and reporting. An automatic data collection system should be established.

CLIMATE CHANGE MITIGATION

Energy consumption has increased owing to the increased energy consumption of the manufacturing equipment for more complex semiconductors, larger wafer diameter, and the increase of air conditioning energy consumption for higher cleanliness of the cleanroom. Changes in areas such as cleanroom design, equipment design, and wafer transfer/storage methods are needed. In addition to the energy saving of the semiconductor manufacturing equipment, it is necessary to reduce the elements that increase the heat load/impact to the cleanroom. Potential solutions for energy are shown in Figure 50.

Global climate change concerns are driving international efforts to reduce emissions of greenhouse gases, such as PFCs used in semiconductor manufacturing.

WORKPLACE PROTECTION

For equipment, processes, maintenance, factory design, and factory integration, the industry must accept and fully employ standard protocol for hazard control utilizing the following ranking for solutions: a) hazard elimination, b) engineering controls, c) administrative controls, and d) personal protective equipment (PPE).

Increases in wafer size and throughput will require wafer handling systems that may increase worker risk during operation and maintenance. The movement of automated system- and people-guided wafer transport systems and their interface with manufacturing equipment are potentially dangerous to nearby workers. Design controls and procedures comprehending ergonomics and robotics to improve equipment operability and prevent incorrect operation need to be established.

An industry need exists for safe, cost-effective materials of construction. Fire-resistant, process-compatible materials that meet the needs of manufacturing and the expectations of insurers are necessary.

Electromagnetic waves exhibit various wavelength-dependent characteristics. When the wavelength used for pattern exposure is shortened to the X-ray region, the health effects must be evaluated.

RESOURCE CONSERVATION

Water—The increase in wafer size, the need for higher water purity, and the increase in process steps indicate a potential trend for higher water usage per wafer. This trend can be reversed by a combination of strategies including development of higher efficiency rinse processes; recycling of higher quality water for process applications; and reuse of lower quality water for nonprocess applications.

Water used in semiconductor manufacture is mostly ultrapure water (UPW). Since UPW manufacturing requires large quantities of chemicals, the increase in UPW consumption and quality has accelerated chemical consumption (and the cost of ultrapure water manufacturing). Reduction of UPW consumption and manufacturing will result in reduced environmental effects caused by the chemicals and reduced manufacturing costs. In areas where water is sufficient, wastewater recycling should be implemented after reviewing the local water reuse and associated recycling costs.

To successfully operate future water systems with recycle and reuse capabilities, reliable and fast response sensors are needed for online monitoring of key contaminants. System simulation tools and advanced control strategies are needed to design and operate the future UPW plants as well as the future water distribution and wastewater collection systems. New high efficiency water purification methods are needed to reduce energy and chemical usage. New factories designed with the idea of matching the water purity supplied with the purity required are critical; this will reduce the waste and minimize the environmental impact of water usage.

Energy—Limits on sources of energy could potentially limit industry's ability to expand existing factories or build new ones. While the semiconductor manufacturers have demonstrated improved energy efficiencies over the past decade, potential resource limitations require the industry to continue the trend.

ESH DESIGN AND MEASUREMENT METHODS

One important element of measurement and evaluation methods is risk assessment. As an example, the results of chemical industry investigations can be applied to the semiconductor industry with appropriate modification. A standardized methodology to identify, access, and accept risk is needed.

A methodology to determine the lowest ESH impact of materials and processes needs to be developed. Measurement and evaluation methods must be easy to use and reliable. Their meaning lessens if their content is not updated in response to new semiconductor technologies and other technical developments. A design algorithm to conduct environmentally-conscious design during the device/process design stage is needed.

Process analysis is another evaluation element. Process by-products, for example from plasma processes, are an important issue. The elementary chemical reactions in each process must be understood, and new

measurement and evaluation methods must be implemented for developing processes that have the lowest ESH impact. For material balance, it may be advantageous to apply the results of pollutant release and transfer disclosure (PRTR) programs.

Database establishment—A database is necessary to store the information for accurately conducting risk assessment on the materials and chemicals used. The database should contain information such as safety data, environmental load/impact data, process data, emission distribution factor (dispersion model) and emission treatment methods to use the material, and conditions regulated by law. At present, the general database for chemical materials is generated by the chemical material industry, but the data are not sufficient, especially on the process used or the distribution factor (dispersion model) of the chemical material to the environment.

Water—Process simulation and cost optimization tools are required to determine the optimum balance of high efficiency rinse processes; recycling of higher quality water process applications; and reuse of lower quality water for nonprocess applications at different factories and different locations.

Table 69a Chemicals, Materials and Equipment Management Technology Requirements—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
ESH								
Chemical risk assessment	**Algorithm**						**Application**	*New processes*
Data accumulation								
Existing chemicals	**Design of data base**			**50%**			**100%**	
New chemicals	**Design of data base**						**After 2 years of market intro**	*New processes*
Assessment of new chemicals: safety data and environmental load/impact	**Evaluation terms and method**			**Evaluation system**			**Data accumulation**	
Reduction of environmental load/impact materials								
Existing materials	**Lead-free process and structure**							
	Bromine-, Antimony-free fire-resistant plastics, Beryllium-free							
	Assessment of other materials			**Substitution process and disposal treatments**				
By-product materials				**Process evaluation**			**Substitution process and disposal treatments**	
Material LCA				**Algorithm**			**Operation**	
Environmental management								
Material balance	**Algorithm**			**Pollutant release, and transfer disclosure (PRTR)**			**Automatic PRTR data acquisition system**	
Disposal management	**System design**						**Operation**	
Equipment standards	**Identify gaps in existing standards**		**Implement comprehensive foundation of international standards**					
ESH impact of spares and consumables	**Analysis of impact**			**Do testing and generate specifications**				

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 69a Chemicals, Materials and Equipment Management Technology Requirements—Near Term (continued)

YEAR / TECHNOLOGY NODE	1999 / 180 nm	2000	2001	2002 / 130 nm	2003	2004	2005 / 100 nm	DRIVER
Interconnect								
Low κ materials – spin on and CVD		Lowest ESH impact solvents/ CVD precursors			Emissions models/ESH benign processes			*Speed, signal loss*
Copper processes	Extend plating bath life		Lowest ESH impact plating chemistries		Plating bath recycle/ESH benign CVD processes			*Speed, reliability*
Advanced metallization			Lowest ESH impact processes/ emissions characterization			Improved chemical utilization		*Perform, cost, SoC*
Planarization	Reduce slurry required			Slurry recycling/ESH benign chemistries				*Planarity*
Plasma processes			Lowest ESH impact etch chemistries					*Etch/clean*
Front end Processes								
High κ	ESH evaluation for high κ		Lowest ESH impact high κ materials		ESH benign processes			
	Low-hazard precursor materials		Low-hazard deposition methods		ESH benign processes			
			High κ materials without potentially toxic/bioaccumulative metals (Pb, Ni)		Lowest hazard metal compounds			
Doping processes	Subatmospheric hydride and halogenated gas delivery systems	Subatmospheric delivery for additional dopants			Lowest hazard dopant materials			
Surface preparation	Fundamental research on surface/interface science		Ongoing research and integration of solutions		Optimized surface preparation processes			
	Alternate wafer rinse methods		Incorporation into new rinse/clean tools					
	Alternate clean methods (O_3, super-critical etc., research)		*In situ* chemical generation		Chemical optimization of high κ cleans			
	Elimination of sulfuric acid							
Front end etch	Characterize plasma by-products		Plasma process simulation-optimize processes for by-product destruction					
Lithography								
Introduction and integration of new equipment into manufacturing								*Reduced feature size*
Optical		Hazardous chemicals, material compatibility						
e-Beam		Ionizing radiation, ergonomics, chemical consumption, disposal						
EUV		Non-ionizing radiation, ergonomics, chemical consumption, disposal						
Specification and integration of new chemicals and materials introduced into manufacturing: Optical, e-Beam, and EUV		New chemicals, purification requirements, wastes, emissions						*Reduced feature size*

Solutions Exist   *Solutions Being Pursued*   *No Known Solutions*

Table 69b Chemicals, Materials, and Equipment Management Technology Requirements—Long Term

YEAR TECHNOLOGY NODE	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*	DRIVER
ESH				
Data accumulation				
New chemicals	After 1 year of market intro			*New processes*
Material LCA	Revision			
Interconnect				
Low κ materials	Zero waste deposition/soluble precursors			*Speed, signal loss*
Copper/advanced metallization	Zero waste deposition			*Speed*
Planarization	Non-chemical consuming processes			*Planarity*
Optical interconnect	Lowest ESH impact materials & processes			*Speed*
Front End Processes				
High κ dielectrics	ESH benign materials and deposition processes			
Doping	Self-cleaning dopant tools (*in situ* clean)			
	ESH benign materials and processes			
Surface preparation	Ambient temperature cleans			
		"No-clean" processes		
Front end etch	ESH – benign process, including high κ etch methodologies			
Lithography				
Introduction and integration of new equipment into manufacturing				*Reduced feature size*
Optical	Hazardous chemical, material compatibility			
e-Beam and EUV	Ionizing radiation, ergonomics, chemical consumption, disposal			
Innovative options	Ionizing/non-ionizing radiation, ergonomics, chemical consumption, disposal			
Specification and integration of new chemicals and materials introduced into manufacturing				*Reduced feature size*
Optical	New chemicals, purification requirements, wastes, emissions			
e-Beam, EUV, and innovative options	New chemicals, purification requirements, wastes, emissions			

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 70a Climate Change Mitigation Technology Requirements—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
ESH								
Energy consumption: overall fab equipment $kWh/cm^2(kWh/in^2)$	0.5 (3.2)–0.7 (4.5)						0.4 (2.6)–0.5 (3.2)	
Energy consumption: fab facility $kWh/cm^2(kWh/in^2)$	0.5 (3.2)–0.7 (4.5)						0.4 (2.6)–0.5 (3.2)	
300 mm production fab equipment energy consumption	X*				0.5X			Productivity
Reduce PFC emissions	[Note 1]							
Front End Processes								
Reduce PFC emissions (etch)	Develop optimized etch processes, alternate chemistries, and cost effective abatement							
				Continued research in alternate etch chemistries				
Lithography								
Equipment energy and material consumption								*Reduced feature size*
e-Beam		Emission of climate change gases, energy consumption						
Specification and integration of new chemicals and materials introduced into manufacturing								*Reduced feature size*
e-Beam		Use of climate change gases, air emissions, wastes						
Assembly & Packaging								
Reduce energy use	X	0.8X						

** X is based on 200 mm tool energy per wafer requirement.*

[Note 1] 10% or greater absolute reduction from 1995 baseline by 2010 is agreed to by the World Semiconductor Council.

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 70b Climate Change Mitigation Technology Requirements—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
ESH				
Energy consumption: overall fab equipment kWh/cm^2(kWh/in^2)	0.4 (2.6)–0.5 (3.2)	0.3 (1.9)–0.4 (2.6)		
Energy consumption: fab facility kWh/cm^2(kWh/in^2)	0.4 (2.6)–0.5 (3.2)	0.3 (1.9)–0.4 (2.6)		
300 mm production fab equipment energy consumption	0.4X			*Productivity*
Reduce PFC emissions	Note 1			
Lithography				
Equipment energy and material consumption				*Reduced feature size*
e-Beam	Emission of climate change gases, energy consumption			
Innovative options	Emission of climate change gases, energy consumption			
Specification and integration of new chemicals and materials introduced into manufacturing				*Reduced feature size*
e-Beam	Use of climate change gases, air emissions, wastes			
Innovative options	Use of climate change gases, air emissions, wastes			
Assembly & Packaging				
Reduce energy use	0.5X			

** X is based on 200 mm tool energy per wafer requirement.*

[Note 1] 10% or greater absolute reduction from 1995 baseline by 2010 is agreed to by the World Semiconductor Council.

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Table 71a Workplace Protection Technology Requirements—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
ESH								
Equipment safety, gases and chemicals leak, and equipment stability during an earthquake	Implement S2 Safety Guidelines and S8 Ergonomic/ Human Factor Guidelines [50, 51]							
Safe interface of Automated Material Handling Systems (AMHS) and manufacturing equipment	Standardized control features and procedures							
Comprehensive exposure data	Comprehensive industrial hygiene (IH) exposure data For operations and maintenance							
MSDS data sheets	Industry standardized format		Use format					
Personal protection equipment (PPE)				Test and rate PPE against chemicals used				
PPE trade-off versus hazard elimination or engineering control			Cost of PPE per employee per shift					
Protocol for selecting risk management solutions	Industry acceptance		Full implementation					
Reduced chemical exposure	Isolate workers from chemicals and by-products during operation and maintenance							
Ergonomic improvement	Understand physiological stresses		Minimize/eliminate physiological stresses					
New chemical qualification	Collaboration of government/academia/industry/company resources							
X-ray exposure	Fundamental research required							
Endocrine disrupters in mold resin	Develop new materials							
N-methyl-2-pyrrolidone (NMP) exposure					Phase out			
Interconnect								
Copper plating processes		Tools w/reduced employee exposure						
Front End Processes								
Less flammable wet deck materials	Develop new materials							
Work environment	Continued reduction of physical stressors in clean room environment – noise, non-ionizing radiation, thermal stress							
High κ		Lowest hazard materials and precursors						
Doping	Low pressure dopants	Reduced potential for exposure during maintenance				Low hazard dopants		
Surface preparation	Robotics safety		Reduced chemical use in clean processes		Inert material cleans (supercritical, cryogenic)			
Front end etch	Minimize potential exposure to plasma etch by-products		Optimize processes to minimize production of potentially hazardous by-products					

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[50] SEMI. S2-93A – *Safety Guidelines for Semiconductor Manufacturing Equipment.*

[51] SEMI. S8-95 – *Safety Guidelines for Ergonomics / Human Factors Engineering of Semiconductor Equipment.*

Table 71a Workplace Protection Technology Requirements—Near Term (continued)

YEAR *TECHNOLOGY NODE*	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*	*DRIVER*
Lithography								
Health and safety								*Reduced feature size*
Optical		**Ergonomics issues, potential exposure to hazardous chemicals**						
e-Beam		**Ergonomics issues, hazardous chemicals, potential exposure to ionizing radiation**						
EUV		**Ergonomics issues, potential exposure to hazardous chemicals, potential exposure to non-ionizing radiation**						
Specification and integration of new chemicals and materials introduced into manufacturing								*Reduced feature size*
Optical		**Potential exposure to toxic chemicals**						
e-Beam and EUV		**Hazardous chemical use**						

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 71b Workplace Protection Technology Requirements—Long Term

YEAR *TECHNOLOGY NODE*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*	*DRIVER*
ESH				
Comprehensive exposure data	Industry database of IH exposure data			
New chemical qualification	Apply new methods			
X-ray exposure	Collaboration of government/ academia/ company resources	Apply new methods		
Endocrine disrupters in mold resin	Use new materials			
NMP exposure	Complete elimination			
Interconnect				
Optical interconnect	Tools with no employee exposure			
Front End Processes				
Less flammable wet deck materials	Use new materials			
High κ	ESH-benign dielectrics, electrode materials and deposition processes			
Doping	Low hazard dopants			
Surface preparation	Novel rinse/clean methods that reduce water and chemical usage			
Starting materials	Ergonomic design of tools and wafer handling for >300 mm wafers			
Front end etch	*In situ* equipment clean processes			
Lithography				
Health and safety				*Reduced feature size*
Optical and e-beam	Potential exposure to hazardous chemicals			
EUV	Potential exposure to non-ionizing radiation			
Innovative options	Potential exposure to ionizing/non-ionizing radiation			
Specification and integration of new chemicals and materials introduced into manufacturing				*Reduced feature size*
Optical, e-beam, and EUV	Potential exposure to toxic chemicals			
Innovative options	Potential exposure to toxic chemicals			

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 72a Resource Conservation Technology Requirements—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
ESH								
Zero emissions	Thorough recycle/reuse system						Develop recycling technology	
Recycle rate: %	60%			65%			70%	
Interconnect								
Copper processes		Minimize rinsewater						
Planarization	Reduce water consumption			Water recycle				
Plasma processing		Measure/ optimize energy use		Reduce tool/system energy requirements				
Front End Processes								
High κ			Energy-efficient deposition processes			Precise uniform thermal processes with minimal energy consumption		
Doping		Energy-use evaluation for future doping technologies such as PGILD			Energy efficient processes			
Surface preparation	Energy use quantification for surface preparation methodologies		Energy efficient clean process with heated chemistries and UPW					
	Water conservation through rinse optimization; idle flow reduction		Incorporation of novel rinse methodologies in wet tools			Novel water reduction techniques derived from surface/interface science		
Front end etch	Measure/ optimize energy use		More energy efficient plasma processes					
Starting Materials		Quantitation of energy/water reduction from simplified SOI-based process flows						
Lithography								
Optimization of resource consumption by equipment: optical, e-beam, and EUV		Equipment energy consumption, equipment related chemicals/ gases/materials						*Reduced feature size*
Optimization of resource usage: optical, e-beam, and EUV		Water/waste recycle/reuse/reduction						*Reduced feature size*
Factory Integration								
Decrease net feed water use Liters/cm^2 (gal/ in^2)	7.6 (13)	7.6 (13)	5.9 (10)	5.9 (10)	3.5 (6)	3.5 (6)	2.9 (5)	
Decrease UPW use Liters/cm^2 (gal/ in^2)	6 (10.2)–8 (13.6)			5 (8.5)–7 (11.9)			4 (6.8)–6 (10.2)	
Assembly & Packaging								
Eliminate waste from molding process	Develop/use new molding technologies							
Reduce water use	X	0.8X						
Reduce chemical use and consumption	X	0.8X						

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 72b Resource Conservation Technology Requirements—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
ESH				
Zero emissions (recycle rate: %)	80%	90%		
Front End Processes				
Surface preparation	Ambient temp. processes	Virtual closed loop water systems		
Lithography				
Optimization of resource consumption by equipment: optical, e-beam, and EUV	Equipment energy consumption, equipment related chemicals/gases/materials			*Reduced feature size*
Innovative options	Equipment energy consumption, equipment related chemicals/gases/materials			
Optimization of resource usage: optical, e-beam, and EUV	Water/waste recycle/reuse/ reduction			*Reduced feature size*
Innovative options	Water/waste recycle/reuse/reduction			
Factory Integration				
Decrease net feed water use Liters/cm^2 (gal/in^2)	1.2 (2)			
Decrease UPW use Liters/ cm^2 (gal/ in^2)	3 (5.1)–5 (8.5)			
Assembly & Packaging				
Reduce/eliminate waste from molding process	Develop/use alternative molding materials			
Reduce water usage	0.5X			
Reduce chemical use and consumption	0.5X			

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 73a ESH Design & Measurement Methods Technology Requirements—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
ESH								
Methodology for determining lowest ESH impact of materials and processes	**Develop basic approach**			**Beta test the approach**			**Integrate approach into industry**	
Material balance	**Basic study**			**System performance check by existing data**			**Implement**	
Risk assessment	**Standardized methodology to identify, access, and accept risk**							
Case study for cost and relative risk model	**Case study**							
Relative risk model with cost performance				**Modeling**			**Check and improvement**	
Default values for risk and cost model				**Interim version**			**Improve accuracy**	
Design tool integration				**Basic study of integration for different values**			**Study for integration**	
Resource cycle system model	**Basic approach**			**Modeling**			**Check and improvement**	
Process simulation model				**Establish basic methodology**			**Develop advanced process methods**	
Evaluation of major process				**Use of simulation model on a major process**			**Use on advanced processes**	
Data base for chemicals and materials				**Software development**				
Data base for regulatory requirements				**Survey on requirements, guidelines, NGO trends, and others**				
Lithography								
Equipment design tools—optical, e-beam, and EUV		**Risk assessment/performance/ cost of ownership**						*Reduced feature size*
Chemical usage design tools—optical, e-beam, and EUV		**Risk assessment/performance/ cost of ownership**						*Reduced feature size*
Factory Integration								
Improved factory design and equipment integration for ESH	**Training for factory designers**				**Implement**			
	Industry strategy to develop and write codes							
	Consensus designs for chemical delivery and by-product management			**Implement**				
	Consensus design for equipment factory interface							

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 73b ESH Design & Measurement Methods Technology Requirements—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
ESH				
Design tool integration	**Integration**			
Evaluation methodology for resource cycle system model	**Performance and predictability check**			
Process simulation model	**Develop advanced process methods**			
Evaluation of major process	**Use on advanced processes**			
Lithography				
Equipment design tools				*Reduced feature size*
Innovative options	**Risk assessment/performance/cost of ownership**			
Chemical usage design tools				*Reduced feature size*
Innovative options	**Risk assessment/performance/cost of ownership**			

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

INTERCONNECT

The interconnect area poses several unique environment, safety, and health (ESH) challenges. Because of the new processes being developed to meet the technology demands, the industry is evaluating new materials in the area of advanced metallization, low κ, high κ, CMP, and optical interconnect. The ESH impacts of these new materials, processes, and subsequent reaction by-products must be determined as early as possible, ideally in the university and early supplier research stages, to ensure that the ESH information is available to the users. This will allow selection of optimal process materials based on both function and lowest ESH impact with respect to reaction product emissions, health and safety properties, materials compatibility with both equipment and other chemical components, flammability and reactivity. This will minimize the unnecessary business impact after processes are developed and in production. The short term technology requirements for Chemicals, Materials, and Equipment Management (Table 69a) include the development of the lowest impact materials and processes for all areas of interconnect. This includes solvents and polymers for spin-on processes, CVD precursors, planarization chemistries, and etch chemistries. It also calls for reduced chemical requirements and reduced waste in these areas, which may be achieved by increasing chemical utilization efficiency in CVD processes; extending bath life or recycling in copper plating; and decreasing slurry requirements or recycling slurry in CMP. The long term technology requirements (Table 69b) include zero-waste deposition processes for both dielectrics and metals and non-chemical consuming processes for planarization.

Global warming has been identified as one of the possible phenomena of climate change. Perfluorocompounds (PFCs), one type of high global warming potential chemicals, are used almost exclusively in interconnect. Both the short and long term technology requirements for Climate Change Mitigation (Table 70) are for a 10% absolute reduction of PFC emissions from the 1995 baseline, the goal established internationally by the semiconductor industry. To achieve this aggressive goal and to ensure that these chemicals remain available for industry use, the industry must strive to reduce emissions of PFCs compounds via process optimization, alternative chemistries, recycle, and/or abatement. The development of new materials results in the implementation of new etch chemistries; the lowest ESH impact etch processes should be developed that do not emit high global warming potential by-products. This concept also applies to CVD chamber cleaning.

The increased requirement for CMP will result in interconnect becoming a major user by volume of both chemicals and water. As indicated in the short term technology requirements for Resource Conservation (Table 72a), efforts must be made to develop the lowest ESH impact CMP and post-CMP clean chemistries while reducing overall water requirements. Rinse water minimization in copper electroplating and post-

CMP cleaning is necessary. Water recycle and reclaim for CMP and post CMP cleans is also a potential solution for water use reduction. With increased focus on energy conservation, the power requirements of plasma processing and CMP tools and related infrastructure must be minimized. RF generators are energy-intensive. Coupled with the process chemistry efficiencies (30–70% dissociation of F ions), plasma processes are not energy-efficient. Some installed base tools can be monitored and optimized for reduction in electricity consumption especially in the idle stages or better end point detectors for chamber cleaning. Waste heat from the plasma systems could be recovered for reuse. Future generation tools would require R&D in low-energy consuming plasma systems. Etchers and CVD tools use point-of-use (POU) chillers and heat exchangers to maintain wafer and chamber temperatures in a vacuum. More efficient heating and cooling control systems could help decrease energy use. New research is needed for improved heat transfer in vacuum systems.

The short term technology requirements for Workplace Protection (Table 71a) call for the development of tools with reduced employee exposure. This applies to the development of new copper plating tools as well as tools that may be developed for optical interconnect in the long term.

FRONT END PROCESSING

Key ESH concerns for Front End Processes center on development of new materials for gate dielectrics and electrodes; natural resources use (especially water); management of potential physical and chemical hazards to ensure worker protection; and optimization of processes to reduce chemical use and generation of wastes requiring abatement. New materials for 100 nm technologies and beyond (and corresponding precursors, clean techniques and etch gases) will require thorough ESH review.

The global EHS challenges affect all areas of Front End Processes. The primary chemical management strategy should be to optimize processes to maximize chemical use efficiency, including consideration of chemical throughput, waste generation, recovery of hazardous materials, and tool utilization factors. On-demand/*in situ* chemical generation can contribute to improved efficiency. Energy needs (tool and facility systems) must be evaluated for new technologies. Worker protection measures should address potential physical (such as thermal, non-ionizing radiation, laser and robotics hazards) as well as chemical hazards, especially during equipment maintenance. Factory planning should identify ergonomic design criteria for wafer handling (especially for 300–450 mm wafers), tools, and factory layout. EHS Cost-of-Ownership (CoO) and risk assessment tools should be utilized to evaluate process improvements and identify potential risks of new materials.

In addition, key ESH issues apply to specific areas of Front End Processes:

Surface preparation—ESH concerns for surface preparation focus on new clean techniques, chemical use efficiency, and consumption of water and energy. Surface preparation methods will undergo fundamental changes to accommodate new materials after the 2005 timeframe for expected adoption of new gate dielectrics and electrodes. There is a need for improved understanding of surface and interface science with the potential for significant reductions in chemical or water use.

Chemical use optimization should be applied to conventional and alternate clean processes. Among the areas being addressed by FEP are post etch via and metal cleans—solvent free dry cleaning; copper cleaning (including post CMP clean)—wet cleans and dry cleans; polymer/residue removal nitride strip by gas phase etching and cleaning; and metal and particle performance-simplified chemical sequences; dilute chemistries; and use of chelating agents. Several alternate clean processes have potential for significant chemical use reduction (cryogenic, supercritical fluids, dilute chemistries, sonic solvent cleans, simplified process flows, O_3 cleans, alternate BEOL cleans, cleans for copper and new low κ materials). Fluid flow optimization and sensor-based process control should be evaluated. Potential increased use of anhydrous gases (HF/HCl and alternatives) should be reviewed through process hazards analysis.

Sustainable, optimized water use strategies utilizing improved UPW production efficiency, reduced tool consumption, and efficient rinsing are being developed. However, the energy-use impact of alternate clean methods (such as cryogenic wafer and parts cleaning and hot-UPW wafer cleaning) or UPW production methods (such as continuous electrolytic ion-exchange) needs to be considered. Alternative solvent-based cleans need development. Development of reliable sensors to speciate low-level organics is needed to mitigate the process risk of UPW recycling. The optimization of test wafer usage can reduce chemical, water,

and energy consumption. Wet-tool designs should continue to incorporate enclosed processes, ergonomic principles, and robotics safety.

Starting materials—Current materials are primarily Czochralski (CZ) polished silicon wafers with epitaxial (Epi) silicon. Silicon-on-insulator (SOI) materials expected in conjunction with the 130 nm node may offer ESH advantages of fewer process steps—less chemicals and less energy than other materials. Larger wafers from 300–450 mm will require more chemicals, energy, and water although industry initiatives have been advanced to hold usage flat.

Thermal/thin films—The evaluation of alternative higher-κ materials must include thorough assessment of potential process hazards associated with both the materials and associated deposition processes. Alternate silicides (such as Co, Ni, others) present potential hazards requiring mitigation through engineering controls and appropriate personal protective equipment. Chemical use efficiency can be optimized through improved delivery systems and tool designs (such as small batch furnaces, single-wafer tools). Energy use, for diffusion and implant tools and associated facility systems (exhaust) should be evaluated and optimized.

A wide variety of organic ligands (potentially including halogens) are proposed as high κ precursors. The resulting metallorganic compounds may pose potential toxicity or flammability hazards. There is work on termanires like BST (barium strontium titanate, $BaSrTiO_3$), and $PbLaTiO_3$. More complex dielectrics include ZrSnTiO compositions, SrBiTaO compositions, PbZrTiO compositions and other ferro, piezo compounds. Anneals are probably necessary, utilizing N_2, FNO_2, O_2, NH_3, H_2 (forming gas).

Various metals and sources (gas phase, solution and solid) are being considered for gate electrodes. Gate metals will range from doped-polysilicon to metals (Ta, Ti, Nb, Al, Mo, Zr, V, Co W, Ru, Rh, Ni, Re, Ir, Pt) and various silicides and nitrides. Most CVD precursors will be organometallics, but they may be dissolved in a matrix solution with stabilizers, and carrier liquid that will be injected as a liquid.

Doping—The potential physical and chemical hazards of alternate technologies (a variety of new techniques are being considered) need to be evaluated and mitigated. Process hazards analysis tools will assist in managing hydrides (SiH_4, B_2H_6, PH_3, SbH_3, AsH_3, possibly others), metal alkyls and laser sources. Sub-atmospheric delivery stems should be developed for a wider variety of dopant materials.

Front end plasma etch—Continued use of PFCs will necessitate near-term process optimization/increased gas utilization (conversion efficiency within the process). Over the longer term, alternative chemistries for PFCs that do not emit PFCs as by-products need to be developed. Changes in gate dielectric materials will drive corollary changes in etch chemistries, necessitating review of potential ESH impacts. High κ materials will require an anisotropic selective etch over doped Si. The chemistry for these etches have not been determined but most likely a Cl-based chemistry will be used.

LITHOGRAPHY

From the perspective of ESH, lithography is represented by four subject areas. These are lithography and mask manufacturing chemicals (photoresists, thinners, developers, rinses, and strippers); processing equipment (spinners, vapor-phase deposition systems, and silylation ovens); exposure equipment (DUV, E-beam, X-ray, and ion beam); and equipment cleaning. Of critical concern with respect to these areas and the implementation of new lithography technologies is the avoidance of showstopper problems. In particular, issues such as new process chemicals evaluation, compliance with environmental regulations, equipment safety, and worker protection must be considered before changes are made.

Photolithography and mask manufacture chemicals—The first critical need in this category is the need for information related to properties and availability of new chemicals used in photolithography and mask manufacture. Among the information required are chemical toxicity, risk assessment data, status under TSCA, ability to monitor potential exposures, process emissions (HAPs and VOCs) including etch, strip, etc. The second critical need is for better materials management. This would include integration of new materials into patterning, maintaining performance and cost while, at the same time, promoting recycling and minimum use.

Potential solutions for these critical needs include preparation of a list of acceptable lithography chemicals based on evaluation of TSCA conformance, development of analytical protocols that enable monitoring of

new chemicals, robust chemical selection criteria, risk assessment, and the use of pollution prevention principles. Additional potential solutions include alternate materials and chemistries, life cycle analysis of new materials and chemistries, use of additive technologies, and use of benign materials.

Processing equipment—Critical needs for processing equipment include understanding potential exposure to toxic materials, emission of HAPs and VOCs, hazardous waste disposal, cost of ownership, and energy consumption. Additional needs are ergonomic design of equipment, controlling emissions from PFC usage, and plasma byproducts. Lastly, there is a need to minimize waste, for example, waste resulting from spin-on processes and assorted "wet" processes.

Among the potential solutions are effective point-of-use abatement, optimization of tool exhaust, use of pollution prevention and DFESH principles, and supplier use of S2 and S8 standards. Further potential solutions include deployment of zero impact processes, elimination of the need for materials with significant global warming potentials, and utilization of DFESH tools in design for manufacture of new equipment.

Exposure equipment—Critical needs with respect to new exposure equipment include understanding toxicity of required chemicals, control of potential exposure to radiation, risk assessment, cost-of-ownership, hazardous energies, and beam shielding.

Potential Solutions include performing risk assessments, analysis of cost-of-ownership and establishing radiation protection programs as necessary.

Equipment cleaning—Critical needs relate to understanding solvent usage, emission of HAPs and VOCs, hazardous waste disposal, and required personal protective equipment. It will also be important to understand the proper selection of cleaners and cleaning methodologies.

Potential solutions include cryogenic cleaning, solvent-free cleaning, dry resist technology, point-of-use abatement, pollution prevention, and optimization of tool design. Additionally, redesign of processes and equipment to achieve minimal environmental impact will be required.

FACTORY INTEGRATION

Responsible safety, health, and environmental performance for the SC industry begins with factory pre-design (training and planning), design and construction. Standardization of safety and environmental systems, apparatus, procedures, and methodologies when applicable, will prove to be an efficient and cost effective approach. Sharing of these practices can reduce start up schedules and will result in greater cooperation by equipment suppliers for interfacing their products into factories. Factory design, manufacturing equipment, the interface between these elements and their interaction with the people who work in this environment strongly influence ESH performance for the industry.

Early comprehension of safe and environmentally responsible design coupled with an understanding of code and regulatory requirements is essential for designers to develop factories that meet ESH expectations, reduce start up schedules and avoid costly retrofits and changes.

Accepted protocol and order of selection for risk management are hazard elimination, design controls (isolation or engineering design), administrative controls (procedural), and personal protective equipment.

One opportunity for greater standardization exists with manufacturing and assembly/test equipment. Standardization in ESH aspects of equipment design, design verification, ESH qualification and signoff will greatly improve ESH performance, start up efficiency, and cost. Additionally, standardization of ESH practices in equipment maintenance, modification, migration, decommissioning, and final disposition will also reap substantial performance improvements in ESH and cost over the life of equipment and factories.

Standardization of building safety systems and interface to tools will improve safety and also increase efficiency of installations and reduce start-up times. This would include but is not limited to fire detection and suppression systems and their monitoring interface, gas detection systems, electrical and chemical isolation devices, emergency shut off systems, and safety related alarms. These include building systems as well as those that are integral to manufacturing and assembly/test equipment.

Additionally, the careful selection of process and maintenance chemicals addressed in other sections of this roadmap should be complemented by designs that serve to isolate personnel from equipment and product during operation and maintenance of equipment and systems.

The safety issues associated with factory processing support systems must also be aggressively improved in future factories. As more is known about potential impacts of the work environment on health and safety, worker protection improvements must be incorporated into factory systems. Improved risk assessment methodologies and their consistent utilization during the design phase will enhance this effort.

A thorough understanding of the potential safety risks associated with automated equipment will drive development of standards that assure safe working conditions for both people and product. These standards and guidelines must be directed at the integrity of the automated systems, the tools with which they interface, and the interface as well.

The industry faces increasing permit, code, and emissions limitations. Planning for future factories and modifications to existing factories should involve cooperative efforts with code entities and government bodies to ensure that advancements in technology of tools and factories are comprehended and utilized in new regulations and amendments. These actions must be driven on a global level. The SC industry should move to establish basic ESH specifications that apply to all equipment and factory practices that are recognized around the world.

Factory design defines the systems that deliver process materials to tools, manage by-products, and control work place environments. Future factory design must employ balanced programs, resource conservation, reduction, and management. These conservation and reduction programs are driven by increasing competition for limited water and energy resources, pollution concerns, and industry consumption.

ESH standardization and design improvements for factories and equipment can be greatly enhanced through training programs established for and by the industry. Technology now allows for computer based training (CBT) programs to be developed to address all of the design and procedural challenges noted in this section.

While much of the responsibility for reduction in use of limited resources and waste minimization rests with the tool suppliers and process technologists, application of advanced resource management programs to factory systems will have a significant impact. The goal of these future programs is to build factories that minimize resource consumption and reuse, recycle, or reclaim by-products to produce near-zero effluent factories. Key factory-related ESH programs require water reuse in process and non-process applications, energy efficient facilities equipment, improved facilities system design, and new facilities operating strategies.

ASSEMBLY & PACKAGING

The drive towards flip-chip and chip-scale packaging will change the ESH needs for assembly and packaging eventually completely, as these technologies eliminate the application of leadframes, conventional molding and substrates.

However, the application of environmentally hazardous materials, such as lead, chromium, beryllium, antimony and brominated flame retardants is under increasing international regulatory pressure. Restrictions on the use of these materials are expected by the year 2004 for products on the European market.

Lead (Pb) gets special attention as the alternative soldering processes will cause numerous problems in the electronics industry, where the current process is widely used and integrated in equipment assembly lines. *Alternatives may cause a technology problem, as the soldering temperature of semiconductors has to be increased, leading to reduction of lifetime and quality.*

For power devices, an additional complication is the use of a lead-containing alloy to attach the chip to the leadframe.

The energy consumption needs to be reduced because of the need to reduce the emissions of global warming gasses, as well as from a resource point of view.

The needs for assembly and packaging are not tied to the nodes of the wafer production, but to the requirements and technologies of our customers. However, to maintain the roadmap format, the same tables have been used.

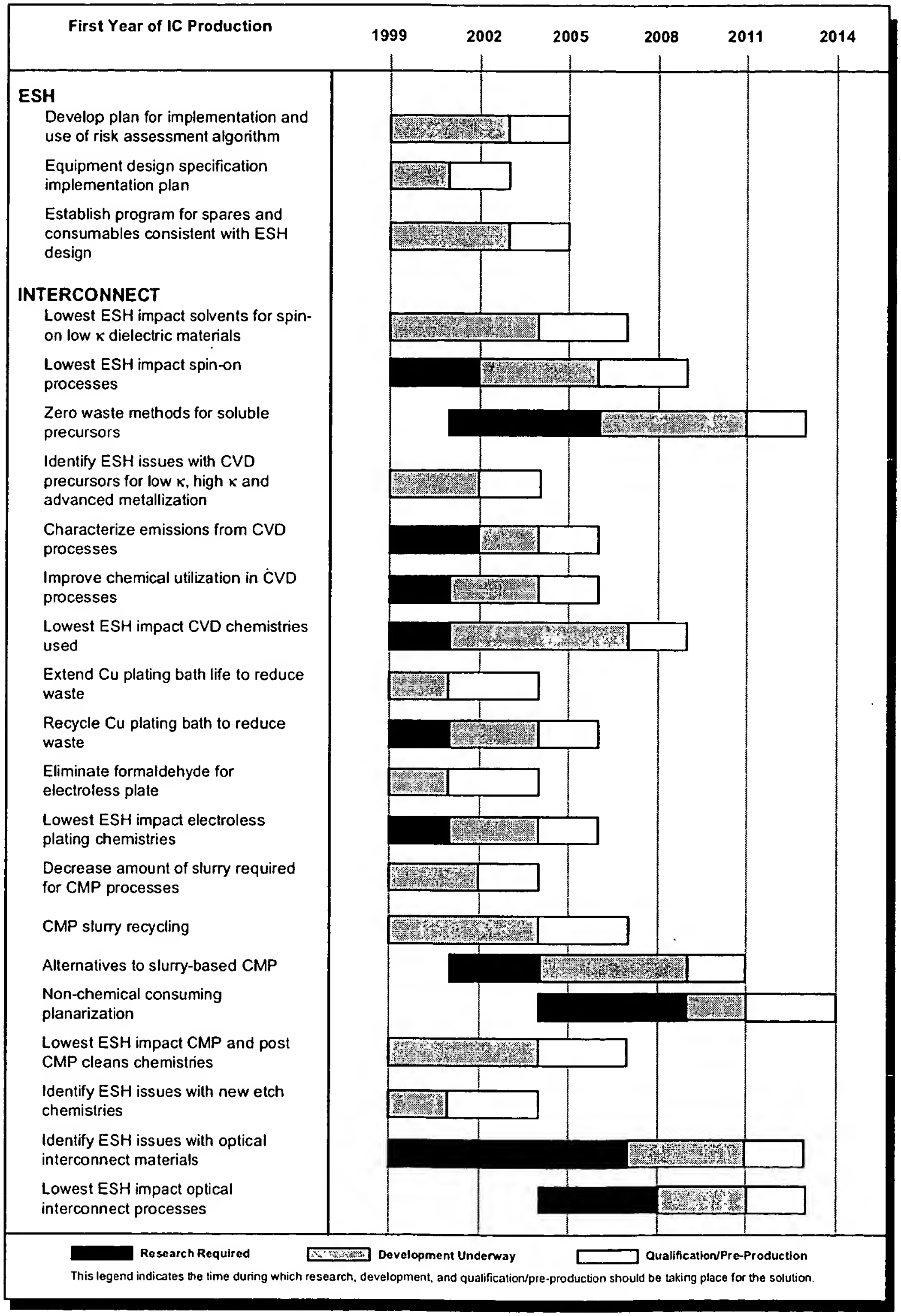

Figure 49 Potential Solutions for ESH: Chemicals, Materials, and Equipment

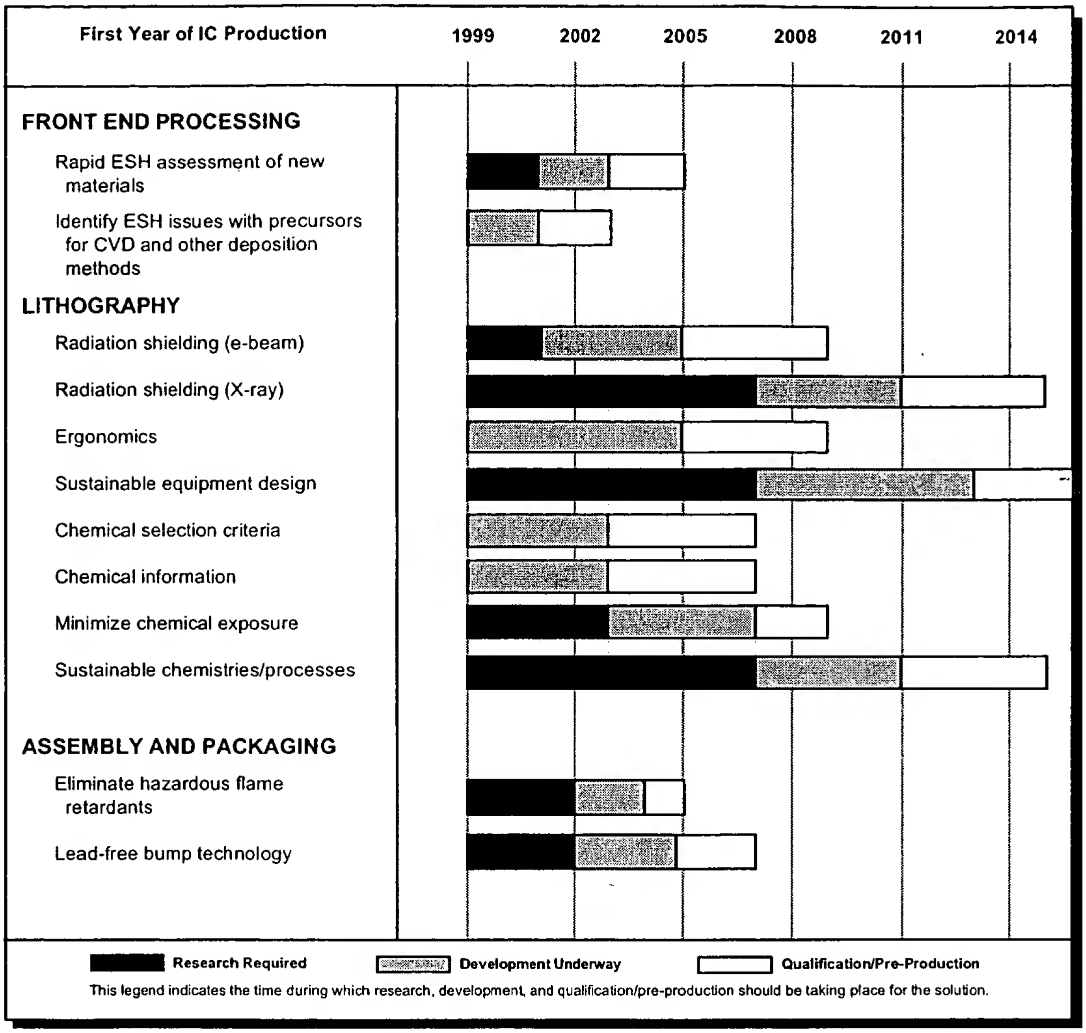

Figure 49 Potential Solutions for ESH: Chemicals, Materials, and Equipment (continued)

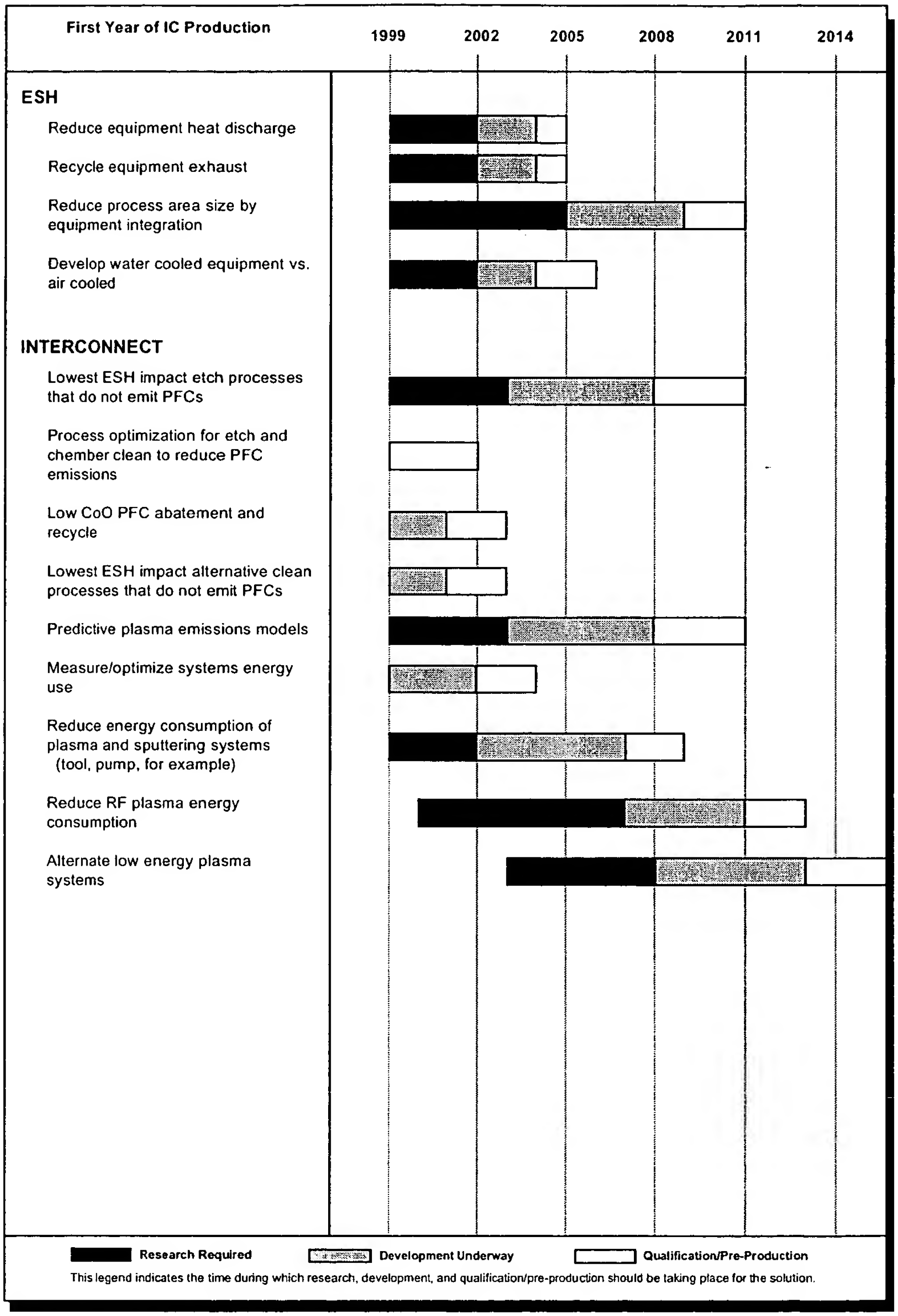

Figure 50 Potential Solutions for ESH: Climate Change Mitigation

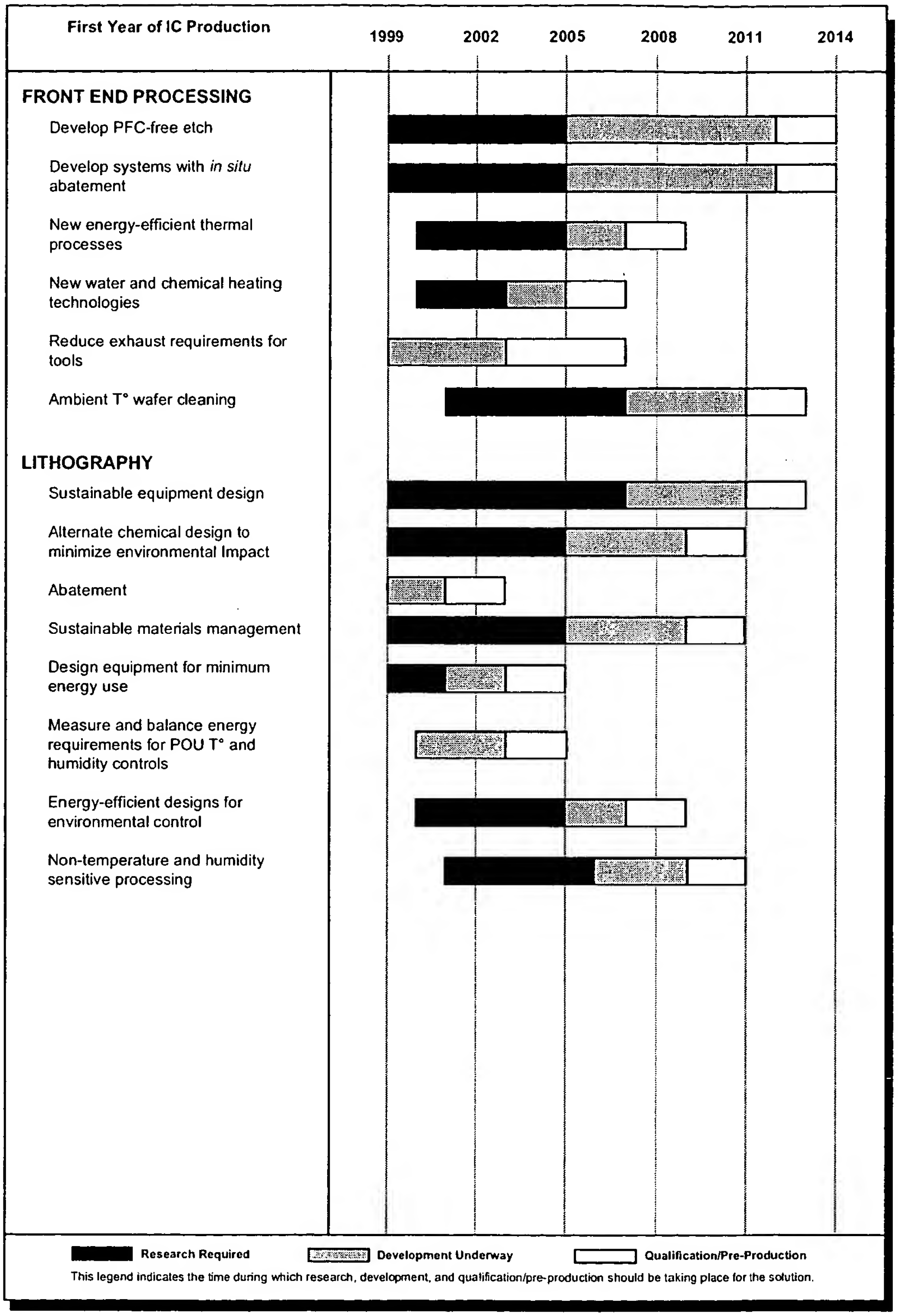

Figure 50 Potential Solutions for ESH: Climate Change Mitigation (continued)

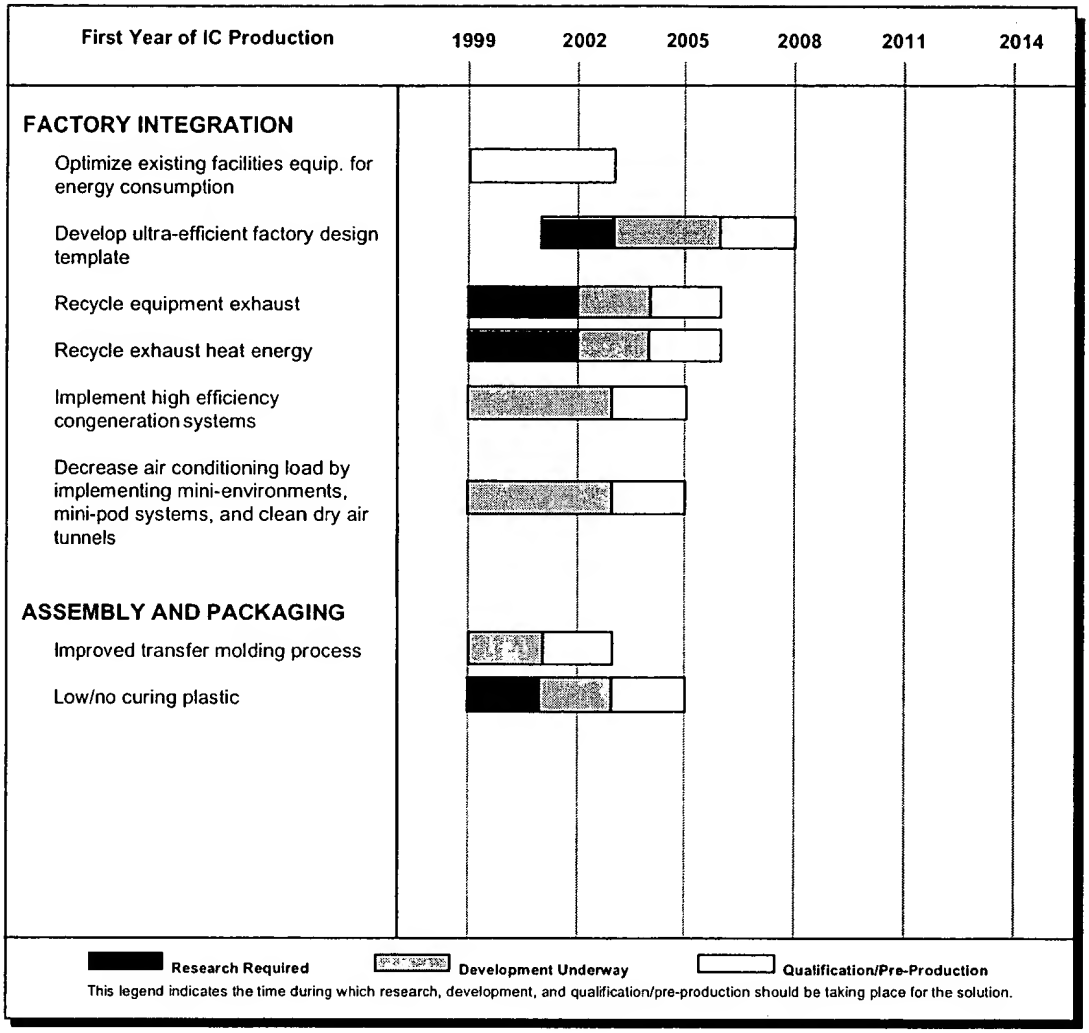

Figure 50 Potential Solutions for ESH: Climate Change Mitigation (continued)

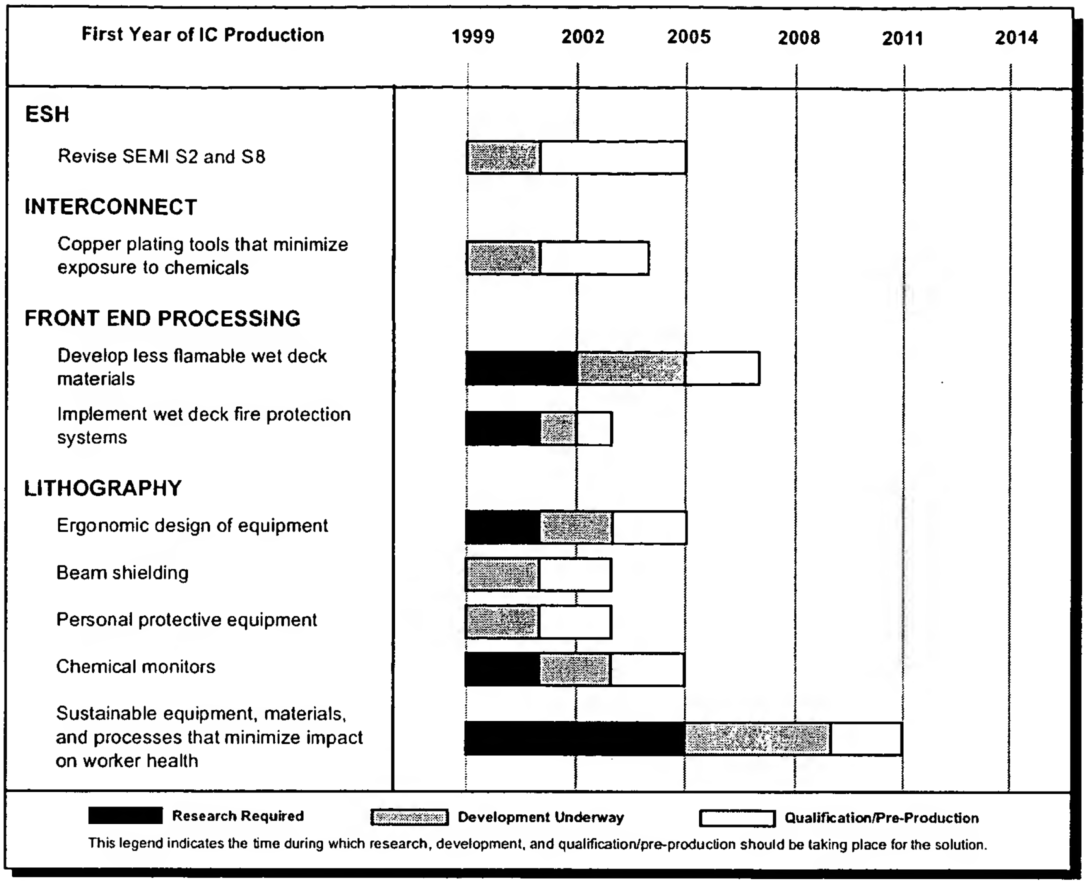

Figure 51 Potential Solutions for ESH: Workplace Protection

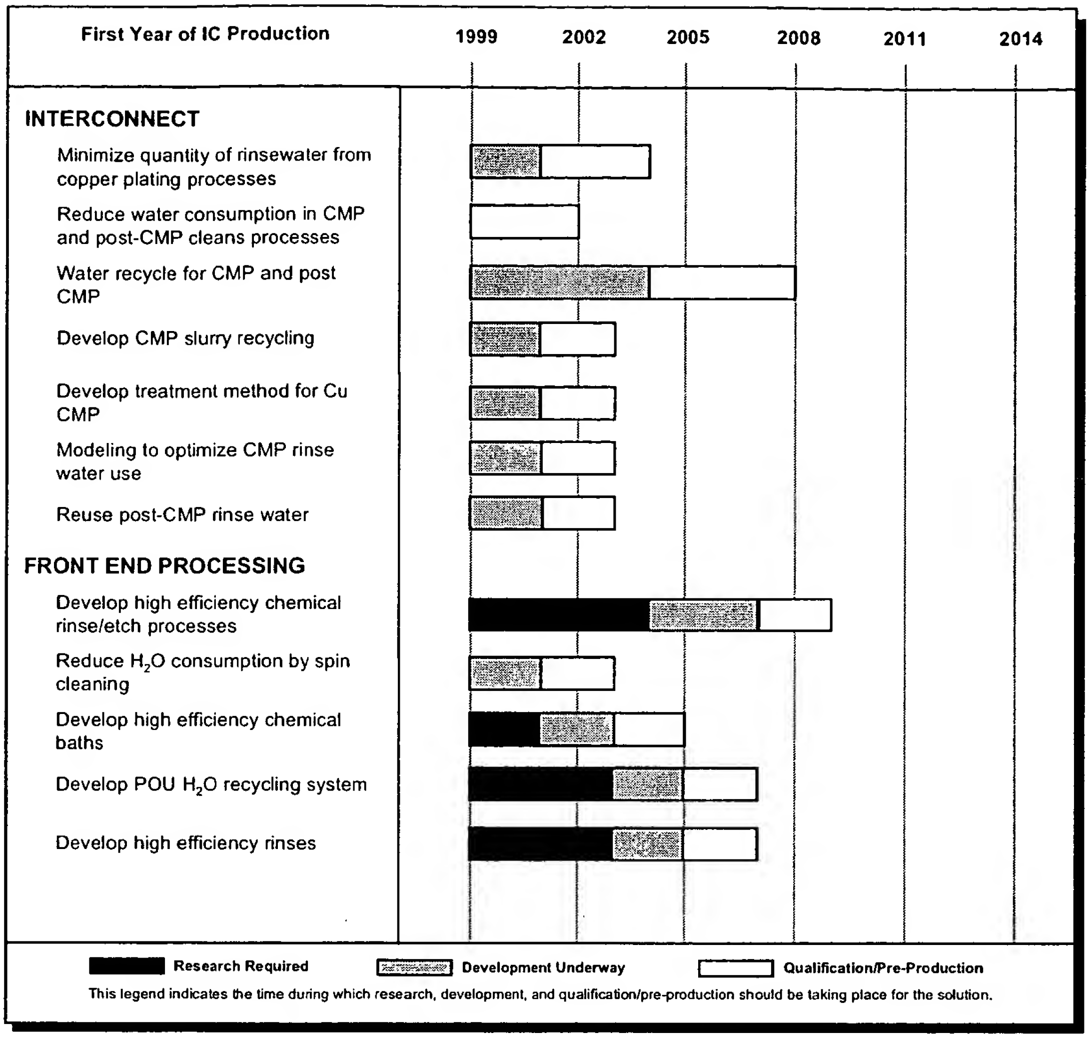

Figure 52 Potential Solutions for ESH: Resource Conservation

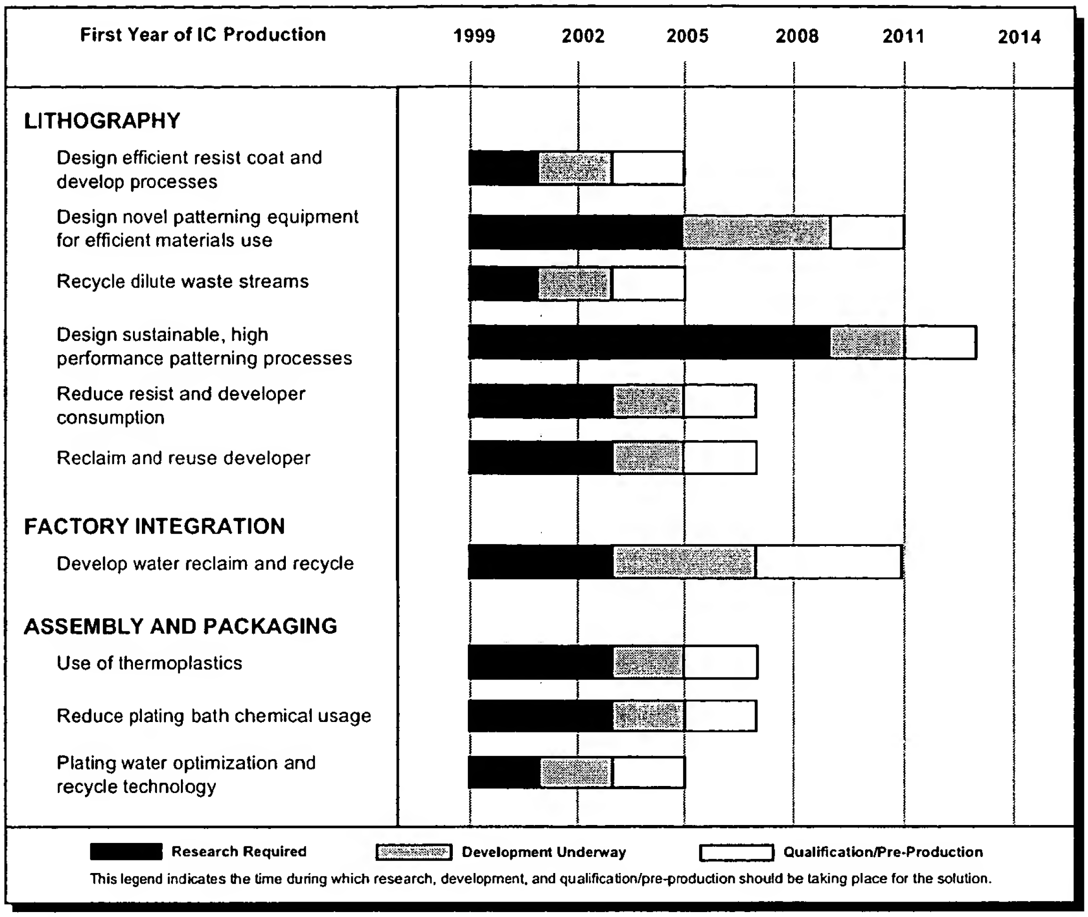

Figure 52 Potential Solutions for ESH: Resource Conservation (continued)

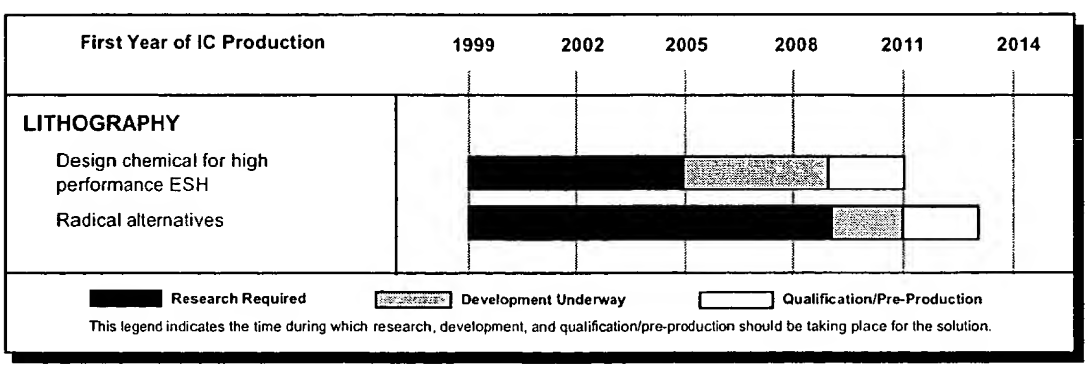

Figure 53 Potential Solutions for ESH: ESH Design and Measurement Methods

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

1999 EDITION

DEFECT REDUCTION

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DEFECT REDUCTION

SCOPE

Defect Reduction addresses the entire yield learning process. As such, the Defect Reduction chapter is partitioned into four focus topics; *Yield Model and Defect Budget, Defect Detection, Defect Sources and Mechanisms,* and *Defect Prevention and Elimination.* These topics correspond with the learning cycle typical of yield engineering and defect reduction. Key business metrics rely on the success of rapid yield improvement and the associated competencies of defect allocation, formation, transport, deposition, detection, characterization, reduction, and elimination. These competencies crosscut all process technologies, as well as the facility infrastructure, device design, and process integration. Key messages include the importance of continued development and availability of defect detection, review, and classification technologies where much greater sensitivity and throughput is necessary. Reduction of process/equipment generated defects is paramount to meet defect targets for 85%–95% yield in mature products. Likewise, significant efforts will be necessary to baseline, reduce and control yield loss associated with systematic mechanisms. Order of magnitude improvements in process critical fluid impurity levels are not believed to be necessary well into the sub-100 nm regime. Defect to fault transformations, kill ratios, and isolation techniques are also believed to be critical challenges as physical device dimensions and corresponding defect dimensions continue to shrink. Automated, intelligent analysis and reduction algorithms, which correlate facility, design, process, test and WIP data will have to be developed to enable integrated yield management.

DIFFICULT CHALLENGES

The difficult challenges for defect reduction technologies are summarized in Table 74. Defect budgets will require frequent revalidation and updates, as information about future processing technologies becomes available. Yield models need to better consider complex integration issues with respect to random-defect limited yield as well as systematic limited yield impacts (such as parametric yield loss, circuit-limited yield, etc) for future technology nodes. Future defect models must consider electrical characterization information, with reduced emphasis on visual inspections and analysis. Detecting defects associated with high aspect ratio contacts, and combinations of canals and vias in dual-damascene structures will continue to be difficult defect detection challenges. More specifically, the detection of defects buried deep within one such structure on a process layer that may have up to 10 billion similar structures will continue to be the grand challenge in this area. The challenge is complicated by the need for both high sensitivity and high throughput-a tradeoff typically accepted today for optimization of tool performance for either baseline yield learning or production line monitoring. Fault isolation complexity is expected to grow exponentially and represent an extremely difficult task of defining both horizontal plane and vertical layer fault location dimensions. Analyzing circuit failures that leave no detectable physical remnant present an extremely difficult task. Statistical means of accurately dealing with near zero defect adder data that frequently exhibit high coefficients of variation is a fundamental data reduction challenge. Through the use of advanced test structures and modeling techniques, the fundamental challenge in the area of process critical materials is to understand the correlation between impurity concentration and device yield, reliability, and performance. This correlation will determine whether increasingly stringent contamination limits are truly required and to provide early warning of needs for tighter specifications. Process tools must have capability to automatically self-monitor production for yield excursions, failures, and faults, and to initiate corrective actions.

Table 74 Defect Reduction Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥ 100 nm / BEFORE 2005	SUMMARY OF ISSUES
Yield Models—Random, systematic, parametric, and memory redundancy models must be developed and validated to correlate process induced defects, equipment generated particles and product/process measurements to yield	Correlated process-induced defects (PID), particles per wafer per pass (PWP), product inspections, and *in situ* measurements Sampling and statistical issues with ultra-small populations Impact of within-wafer variations on yield predictions Development of parametric yield loss models
High Aspect Ratio Inspection—High-speed, cost-effective tools must be developed that rapidly detect defects associated with high-aspect ratio contacts/ vias/trenches, and especially defects near/at the bottom of these features.	Poor transmission of energy into bottom of via and back out to detection system Large number of contacts and vias per wafer
Trace Impurity Specifications—Test structures and advanced modeling are needed to determine the effect of trace impurities on device performance, reliability and yield.	The need to better understand the impact of trace impurities is expected to become more important as new materials and processes are introduced.
Defect Sourcing—Automated, intelligent analysis and reduction algorithms that correlate facility, design, process, test and WIP data must be developed to enable rapid root cause analysis of yield limiting conditions.	Circuit complexity grows exponentially and the ability to rapidly isolate failures on non-arrayed chips is needed. Automated data reduction algorithms must be developed to source defects from multiple data sources (facility, design, process and test.)
Nonvisual Defects—Failure analysis tools and techniques are needed to enable localization of defects where no visual defect is detected.	Many defects that cause electrical faults are not detectable inline.
FIVE DIFFICULT CHALLENGES < 100 nm / BEYOND 2005	
Yield Models—Defect "budgeting" must comprehend greater parametric sensitivities, complex integration issues, greater transistor packing, ultra-thin film integrity, etc.	Development of test structures for new technology nodes Modeling complex integration issues Ultra-thin film integrity modeling Better methods of scaling front end process complexity that considers increased transistor packing density
Defect Detection—Detection and simultaneous differentiation of multiple killer defect types is necessary at high capture rates and throughputs	Existing techniques tradeoff throughput for sensitivity, but at predicted defect levels, both throughput and sensitivity are necessary for statistical validity. Ability to detect particles at critical size may not exist
Escalating Inspection Costs—Equipment must effectively utilize realtime process and contamination control through integrated *in situ* process and product metrology	Equipment must effectively utilize real time process and contamination control through *in situ* sensors. Inspection must occur during yield ramp and by exception only in a production environment.
Defect Characterization—Defect data must include size, shape, composition, location all independent of "background," for accelerated yield learning	Defect characteristic data will be necessary to enable continued yield learning. Inline defect detection data must include size, shape, composition, and so on., all independent of location and topology. Test structures will have to be developed that emulate design to process and process integration issues.
Defect Free Intelligent Equipment—Advanced modeling (chemistry/contamination), materials technology, software and sensors are required to provide robust, defect-free process tools that predict failures/faults and automatically initiate corrective actions prior to defect formation.	Advanced modeling (chemistry/contamination), materials technology, software and sensors are required to provide robust, defect-free process tools that predict failures/faults and automatically initiate corrective actions prior to defect formation Development of advanced low defect surface preparation techniques

TECHNOLOGY REQUIREMENTS

YIELD MODEL AND DEFECT BUDGET

$$Y = Y_S * Y_R = Y_S * \left(\frac{1}{1 + \frac{AD_0}{\alpha}} \right)^{\alpha}$$

The overall die yield of a IC process can broadly be described as the product of systematic (or gross) limited yield (Y_S) and random-defect limited yield (Y_R). The defect budget technology requirements defined in Tables 76 and 77 are based on the negative binomial yield model where Y_R is the random-defect limited yield, A is the critical area of a device, D_0 is the defect density and α is the cluster factor. Assumptions made in calculating the defect budget

technology requirements in this revision are indicated in Table 75. Requirements for the 1999 180 nm technology node use the results of a 1999 study of current process-induced defect (PID) levels at SEMATECH member companies. The PID budget technology requirements were extrapolated from a median PID value scaled to a 150 nm groundrule process for MPUs and DRAMs respectively for a set of generic process tools that represent an entire process flow.

$$PID_n = PID_{n-1} \times \frac{F_n}{F_{n-1}\left(\frac{S_{n-1}}{S_n}\right)^2}$$

The extrapolation takes into consideration increase in chip size, increase in complexity, and shrinking feature size. The extrapolation uses the equation where PID is the process-induced defect density per square meter, F is the average faults per mask level (as determined by the random electrical fault density (D_0) divided by number of masks at a given technology node), S is the minimum critical defect size, and n refers to the technology node. The PID extrapolation equation was used to calculate PID budget values both forward and backward in technology node from a 150 nm ground rule process. All PID budget values are defined with respect to a 75 nm critical defect size. Each entry in the PID section of Tables 76 and 77 refers to a generic tool type used in a process flow. Since future actual tools and processes are not known, this roadmap assumes that no new process, material, or tool will be acceptable with a larger PID budget than prior methods. This assumption needs periodic validation. This defect budgeting method tends to be a worst case model since all process steps are assumed to be at minimum device geometry. In actuality, many processes allow process zones with more relaxed geometries. However, the same tools are used for both minimum and relaxed geometries. Thus, a worst case defect budgeting model is prudent. Table 75 states the yield, chip area, and product maturity assumptions that were used in calculating electrical fault density values and PID defect budget values for MPUs and DRAMs respectively. These assumptions for the most part are as defined in the ORTC. Table 76 presents the random PID budget targets necessary to meet the stated assumptions for a cost-performance MPU as defined in the ORTC Table 1a. This MPU is assumed to have a small L1 cache, but the device consists primarily of logic transistor functionality. With respect to MPUs, this analysis assumes that the process/design improvement target factor (ORTC Table 1b) in each technology node is met. If not, then MPU random PID budgets would need to be reduced by an additional ~6% per year. Similarly, Table 77 presents the random PID budget targets necessary to meet the yield assumptions stated in Table 75 for DRAMs. The random fault density that is used to calculate faults per mask level (which is used as input to the PID extrapolation equation) is based on only the periphery (logic/decoder) area of the DRAM chip. This is projected in the ORTC to be 30% of chip area at the stated product maturity. Since there is no redundancy in the periphery, this portion of the chip must consistently achieve the 89.5% random-defect limited yield. It is assumed that the core (array) area of the DRAM can implement redundancy to attain the overall yield target of 85%.

Table 75 Defect Budget Technology Requirement Assumptions

Product	*MPU*	*DRAM*
Yield Ramp Phase	*RAMP PHASE END*	*PRODUCTION PHASE END*
$Y_{OVERALL}$	**75%**	**85%**
Y_{RANDOM}	**83%**	**89.5%**
$Y_{SYSTEMATIC}$	**90%**	**95%**
Cluster Parameter	**5**	**5**
Chip Size	**170 mm² through 2002, then increasing**	**132 mm² in 1999, then increasing**

Table 76 *Yield Model and Defect Budget MPU Technology Requirements*

YEAR TECHNOLOGY NODE	1999 140 nm	2000	2001 100 nm	2002	2003	2004 70 nm	2005	2008 50 nm*	2011 35 nm*	2014 25 nm*
MPU										
MPU / ASIC ½ pitch [A]	230	210	180	160	145	130	115	81	58	41
Critical defect size	115	105	90	80	73	65	58	41	29	21
Chip size [B]	170	170	170	191	214	224	235	269	308	354
Overall electrical D_0 (faults/m^2) at critical defect size or greater [C]	1742	1742	1742	1550	1384	1322	1260	1101	961	836
Random D_0 × (faults/m^2) [D]	373	373	373	332	296	283	270	235	206	179
# Mask levels [E]	23	23	23	24	24	24	25	27	28	29
Random faults/mask	16	16	16	14	12	12	11	9	7	6
MPU Random Process Induced Defect (PID) budget (defects/m^2) for generic tool type scaled to 75 nm critical defect size or greater										
CMP clean	293	244	179	121	89	68	49	20	8	4
CMP insulator	421	351	258	174	128	98	70	28	12	5
CMP metal	307	256	188	127	93	71	51	20	9	4
Coat/develop/bake	118	99	72	49	36	27	20	8	3	1
CVD insulator	542	452	332	224	164	126	90	36	16	7
CVD oxide mask	503	419	308	208	152	117	84	34	15	6
Dielectric track	157	131	96	65	48	37	26	11	5	2
Furnace CVD	561	468	344	232	170	130	93	37	16	7
Furnace fast ramp	196	164	120	81	59	46	33	13	6	2
Furnace oxide/anneal	269	224	165	111	81	62	45	18	8	3
Implant high current	462	385	283	191	140	107	77	31	13	6
Implant low/mid current	403	336	247	166	122	94	67	27	12	5
Inspect PLY	165	138	101	68	50	38	28	11	5	2
Inspect visual	187	156	115	77	57	43	31	12	5	2
Lithography cell	183	152	112	75	55	42	30	12	5	2
Lithography stepper	87	73	53	36	26	20	15	6	3	1
Measure CD	181	151	111	75	55	42	30	12	5	2
Measure film	202	168	124	83	61	47	34	13	6	2
Measure overlay	165	138	101	68	50	38	28	11	5	2
Metal CVD	263	219	161	109	80	61	44	18	8	3
Metal electroplate	157	131	96	65	48	37	26	11	5	2
Metal etch	611	509	374	252	185	142	102	41	18	7
Metal PVD	392	326	240	162	118	91	65	26	11	5
Plasma etch	576	481	353	238	174	134	96	38	17	7
Plasma strip	401	334	245	165	121	93	67	27	12	5
RTP CVD	171	143	105	71	52	40	28	11	5	2
RTP oxide/anneal	118	99	72	49	36	27	20	8	3	1
Test	64	54	39	27	19	15	11	4	2	1
Vapor phase clean	428	357	262	177	130	100	71	29	12	5
Wafer handling	25	21	15	10	8	6	4	2	1	0.3
Wet bench	446	371	273	184	135	104	74	30	13	5

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

* *The MPU 50 / 35 / 25 nm technology nodes are shown to actually occur in 2007, 2010 and 2013 respectively in ORTC table 1b.*

[A] As defined in the ORTC Table 1a

[B] As defined in the ORTC Table 2a

[C] As defined in the ORTC Table 5a

[D] Based on assumption of 83% Random Defect Limited Yield (RDLY)

[E] As defined in the ORTC Table 5a

Table 77 Yield Model and Defect Budget DRAM Technology Requirements

YEAR TECHNOLOGY NODE	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
DRAM										
DRAM ½ pitch [A]	**180**	**165**	**150**	**130**	**120**	**110**	**100**	**71**	**50**	**35**
Critical defect size	**90**	**83**	**75**	**65**	**60**	**55**	**50**	**35**	**25**	**18**
Chip size [B]	**132**	**138**	**145**	**152**	**159**	**166**	**174**	**199**	**229**	**262**
Overall electrical D_0 (faults/m^2) at critical defect size or greater [C]	**1249**	**1193**	**1140**	**1089**	**1040**	**994**	**950**	**828**	**723**	**630**
Random D_0 × (faults/m^2) [D]	**2826**	**2700**	**2580**	**2465**	**2355**	**2250**	**2150**	**1875**	**1636**	**1426**
# Mask levels	**20**	**20**	**20**	**21**	**21**	**21**	**22**	**24**	**25**	**26**
Random faults/mask	**141**	**135**	**129**	**117**	**112**	**107**	**98**	**78**	**65**	**55**
DRAM Random Process Induced Defect (PID) budget (defects/m^2) for generic tool type scaled to 75 nm critical defect size or greater										
CMP clean	**758**	**608**	**480**	**328**	**267**	**215**	**162**	**65**	**27**	**11**
CMP insulator	**1090**	**875**	**691**	**472**	**385**	**309**	**233**	**93**	**39**	**16**
CMP metal	**793**	**637**	**503**	**344**	**280**	**225**	**169**	**68**	**28**	**12**
Coat/develop/bake	**306**	**246**	**194**	**133**	**108**	**87**	**65**	**26**	**11**	**4**
CVD insulator	**1402**	**1126**	**889**	**608**	**495**	**397**	**299**	**120**	**50**	**21**
CVD oxide mask	**1301**	**1045**	**825**	**564**	**459**	**369**	**278**	**111**	**46**	**19**
Dielectric track	**407**	**327**	**258**	**176**	**144**	**115**	**87**	**35**	**15**	**6**
Furnace CVD	**1453**	**1166**	**921**	**629**	**512**	**411**	**310**	**124**	**52**	**21**
Furnace fast ramp	**508**	**408**	**322**	**220**	**179**	**144**	**108**	**43**	**18**	**7**
Furnace oxide/anneal	**695**	**558**	**441**	**301**	**245**	**197**	**148**	**59**	**25**	**10**
Implant high current	**1194**	**959**	**757**	**517**	**421**	**338**	**255**	**102**	**43**	**18**
Implant low/mid current	**1043**	**837**	**661**	**452**	**368**	**295**	**223**	**89**	**37**	**15**
Inspect PLY	**428**	**343**	**271**	**185**	**151**	**121**	**91**	**37**	**15**	**6**
Inspect visual	**484**	**389**	**307**	**210**	**171**	**137**	**103**	**41**	**17**	**7**
Lithography cell	**472**	**379**	**299**	**205**	**167**	**134**	**101**	**40**	**17**	**7**
Lithography stepper	**226**	**181**	**143**	**98**	**80**	**64**	**48**	**19**	**8**	**3**
Measure CD	**496**	**377**	**298**	**203**	**166**	**133**	**100**	**40**	**17**	**7**
Measure film	**523**	**420**	**331**	**227**	**184**	**148**	**112**	**45**	**19**	**8**
Measure overlay	**428**	**343**	**271**	**185**	**151**	**121**	**91**	**37**	**15**	**6**
Metal CVD	**680**	**546**	**431**	**295**	**240**	**193**	**145**	**58**	**24**	**10**
Metal electroplate	**407**	**327**	**258**	**176**	**144**	**115**	**87**	**35**	**15**	**6**
Metal etch	**1581**	**1269**	**1002**	**685**	**558**	**448**	**337**	**135**	**56**	**23**
Metal PVD	**1013**	**813**	**642**	**439**	**357**	**287**	**216**	**86**	**36**	**15**
Plasma etch	**1491**	**1197**	**945**	**646**	**526**	**422**	**318**	**127**	**53**	**22**
Plasma strip	**1037**	**832**	**657**	**449**	**366**	**294**	**221**	**88**	**37**	**15**
RTP CVD	**443**	**355**	**281**	**192**	**156**	**125**	**94**	**38**	**16**	**6**
RTP oxide/anneal	**306**	**246**	**194**	**133**	**108**	**87**	**65**	**26**	**11**	**4**
Test	**166**	**134**	**105**	**72**	**59**	**47**	**36**	**14**	**6**	**2**
Vapor phase clean	**1108**	**890**	**703**	**480**	**391**	**314**	**27**	**95**	**40**	**16**
Wafer handling	**65**	**52**	**41**	**28**	**23**	**19**	**14**	**6**	**2**	**1.0**
Wet bench	**1153**	**925**	**731**	**499**	**407**	**325**	**246**	**98**	**41**	**17**

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

[A] As defined in the ORTC Table 1a
[B] As defined in the ORTC Table 2a
[C] As defined in the ORTC Table 5a
[D] Based on assumption of 89.5% Random Defect Limited Yield (RDLY) and peripheral area = 30% of overall chip size

DEFECT DETECTION

The ability to detect inline yield-limiting defects on specific process layers is the primary requirement of a defect detection technology. The extension of this ability to the diverse throughput requirements of various phases of production—process research and development (PRD), yield ramp (YR), and volume production (VP)—broadens the applicability of the technology and creates extremely complex solutions that must be fast and sensitive. This is becoming more critical as fabs begin to run different products in multiple stages of process maturity through the same defect detection tools to extract maximum returns from extensive capital investment in such tools.

The respective capabilities must be ready for use by the chip manufacturers just-in-time for each phase of the process cycle. Tools that meet the requirements for PRD are typically required well in advance of the planned introduction of a technology generation. Tools that can accelerate YR must be available several months before production begins. Finally, the ability to monitor excursions at a technology node is needed when the product hits high yield levels.

Technology requirements are separated into unpatterned wafer inspection, patterned wafer inspection, and high aspect ratio inspection, as shown in Table 78. The effects of the buried patterning in post-chemical mechanical planarization (CMP) wafers makes their inspection more similar to patterned wafer inspection than unpatterned for the purposes of this roadmap. High aspect ratio inspection, defined as the detection of defects occurring deep within structures having depth to width ratios greater than 3, is treated separately from patterned wafer inspection due to special sensitivity requirements described in the *Difficult Challenges* section as well as note C under Table 78.

The technology requirements for defect detection on unpatterned wafers depend on the film and substrate. Detection of defects on the backside of wafers without introducing any contamination or physical contact on the front side is desirable. The wafer backside requirements are based on lithography depth-of-focus considerations as stipulated in Table 38.

Several other defect modes also need to be addressed by detection tools. A better understanding of non-visible killers (defects that cannot be detected with conventional optical technologies) is emerging with the increased usage of e-beam based technologies. Most of these defects tend to be sub-surface and possess a significant dimension in the longitudinal direction or z-axis. A clear definition is not yet available for the minimum size of such defects that must be detected. Macro defects that impact large areas of the wafer should not be overlooked because of the urgency to address the sub-micron detection sensitivities stipulated below. Scan speeds for macro inspection should be continuously improved to match the wafer throughput (plus overhead of the inspection) of the lithography systems at every technology node.

Semiconductor manufacturers balance the costs and benefits of automated inspection by inspecting with sufficient frequency to enable rapid yield learning and avoid substantial risk of yield loss. The price, fab space occupied, and the throughput of defect detection tools are major contributors to their cost-of-ownership (CoO). Currently, CoO forces many semiconductor manufacturers to deploy such tools in a sparse sampling mode. Statistically optimized sampling algorithms are needed to maximize the yield learning resulting from inspection tool usage. In order to maintain acceptable CoO in the future, the throughput as well as the sensitivity of these inspection tools must be increased. If future tools operate at increased sensitivity with decreased throughput, thereby increasing their CoO, semiconductor manufacturers will have to adopt even sparser sampling plans, thereby increasing their risk of yield loss and slowing their yield learning rates.

The requirements for sensitivity in Table 78 have been stipulated on the basis of detecting accurately sized Polystyrene Latex (PSL) spheres that are deposited on test and calibration wafers. However, new tools are mostly evaluated on their capability to detect real defects that occurred during process development that were captured using high-resolution microscopy. Such defects include particles, pattern flaws, and scratches. There is an urgent need for the development of a defect standard wafer that will enable objectively

evaluating new and existing defect detection tools to accommodate the growing palette of defect types on various layers.

Defects detected on future technology generation wafers will require higher resolution microscopes for review. Rapid developments in Scanning Electron Microscopy (SEM) have already enabled quick review and classification of such defects. Speeding up SEM review could provide the opportunity to gather information on more defects than currently possible, thereby increasing yield learning.

Table 78a Defect Detection Technology Requirements—Near Term.

YEAR TECHNOLOGY NODE	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*	DRIVER
*Patterned Wafer Inspection, PSL Spheres at 90% Capture, Equivalent Sensitivity (nm) *[A, B]*								
Process R&D at 300 (cm^2/hour)	54	49	44	39	36	33	30	*0.3×DR*
Yield ramp at 3,000 (cm^2/hour)	72	65	59	52	48	44	40	*0.4×DR*
Volume production at 10,000 (cm^2/hour)	90	81	73	65	60	55	50	*0.5×DR*
High Aspect Ratio Feature Inspection: Defects other than Residue, Equivalent Sensitivity in PSL Diameter(nm) at 90% Capture Rate. [C]								
All stages of manufacturing	54	49	44	39	36	33	30	*0.3×DR*
Unpatterned, PSL Spheres at 90% Capture, Equivalent Sensitivity (nm) [D, E]*								
Metal film	69	63	57	51	47	43	39	*0.3×MCP*
Nonmetal films	54	49	44	39	36	33	30	*0.3×DR*
Bare Silicon	54	49	44	39	36	33	30	*0.3×DR*
Wafer backside	180	163	150	130	120	110	100	*DR*
Defect Review								
Resolution (nm) [F]	9	9	8	7	7	6	5	*0.05×DR*
Coordinate accuracy (µm) at above resolution	3	3	2	2	2	1	1	*
Automatic Defect Classification on a Defect Review Platform [G, H]								
Redetection: minimum defect size (nm)	72	65	59	52	48	44	40	*0.4×DR*
Number of defect types	5	5	5	10	10	10	15	**
Speed (seconds/defect)	10	10	7	5	5	5	5	
Speed—w/elemental (seconds/defect)	25	25	20	15	15	13	10	

DR—Design Rule   * *Assume 0.67×1024×1024 pixels at stated resolution*

MCP—Minimum Contacted Pitch   ** *Trend to indicate coarse-fine classification*

Solutions Exist   *Solutions Being Pursued*   *No Known Solutions*

Notes for Table 78 for Defect Detection Requirements

[A] Patterned wafer scan speed is required to be at least 300 cm^2/hour for process R&D mode, 3,000 cm^2/hour for yield ramp mode, and at least 10,000 cm^2/hour for volume production mode. Existing solutions do not achieve these targets at the above mentioned sensitivity requirement.

[B] Patterned wafer nuisance defect rate shall be lower than 15% in process R&D phase, less than 10% in yield ramp phase, and less than 5% in volume production phase.

[C] HARI defects are already considered "killers" at any process stage. Hence, minimum defect sensitivity was stipulated as 0.3 × technology node at all stages of production. Physically uninterrupted coverage of the bottom of a contact by a monolayer of material or more should also be detected.

[D] Unpatterned wafer defect detection tools will be required to scan 150 (200 mm or equivalent) wafers per hour at nuisance defect rates lower than 5%.

[E] Metal films inspection tools must detect defects greater than half the minimum contacted pitch (Interconnect chapter, Tables 46 – 48) × 0.3 (process R&D requirement for patterned wafer defects) for nongrainy films and × 0.5 for rough or grainy films. Nonmetal films and bare Si detection sensitivity must be at least as good as that for patterned wafer inspection to justify monitor wafer usage.

[F] Resolution corresponds to 10% of patterned wafer detection sensitivity for volume production.

[G] ADC: Detectability, as % of defects redetected, should be greater than 95; Accuracy, as the % of defects correctly classified as per a human expert, should be greater than 95; Repeatability should be greater than 95%; and Reproducibility, as COV%, should be no greater than 5%.

[H] Assumptions: 5,000 wafer starts per month, defects per wafer based on surface preparation at FEOL, leading to defects per hour that need review, 100% ADC.

Table 78b Defect Detection Technology Requirements—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
*Patterned Wafer Inspection, Equivalent Sensitivity (nm) *[A, B]*				
Process R&D at 300 cm^2/hour	21	15	11	0.3×DR
Yield ramp at 3,000 cm^2/hour	28	20	14	0.4×DR
Volume production at 10,000 cm^2/hour	35	25	18	0.5×DR
High Aspect Ratio Feature Inspection. [C]				
All stages of manufacturing	21	15	11	0.3×DR
*Unpatterned, Equivalent Sensitivity (nm) * [D, E]*				
Metal film	29	21	14	0.3×MCP
Nonmetal films	21	15	11	0.3×DR
Bare Silicon	21	15	11	0.3×DR
Wafer backside	70	50	35	DR
Defect Review				
Resolution (nm) [F]	4	3	2	0.05×DR
Coordinate accuracy (μm) at above resolution	1	1	0.5	*
Automatic Defect Classification on a Defect Review Platform [G, H]				
Redetection: Minimum defect size (nm)	28	20	14	0.4×DR
Number of defect types	20	20	25	**
Speed (seconds/defect)	5	5	5	
Speed — w/elemental (seconds/defect)	10	10	10	

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

DEFECT SOURCES AND MECHANISMS

Rapid identification of yield detracting mechanisms through integrated yield management is the essence of defect sourcing and yield learning. Table 79 presents the technology requirements for defect sources and mechanisms. Learning must proceed at an accelerated rate to maintain current defect sourcing cycle time despite the growth in circuit complexity and the amount of data acquired on a given wafer lot. As integrated circuit fabrication processes continue to increase in complexity, it has been determined that data collection, retention, and retrieval rates increase exponentially. At future technology nodes, the time necessary to source manufacturing problems must at least remain constant, approximately 50% of the theoretical process cycle time on average during yield learning. In the face of this increased complexity, strategies and software methods for integrated yield management (IYM) have been identified as critical for maintaining productivity. IYM must comprehend integrated circuit design, visible and non-detectable defects, parametric data, and electrical test information to recognize process trends and excursions to facilitate the rapid identification of yield detracting mechanisms. Once identified, the IYM system must source the product issue back to the point of occurrence. The point of occurrence is defined to be a process tool, design, test, or process integration issue that resulted in the defect, parametric problem, or electrical fault. IYM will require a merging of the various data sources that are maintained throughout the fabrication environment. This confluence of data will be accomplished by merging the physical and virtual data from currently independent databases. The availability of multiple data sources and the evolution of automated analysis techniques such as automatic defect classification (ADC) and spatial signature analysis (SSA) can provide a mechanism to convert basic defect, parametric, and electrical test data into useful process information. The technology requirements for various types of defects are described below.

VISIBLE DEFECTS

Tools are needed to detect, review, analyze and source continuously shrinking visible defects.

NONDETECTABLE DEFECTS

Defects that cause electrical failure but do not leave behind a physical remnant that can be affordably detected with today's detection techniques are called non-detectable defects. As circuit design becomes more complex, more circuit failures will be caused by defects that leave no detectable physical remnant. Some of these failures will be systematic and parametric in nature, such as cross-wafer and cross-chip variations in resistance or capacitance; others will be random and non-parametric, such as stress caused dislocations and localized crystalline/bonding defects. The rapid sourcing of the latter (non-parametric, random, and non-detectable defects) will become increasing challenging. Techniques need to be developed that rapidly isolate failures and partitions them into those caused by visible defects, non-detectable defects, and parametric issues.

PARAMETRIC DEFECTS

As the design rules decrease, the impact on the systematic component of the yield (Ys) increases, and a major contributor to the Ys component is parametric variation within a wafer and wafer-to-wafer. Parametric defects have traditionally been referred to as "nondetectable defects," however, parametric defects require separation from the "nondetectable defects" for rapid sourcing.

ELECTRICAL FAULTS

As the number of steps, the number of transistors, and the circuit density increases, and the critical defect size decreases, an increasing number of defects are only seen as electrical faults. This includes faults caused by spot defects and faults caused by parametric process disturbances. In order to perform defect sourcing, the electrical fault must be isolated (localized) within the chip. The complexity of this task is roughly proportional to the number of transistors per unit area (mm^2) times the number of process steps, forming the defect sourcing complexity factor as shown in Table 79. In order to maintain the defect sourcing time, the time to isolate (localize) the electrical fault within the chip must not grow despite the increasing complexity.

DATA MANAGEMENT SYSTEMS

The current practice in data management system (DMS) technology is to maintain several independent databases that can be accessed by different engineering groups for yield analysis. This data is used for base-line analysis, excursion control, trend identification, process design, and yield prediction.

A fundamental impediment to efficient IYM is a lack of standards on which to base system communication, data formats, and a common software interface between data repositories. The creation of useable standards is also needed to facilitate automation methods. Current engineering analysis techniques are highly manual and exploratory by nature. The ability to automate the retrieval of data from a variety of database sources, such as based on statistical process control charts and other system cues, will be required to efficiently reduce these data sources to process-related information in a timely manner. To close the loop on defect sourcing capabilities, methods must be established for integrating workflow information (such as WIP data) with the DMS, especially in commercial DMS systems. This will be especially important when addressing issues of advanced process and tool control beyond simple tool shutdown, such as lot and wafer re-direction, tool prognostics and health assessment.

DMS systems today are limited in their ability to incorporate time-based data such as that generated from *in situ* process sensors, tool health, and tool log data. Methods for recording time-based data such that it can be correlated with lot and wafer-based data are needed.

Even though there is a wide variety of manufacturing data accessible through the DMS system today, yield prediction tools and methods continue to be limited to a small number of experts. The ability to provide these analysis techniques to a broader engineering group will result in the rapid prioritization of defect generating mechanisms and a faster engineering response to the most important of these issues.

Table 79a Defect Sources and Mechanisms Technology Requirements—Near Term

YEAR *TECHNOLOGY NODE*	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*
DRAM ½ PITCH (nm)	*180*			*130*			*100*
MPU GATE LENGTH (nm)	*140*		*100*			*70*	
WAFER SIZE (mm)	*300*	*300*	*300*	*300*	*300*	*300*	*300*
Sourcing Complexity [A], [F]							
Logic transistor density/mm^2 (1E4)	**7.0**	**9.9**	**14.0**	**17.6**	**22.2**	**30.0**	**40.6**
Number of processing steps	**380**	**—**	**—**	**430**	**—**	**—**	**480**
Defect sourcing complexity factor (1E6) [B]	**27**	**—**	**—**	**76**	**—**	**—**	**195**
Defect sourcing complexity trend [C]	**1**	**—**	**—**	**3**	**—**	**—**	**7**
Data Analysis for Rapid Sourcing							
Defect data volume (#data items/wafer) (1E12) [D]	**1.9**	**—**	**—**	**5.4**	**—**	**—**	**14**
Defect data volume (DV) trend [E]	**1**	**—**	**—**	**3**	**—**	**—**	**7**
Time required to recognize trends	**Days**	**—**	**—**	**Days**	**—**	**—**	**Hours**
Information sources for automatic data analysis	**Spatial**	**—**	**—**	**Spatial and time**	**—**	**—**	**Merge**
Transport Modeling							
Gas transport mechanism	**Transitional**	**Transitional**	**Transitional**	**Transitional**	**Transitional**	**Transitional**	**Transitional**
Deposition mechanism	**Assumed**	**Assumed**	**Assumed**	**Sticking coefficient**	**Sticking coefficient**	**Sticking coefficient**	**Sticking coefficient**
Time to solve for analysis	**Hours**	**Hours**	**Hours**	**Minutes**	**Minutes**	**Minutes**	**Minutes**

Table 79b Defect Sources and Mechanisms Technology Requirements—Long Term

YEAR *TECHNOLOGY NODE*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
DRAM ½ PITCH (nm)	*70*	*50*	*35*
MPU GATE LENGTH (nm)			
WAFER SIZE (mm)	*450*	*450*	*450*
Sourcing Complexity [A], [F]			
Logic transistor density/mm^2 (1E4)	**100**	**247**	**609**
Number of processing steps	**530**	**580**	**630**
Defect sourcing complexity factor (1E6) [B]	**530**	**1433**	**3837**
Defect sourcing complexity trend [C]	**20**	**53**	**142**
Data Analysis for Rapid Sourcing			
Defect data volume (#data items/wafer) (1E12) [D]	**84**	**230**	**610**
Defect data volume (DV) trend [E]	**44**	**121**	**321**
Time required to recognize trends	**Hours**	**Hours**	**Hours**
Information sources for automatic data analysis	**Improve**	**Improve**	**Improve**
Transport Modeling			
Gas transport mechanism	**Free molecular**	**Free molecular**	**Free molecular**
Deposition mechanism	**Mechanistic**	**Mechanistic**	**Mechanistic**
Time to solve for analysis	**Minutes**	**Minutes**	**Minutes**

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Notes for Table 79 for Defect Sources and Mechanisms Requirements

[A] Defect sourcing means identifying point of occurrence (identify process tool, design, test or process integration issue causing a visible or nondetectable defect, parametric problem or electrical fault).

[B] Defect sourcing complexity factor = (logic transistor density #/ mm^2)x (# processing steps)

[C] Defect sourcing complexity trend is normalized to 180 nm technology node.

[D] Defect data volume (DV) is the product of wafer area in mm^2 and defect sourcing complexity factor (#/mm^2).

[E] DV trend is normalized to 180 nm technology node.

[F] Rapid defect sourcing and yield learning assumptions:

- *Keep yield ramp constant at current benchmark level for successive technology nodes despite the increasing complexity and data volumes. This implies a need for increasingly sophisticated integrated yield management (IYM) tools.*
- *Keep time to source new yield detractors to ≤ 50% of theoretical cycle time.*
- *New material introduction should not increase defect sourcing time.*
- *Focus defect sourcing on ramp portion of yield learning curve.*
- *Data collection, retention and retrieval will go up exponentially and significant improvement will be required in the IYM tools to enable the above assumptions.*

DEFECT PREVENTION AND ELIMINATION

Defect prevention and elimination requirements are categorized by manufacturing materials or environment, as shown in Table 80.

Wafer environment control—There is now consensus that as device geometries approach 100 nm and beyond, wafer isolation will prove to be an enabling technology. The percentage of process steps affected by non-particulate or molecular contamination is expected to increase. The use of copper in the process introduces another potential contaminant. Because of these trends, the ability of wafer isolation technology to facilitate factory automation, integrated tool mini-environments and closed carriers (pods) is needed. The wafer environment control (WEC) technology requirements indicate target levels of ambient acids, bases, condensables, dopants, and metals for specific process steps. Other exposure times and sticking coefficients may be scaled linearly. The calculations do not account for localized differences in surface terminations, changes in the sticking coefficient over time, or chemical/kinetic interactions of analytes in the air or on the surface.

Process critical materials—Little understanding exists today regarding impurity specifications in novel materials such as sputter targets, Cu plating solutions, CMP slurries, chemical vapor deposition (CVD) precursors, and high/low κ materials and additional experimental investigation is required. Particle levels per volume have been held constant at critical particle size. Assuming an $1/x^3$ power law relationship, this means a cleanliness increase of approximately 2× per generation or ~80× from the 180 to the 35 nm technology node. Measurement of particles at the critical size is inferred, but monitoring of larger size particles is possible with requirements scaling according to the power law.

Ultrapure water (UPW) is generally considered to be >18.1 megΩ resistivity and below 1 PPB (except TOC) in ionics (cations and anions), organics, silica (dissolved and colloidal), particles, and bacteria. Table 80 shows needs as an extrapolation from the present. Lower criteria than present "state of the art," are not projected unless a process need is demonstrated according to each manufacturers requirements. Dissolved oxygen (DO) content needs to be controlled for rinsing of hydrogen passivated silicon due to the etching by oxygenated water and for control of gate oxide thickness. Tool operation and configuration impacts DO levels at the wafer, and N_2 environments may be required to control DO at the point of use (POU.) Until tools operate in N_2 environment, control of oxygen below 1 ppb is unlikely to prove practical.

Viable (cultured) bacteria typically are < 1 colony per liter due to the low levels of Total Organic Carbon (TOC) and DO within UPW production plants. UPW particle levels are currently well beyond available online particle metrology. Scanning Electron Microscopy (SEM) techniques are now in use that extend particle detection limit to approximately 0.05 µm, but this technique, while valuable for periodic quality checks, is not realtime.

Sensitivity to ionics (cations and anions) are process/product dependent. Levels of calcium and iron may be critical because they tend to precipitate on the wafer at lower levels.

MINIMIZING WATER CONSUMPTION

Due to the serious environmental impact of large demands on water sources and wastewater reception areas, (even if it is clean in some cases), conservation activities are mandatory. Ultrapure water must be recycled for use as wafer rinse water, reclaimed for other uses (like cooling towers, fume scrubbers, and irrigation), and minimized. The industry will require that recycled water be equal to or better than single-pass water. Refer to Figure 54.

PARAMETER	MEASURED	TEST METHOD
Resistivity	Online	Electric cell
Cultured bacteria	Incubation	Nutrients / heat
TOC	Online	Resistivity / CO_2
Reactive Silica	Online	Colormetric
Colloidal Silica	Lab	Dissolve in acid
Total Silica	Reactive + colloidal	Reactive + colloidal
Particle count	Online	Light scatter at ½ feature size
SEM filter	Lab	At ½ feature size
Cations / anions	Online	Ion chromatograph (process dependent)
Dissolved O_2	Online	Process variable (see text for details)
Non volatile residue	Online	—

Figure 54 General Test Methodology for Ultrapure Water

Liquid chemicals—For process chemicals, pre-diffusion cleaning requirements drive the most aggressive impurity levels. The purity levels of liquid chemicals are expected to remain unchanged from 2012 to the next technology node. The trend toward the use of more dilute chemistries helps to offset increased purity levels.

This evolution shows only a 10× improvement required over the next 15 years. Importantly, liquid particle counting technology is a very critical challenge below 90 nm. For HF last or SC-1 last cleans, use of novel chemistry (such as complexants, pH adjustments) may be required to meet the surface preparation requirements. With the increased use of CMP there must be a better understanding of purity requirements for slurries including the development of specifications for parameters such as agglomeration and ease of removal (such as rinse-ability).

Bulk/specialty gases—Although generic guidelines for impurities and chemicals are found in Table 80, specific needs may vary for each individual gas. No major changes are required for bulk ambient gases such as nitrogen, oxygen, argon, and hydrogen. Impurity reductions improvements have been pushed out to later

nodes in some cases. However, inline non-intrusive particle measurements at the critical size in these and specialty gases will be a significant challenge. Although current technology can be extended to meet the measurement requirements at point of use (POU) continuous particle monitoring in each specialty gas line would add substantial costs to factory infrastructure. For specialty gases the sensitivity to contamination may vary significantly by process. For example, a given contamination level in certain deposition gases may have far more impact than the same level of contaminants in certain etchant gases. POU filters, and in some cases purifiers and generators, can be utilized to meet the most stringent requirements. Cost-effective rapid response detection of molecular impurities is required. Purity requirements for gases related to low κ and Cu processes are too speculative to include at this time.

Novel materials—Impurity specifications for novel materials used in processing will be increasingly important. Specifications for critical materials such as novel metal oxides, CMP slurries, low/high dielectric materials, precursor materials (such as CVD and electroplating solutions) for novel barrier and conductor metals (such as Cu, Ta) have not been widely studied. Novel measurement techniques and impact studies are needed to ensure that these materials are produced with the impurity specifications that meet technology requirements.

Design-to-process interactions—The need for standard test structures is critical in determining defect sources and mechanisms. Once the design process interactions are understood, device design ground rules may be established and communicated that decrease process sensitivity. Cycles of process sensitivity analysis and reduction will be critical to advancing device design and yield. Additionally, sensitivities of designs to various levels of random defects need to be considered in the design process.

Process-to-process interactions—Interactions that result in defect formation (such as thickness of photoresist and contact density can affect the level of residue inside a via/contact) between process steps may drive particular requirements to a tool or process upstream or downstream that are not necessarily germane to that tool or process. Cluster tools and wet sinks are two examples of tools that must be carefully designed to ensure that their modules do not transfer any contaminants that degrade the performance of adjacent modules. To detect, to understand, and to eliminate unwanted process interactions, process monitoring and control will play a key role. The appropriate sensors and data must be available, along with an appropriate information management system to correlate process parameters to upstream/downstream parameters and yield and provide smart, intertool and intratool statistical process control (SPC).

Table 80a Defect Prevention and Elimination Technology Requirements—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
Wafer Environment Control							
Critical particle size (nm) [A]	90	90	75	65	60	55	50
Particles ³ critical size (/m^3) [B]	12	10	8	5	4	3	2
Airborne Molecular Contaminants (pptM) [C]							
Lithography—Bases (as amine, amide, or NH_3)	1000	1000	1000	750	750	750	750
Gate—Metals (as Cu, $E=2 \times 10^{-5}$) [C]	0.3	0.3	0.25	0.2	0.2	0.15	0.1
Gate—Organics (as molecular weight greater than or equal to 250, $E=1 \times 10^{-3}$) [D]	200	170	130	100	90	80	70
—Organics(as CH_2)	3600	3000	2400	1800	1620	1440	1260
Salicidation contact—acids (as Cl–, $E=1 \times 10^{-5}$)	10	10	10	10	10	10	10
Salicidation contact—bases (as NH_3, $E=1 \times 10^{-6}$)	40	32	24	20	16	12	10
Dopants (P or B) [F]	< 10	< 10	< 10	< 10	< 10	< 10	< 10
Process Critical Materials							
Critical particle size (nm) [B]	90	90	75	65	60	55	50
Ultrapure Water							
Total oxidizable carbon (ppb)	2	2	2	1	1	< 1	< 1
Bacteria (CFU/ liter)	< 1	< 1	< 1	< 1	< 1	< 1	< 1
Total Silica (ppb)	0.1	0.1	0.05	0.05	0.05	0.05	0.05
Dissolved oxygen (ppb)	10	7	3	1	1	1	1
Particles ³ critical size (/ml)	< 0.2	< 0.2	< 0.2	< 0.2	< 0.2	< 0.2	< 0.2
Critical cation, anion, metals (ppt, each)	20	20	< 20	< 20	< 20	< 20	10
Liquid Chemicals [E])							
Particles ³ critical size (/ml)	< 0.5	< 0.5	< 0.5	< 0.5	< 0.5	< 0.5	< 0.5
HF-, H_2O_2, NH_4OH: Fe, Cu (ppt, each)	< 250	< 220	< 180	< 150	<135	< 110	< 100
Critical cation, anion, metals (ppt, each)	< 20	< 20	< 20	< 10	< 10	< 10	< 5
HF-only TOC (ppb)	< 60	< 50	< 40	< 30	< 30	< 25	< 20
HCl, H_2SO_4: All impurities (ppt)	< 1000	< 1000	< 1000	< 1000	< 1000	< 1000	< 1000
BEOL Solvents, Strippers K, Li, Na (ppt, each)	< 1000	< 1000	< 1000	< 1000	< 1000	< 1000	< 1000
Bulk Ambient Gases							
N_2,O_2,Ar,H_2: H_2O,O_2,CO_2,CH_4 (ppt, each)	<1000	< 1000	< 1000	< 1000	< 1000	< 1000	< 1000
Particles > critical size (liter)	< 0.1	< 0.1	< 0.1	< 0.1	< 0.1	< 0.1	< 0.1
Specialty Gases							
POU Particles ³ critical size (/liter) [D]	2	2	2	2	2	2	2
Corrosives—metal etchants							
O_2 (ppbv)	< 500	< 500	< 500	< 500	< 500	< 500	< 200
H_2O (ppbv)	< 500	< 500	< 500	< 500	< 500	< 500	< 200
Inerts—Oxide/PR Etchants/Strippers							
O_2 (ppbv)	< 1000	< 1000	< 1000	< 1000	< 1000	< 1000	< 500
H_2O (ppbv)	< 1000	< 1000	< 1000	< 1000	< 1000	< 1000	< 500
Total metallics (pptwt)	< 500	< 500	< 500	< 500	< 500	< 500	< 500

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 80b Defect Prevention and Elimination Technology Requirements—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
Wafer Environment Control			
Critical particle size (nm) [A]	35	25	18
Particles ³ critical size (/m^3) [B]	1	1	1
Airborne Molecular Contaminants (pptM) [C]			
Lithography—Bases (as amine, amide, or NH_3)	< 750	< 750	< 750
Gate—Metals (as Cu, E=2 × 10^{-5}) [C]	0.07	< 0.07	< 0.07
Gate—Organics (as molecular weight greater than or equal to 250, E=1 × 10^{-3}) [D]	70	50	< 50
—Organics(as CH_2)	1260	900	< 900
Salicidation contact—acids (as Cl–, E=1 × 10^{-5})	10	10	10
Salicidation contact—bases (as NH_3, E=1 × 10^{-6})	4	< 4	< 4
Dopants (P or B) [F]	< 10	< 10	< 10
Process Critical Materials			
Critical particle size (nm) [B]	35	25	18
Ultrapure Water			
Total oxidizable carbon (ppb)	< 1	< 1	< 1
Bacteria (CFU/ liter)	< 1	< 1	< 1
Total Silica (ppb)	0.01	0.01	0.01
Dissolved oxygen (ppb)	1	1	1
Particles ³ critical size (/ml)	< 0.2	< 0.2	< 0.2
Critical cation, anion, metals (ppt, each)	1	1	1
Liquid Chemicals [E])			
Particles ³ critical size (/ml)	< 0.5	< 0.5	< 0.5
HF-, H_2O_2, NH_4OH: Fe, Cu (ppt, each)	< 50	< 50	< 50
Critical cation, anion, metals (ppt, each)	< 1	< 1	< 1
HF-only TOC (ppb)	< 15	< 10	< 10
HCl, H_2SO_4: All impurities (ppt)	< 1000	< 1000	< 1000
BEOL Solvents, Strippers K, Li, Na (ppt, each)	< 1000	< 1000	< 1000
Bulk Ambient Gases			
N_2,O_2,Ar,H_2: H_2O,O_2,CO_2,CH_4 (ppt, each)	< 100	< 100	< 100
Particles > critical size (liter)	< 0.1	< 0.1	< 0.1
Specialty Gases			
POU Particles ³ critical size (/liter) [D]	2	2	2
Corrosives—metal etchants			
O_2 (ppbv)	< 200	< 50	< 50
H_2O (ppbv)	< 200	< 50	< 50
Inerts—Oxide/PR Etchants/Strippers			
O_2 (ppbv)	< 500	< 100	< 100
H_2O (ppbv)	< 500	< 100	< 100
Total metallics (pptwt)	< 100	< 100	< 100

TOC—total oxidizable carbon

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Notes for Table 80a and b for Defect Prevention and Elimination Requirements

[A] Critical particle size is based on ½ design rule. All defect densities are "normalized" to critical particle size. Critical particle size does not necessarily mean "killer."

[B] Airborne particle requirements are based on an assumed value for deposition velocity of 0.01 cm/second, resulting in 1 particle/m^2/hr. for a ambient concentration of 3 particles/m^3. (This value represents an approximate value at atmospheric conditions. As an example, the 180 nm requirement is calculated as: (13 particles/m^2/step) × (300 steps)/1000 hrs) × (3 particles/ m^3/1 particle/m^2/hr =12 particles / m^3.

[C] Ion indicated is basis for calculation. Exposure time is 60 minutes with starting surface concentration of zero. Basis for lithography is defined by lithography roadmap. Gate metals and organics scale as surface preparation roadmap metallics and organics All airborne molecular contaminants calculated as $S=E*(N*V/4)$; where S is the arrival rate (molecules/second/cm^2), E is the sticking coefficient (between 0 and 1, N is the concentration in air (molecules/cm^3); and V is the average thermal velocity (cm/second)

[D] The sticking coefficients for organics vary greatly with molecular structure and are also dependent on surface termination. In general molecular weights < 250 not considered detrimental due to the higher volatility of these compounds.

[E] Particle targets apply at POU, not incoming chemical. Point-of-tool connection chemical metallic targets are based on Epi starting material, sub-ppb contribution from bulk distribution system, 1:1:5 standard clean 1 (SC-1) and elevated temperature 1:1:5 standard clean 2 (SC-2) final clean step. "HF last" or "APM last" cleans would require ~10x and ~100x improved purity HF (mostly Cu) and APM chemicals, respectively.

[F] Includes P, B, As, Sb

[G] Critical metals and ions include: Ca, Co, Cu, Cr, Fe, Mo, Mn, Na, Ni, W

[H] TOC values are based on best available technology and are not necessarily supported by yield data.

POTENTIAL SOLUTIONS

YIELD MODEL AND DEFECT BUDGET

The validation information provided by SEMATECH significantly improved the quality of the defect budgets in the 1997 iteration of the NTRS. This validation effort has continued for the 1999 revision. To ensure on-going relevance of roadmap defect targets, modeling validation should continue periodically. Research into better yield modeling techniques is required to address future modeling challenges. The increasing dominance of non-visual defects will further complicate yield modeling and defect budgeting. Thus defect models will need to better consider electrical characterization information, and reduce emphasis on visual analysis. This will require research into new characterization devices and methods and a better understanding of systematic and parametric impacts on device yield. Interconnect process layers are a particular challenge and have been so identified in the technology requirements. Some issues include modeling the yield impacts of ultra-thin film integrity, increased process complexity, interconnect speed and transmission characteristics, and the impact of wavelength dependent defects on reticle that may or may not result in defects. This research is complicated by the lack of state-of-the-art semiconductor processing capabilities in universities and other research sources. Figure 55 illustrates the potential solutions.

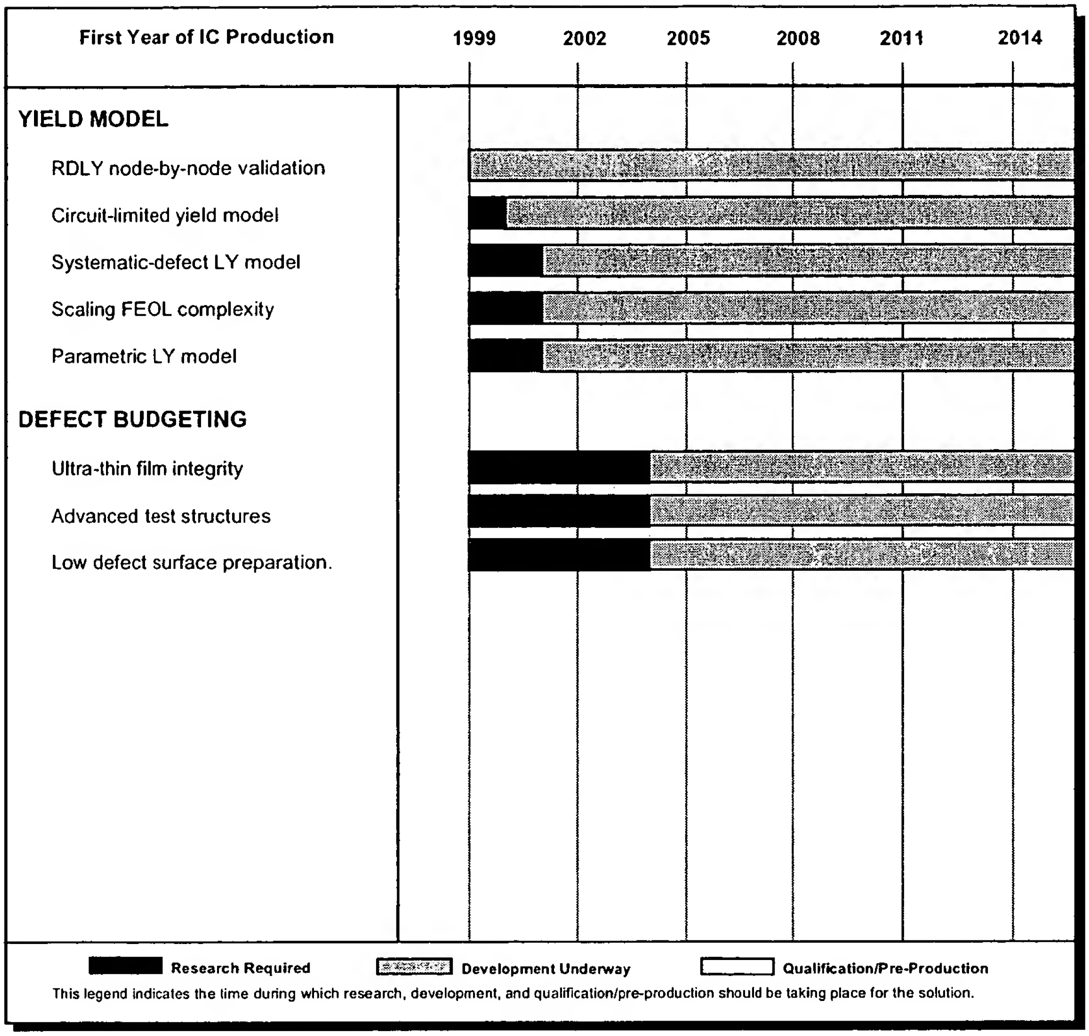

Figure 55 Yield Model and Defect Budget Potential Solutions

DEFECT DETECTION

Considerable research and development is necessary to meet the technology requirements for advanced defect detection tools. Figure 56 indicates the known set of potential solutions for defect detection. Light scattering and optical imaging solutions are expected to continue addressing the increased sensitivity requirements of patterned wafer defect detection for the next 2–3 technology nodes. Variations of these technologies could be utilized for detection of some high aspect ratio defects. The quest for an effective solution to the detection of very thin residue at the bottom of a single deep structure demands faster development of novel methods such as holographic imaging, e-beam (scattering or imaging), acoustic techniques, or X-ray imaging.

Demands on the pace of technical improvement and new detection tool development are tempered by the realization of suitable component technologies that form an integral part of the detection system. Significant advancements associated with shorter wavelength, compact, continuous-wave lasers, detectors with higher quantum efficiency and higher acquisition speed, suitable low-loss and low-aberration lenses, waveplates

and polarizers, and robust mechanical and acousto-optic scanners are needed in the near future to continue the economical development of optical techniques.

It is expected that major breakthroughs will be necessary to achieve the required throughputs at roadmap sensitivities (especially throughputs for yield ramp and volume production). Arrayed detection schemes for parallel data acquisition from a larger area of the wafer need to be explored. Enhancement of signal-to-noise ratio by means of software algorithms could potentially extend the applicability of optical approaches.

These solutions must also comprehend the need for greater amounts of defect-related data, such as composition, shape, defect classification, etc., and the need for greater intelligence and rapid decision making. (Refer to the following section on Defect Sources and Mechanisms for a comprehensive explanation of the needs in this area.) Automated defect classification, spatial defect signature analysis, adaptive sampling, yield impact assessment, and other artificial intelligence are already reducing time to decisions and product at risk. While continued software development will be key to advancing these capabilities, it is also important for defect detection equipment to produce more information for these techniques to analyze. The challenge of improved sensitivity to smaller defect sizes is rapidly blurring the line between detection tools and review platforms. While considering higher resolution imaging technologies, the tradeoff between associated throughput and amount of information is a crucial factor. With due consideration to the above, defect detection must evolve closer to the defect source and as such, development to integrate defect detection into process equipment must also be accelerated.

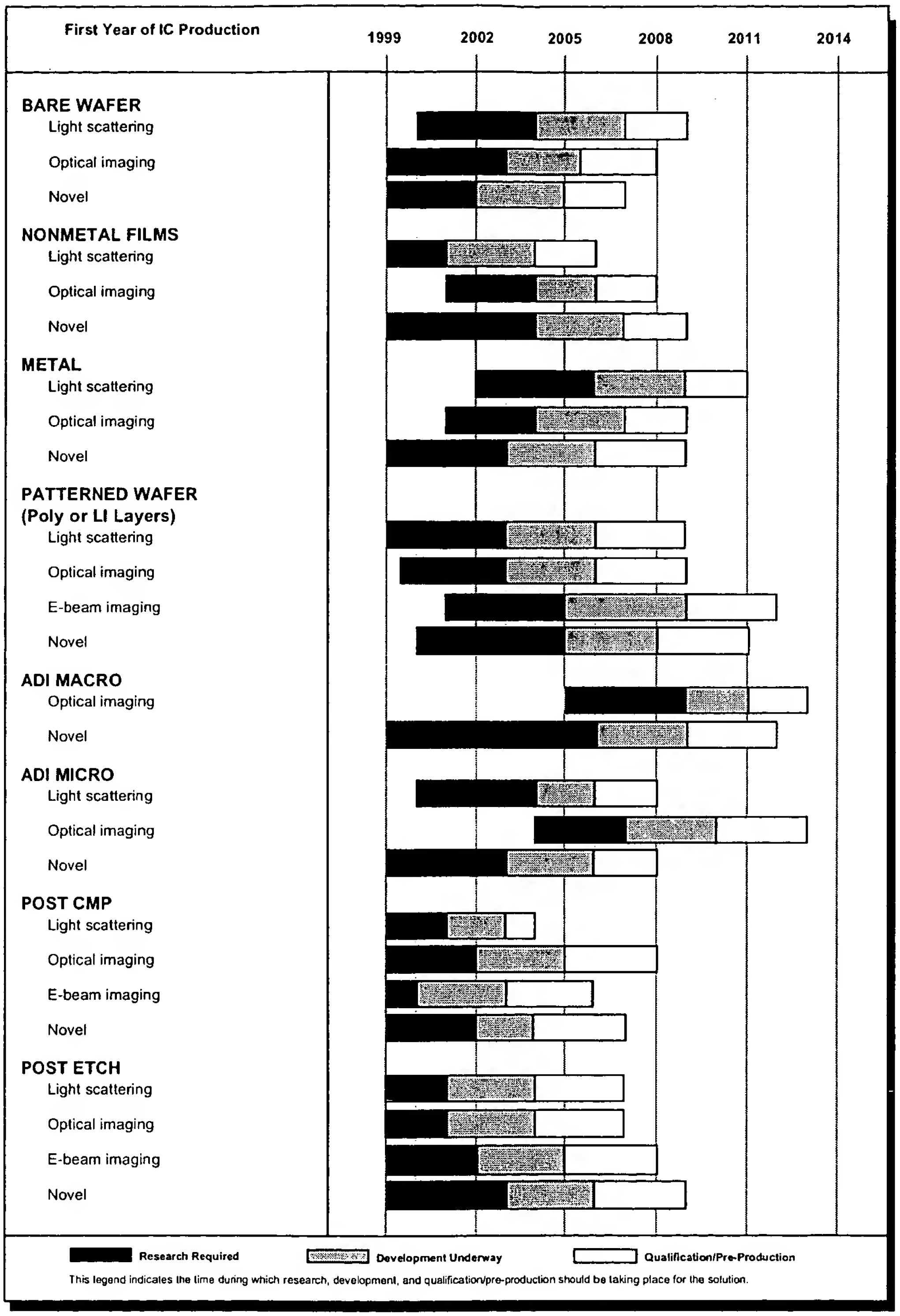

Figure 56 Defect Detection Potential Solutions

DEFECT SOURCES AND MECHANISMS

With the continued increase in complexity of the fabrication process, the ability to detect and react to yield impacting trends and excursions in timely fashion will require a larger dependence on passive data. This will be especially true during yield ramp where maximum productivity and profit benefits will be achieved. Passive data is defined as defect, parametric, and electrical test data collected inline from the product through appropriate sampling strategies. The additional time required to perform experiments, such as short-loop testing, will not be readily available at future nodes. The time necessary to trend potential problems and/or identify process excursions will require the development of sampling techniques that maximize the signal-to-noise ratio inherent in the measured data. The goal of IYM is to identify process issues in as few samples as possible. Analysis techniques that place product data in the context of the manufacturing process provide a stronger "signal" and are less likely to be impacted by measurement noise since they comprehend various levels of process history and human experience (lessons learned). Therefore, potential solutions to IYM include the development of technologies that generate information from product data and tool-health or other *in situ* process measurements. Automation methods are also required that correlate product information with fabrication processes, sometimes referred to as data-mining. Fundamental to the successful integration of new methods and technologies is a requirement for standards that facilitate data communications in the virtual and/or physically merged database environment.

VISIBLE DEFECTS

Although tools for sourcing visible defects are fairly well established (optical and SEM detection and review, SSA, ADC, EDX, FIB), new tools and methodologies will have to be developed to achieve adequate signal to noise ratio for differentiating real defects from background nuisance defects and to characterize the elemental composition of continuously shrinking visible defects.

NON-DETECTABLE DEFECTS

Affordable inspection techniques are needed that go beyond optical microscopy that offer high resolution without sacrificing throughput. To source non-detectable defects, the resolution of analytical tools for failure analysis needs to be improved. Technology nodes < 100 nm will require the development of affordable failure analysis techniques that can extend the range of detectable defects down to the atomic level. In addition, the resolution of internal node DC micro-probing for characterizing individual circuit/transistor parameters or isolating leakage paths needs to be improved. Design to process interactions that can lead to localized non-detectable structural defects have to be researched and modeled. Design for Testability/Diagnosibility techniques need to utilize these models to enhance the localization of a defect source.

PARAMETRIC DEFECTS

Saving more parametric data as measured on circuit testers will aid in sourcing parametric source defects. This information will allow for correlation to process data, through a variety of techniques, including spatial signature analysis. Modeling the probabilities of factors that can lead to "parametric defects" can also reduce the time it takes to source the cause. BIST techniques should be developed to identify race conditions and other failure modes that are a function of parametric variation or mismatch.

ELECTRICAL FAULTS

Presently memory array test chips and memory arrays within microprocessors are used to quickly isolate faults and is likely to continue for non-arrayed devices. Future products must be designed so that the test process can isolate failures. Design for test (DFT) and built in self-test (BIST) are two methods that can aid in defect isolation. Both DFT and BIST failure pattern must map to a physical location on a circuit. Accurate fault to defect mapping models must also be developed to further assist in the defect localization process. Other test programs are needed to save failure pattern information so that it can be analyzed based on pre-determined (modeled) failure mode probabilities. All of these techniques will allow yield engineers to more quickly and precisely determine the locations and causes of circuit failures.

DATA MANAGEMENT SYSTEMS (DMS)

The following key areas of R&D investment have been identified as necessary elements for meeting tomorrow's DMS challenges:

- Standards for data/file formats and coordinate systems

- Cost of ownership modeling for DMS
- DMS/WIP integration
- DMS methodologies for data collection, storage, archiving and purging
- DMS for advanced tool/process control

The key findings of this report by Oakridge National Lab (ORNL), as part of a SEMATECH-sponsored 1999 DMS assessment study, are presented in a summary provided as supplementary material of this roadmap. Also refer to Figure 57 indicating areas for potential solutions.

Additional information on defect mechanisms is also provided in supplemental material.

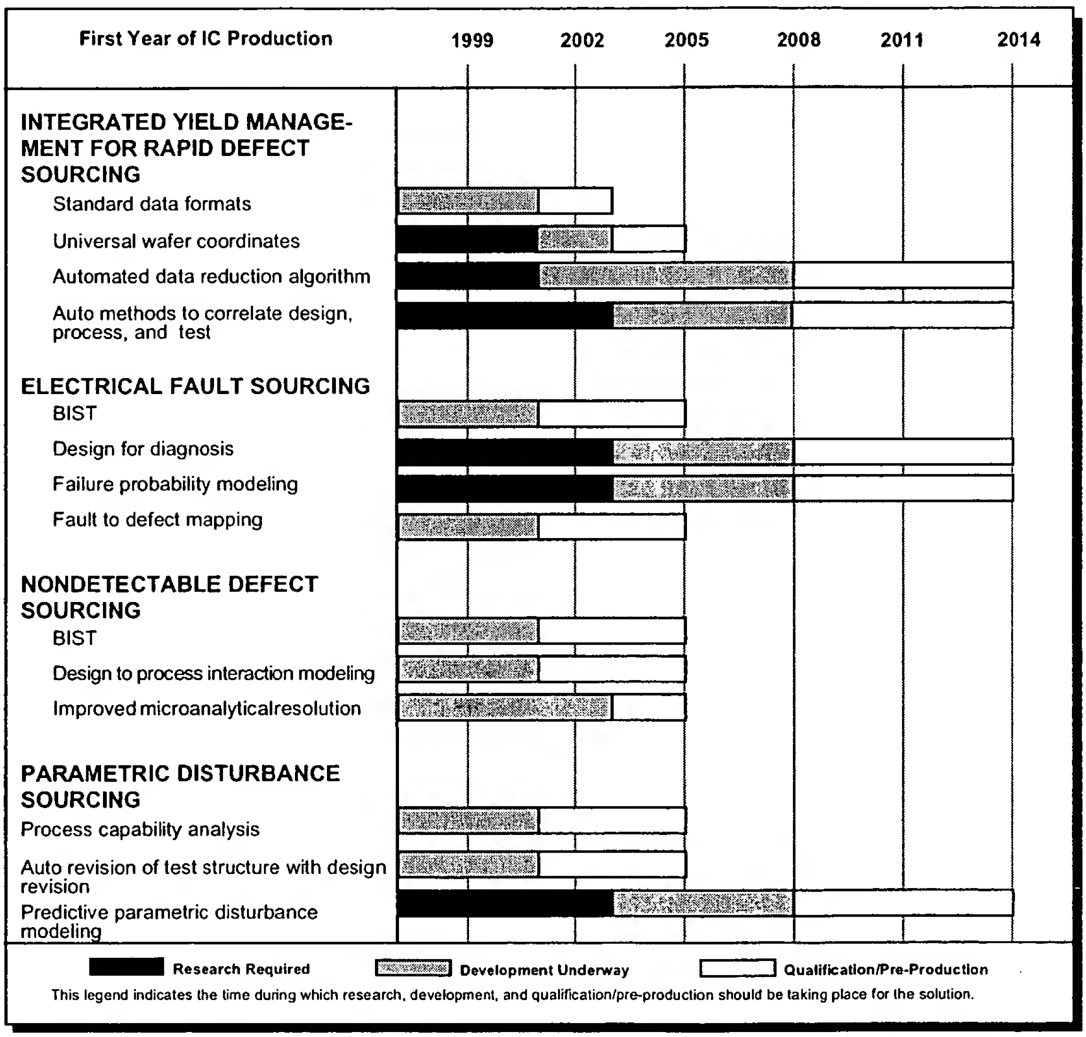

Figure 57 Defect Sources and Mechanisms Potential Solutions

DEFECT PREVENTION AND ELIMINATION

Process Equipment—Defect reduction in process equipment remains paramount to achieving defect density goals. Solutions and technology developments are expected to provide major enhancement capabilities in the

next 15 years and actually enable cost-effective high volume manufacturing for 130–100 nm devices. Refer to Figure 58. Equipment defect targets are primarily based on horizontal scaling. Vertical faults, particularly as they apply to the gate stack, metallic, and other nonvisual contaminants, and parametric sensitivities need to be understood. New cleaning chemistries, *in situ* chamber monitoring, materials development, and other techniques including improved techniques of parts cleaning can help maintain chamber cleanliness run-to-run and dramatically reduce the frequency of chamber wet cleans. These developments will also act to increase equipment utilization. Reduced backside wafer contamination control must drive both measurement technology and fundamental changes in equipment. Metal/particle cross contamination from backside to next wafer front-side, hot spots/depth of focus in lithography, and punch through on electrostatic chucks are all examples of issues that must be addressed in future tools. Particle avoidance techniques (o-ring material selection, gas flow/temperature management, wafer chuck optimization) will continue to play a key role in meeting defect densities. It is believed that a more fundamental understanding of reactor contamination formation, transport, and deposition will be required to enhance current equipment and process design and aid in the placement and interpretation of data from *in situ* sensors. These fundamental physical, chemical, and plasma reactor contamination models must be employed. *In situ* process control will become increasingly important to reduce process-induced defects and to minimize requirements for post-measurements. Intelligent process control at a tool requires a fundamental understanding of how parameters impact device performance. Open tool control systems that allow both users and equipment suppliers to easily integrate new sensor and new control software will be necessary to enable intelligent process control.

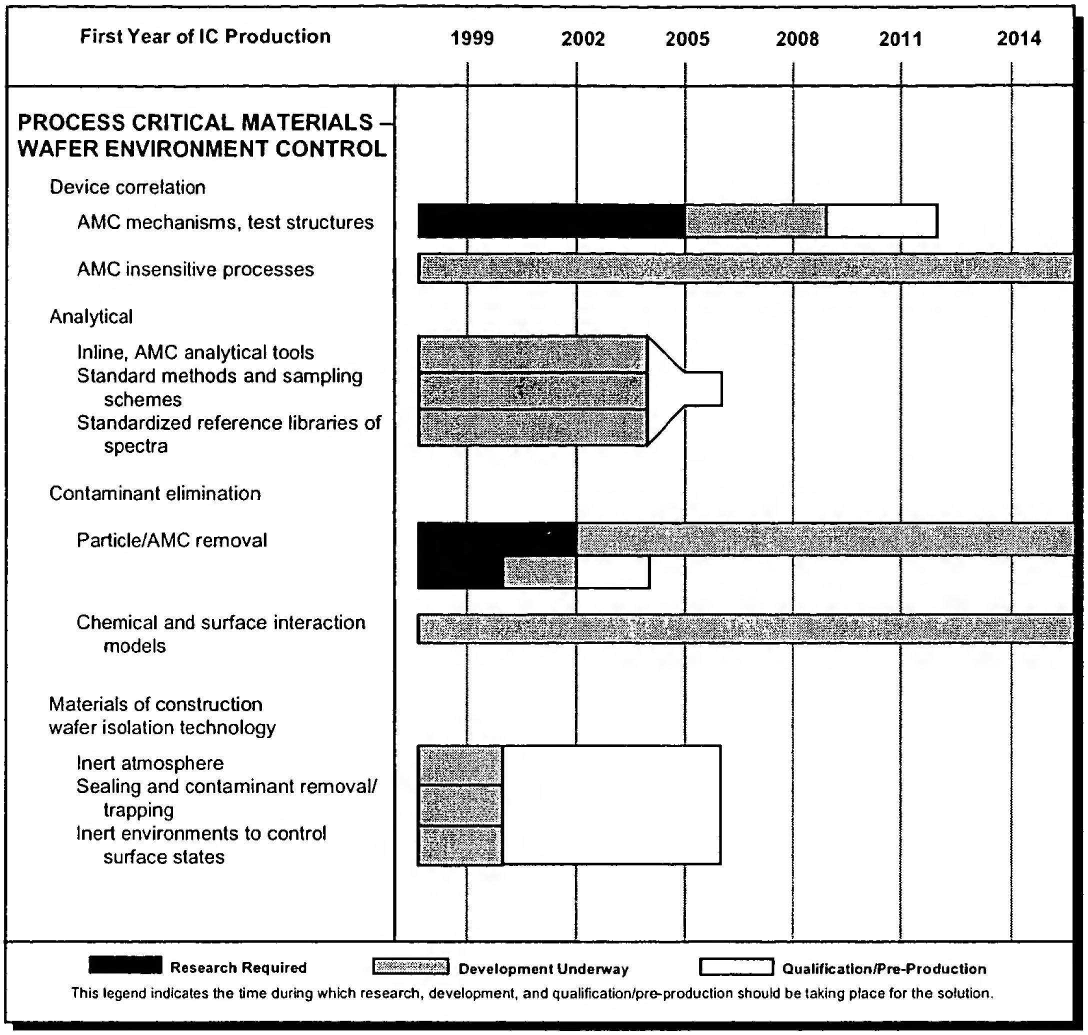

Figure 58 Defect Prevention and Elimination Potential Solutions

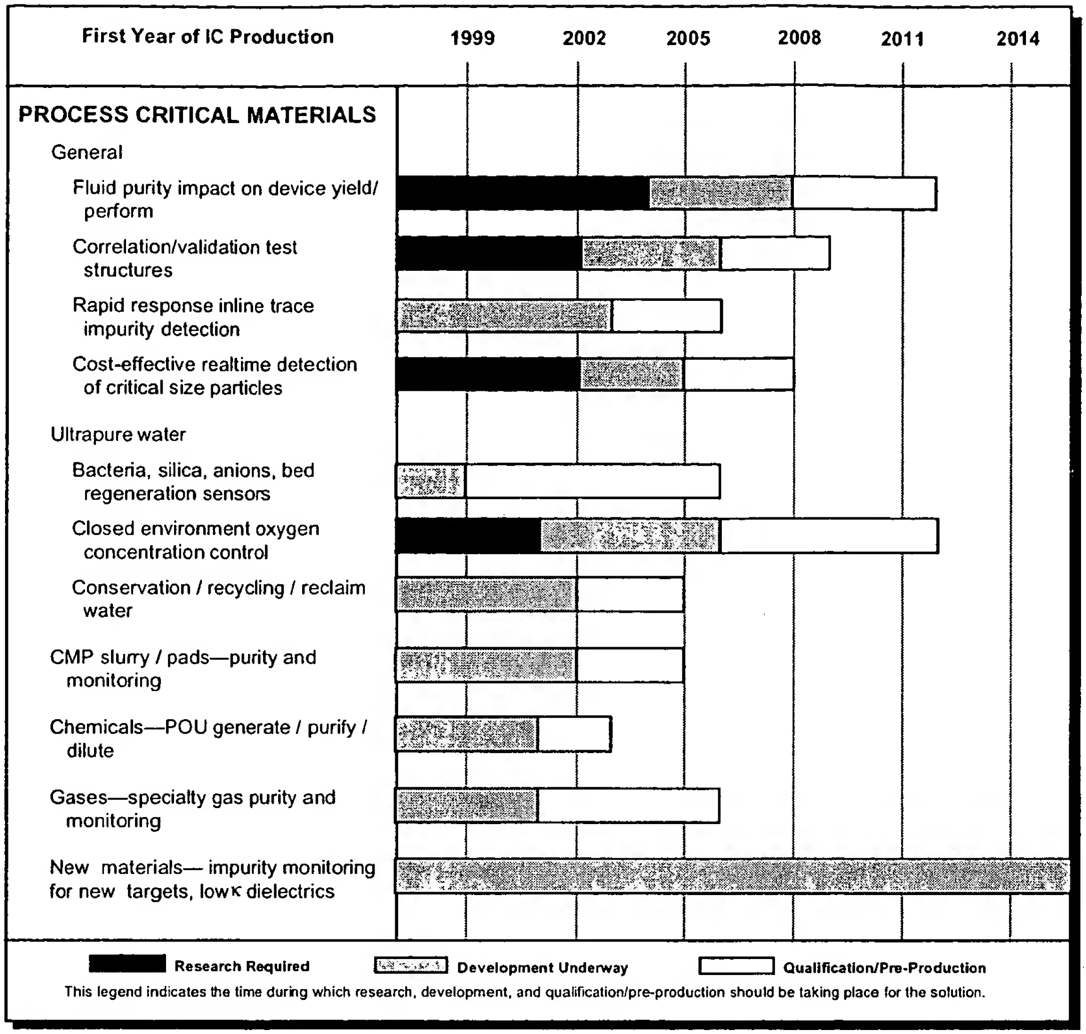

Figure 58 Defect Prevention and Elimination Potential Solutions (continued)

Process critical materials—Figure 58 illustrates the set of potential solutions for prevention and elimination of defects. Further studies into device impact are necessary to validate any need for increased purities. System concerns such as corrosion potential may lead process concerns in seeking higher purities. UPW quality focus needs to move towards the point of use. Water quality is generally measured at the point of production and not at the POU or at the wafer. An understanding of the impact of the tool upon water quality, specifically particles, bacteria, and dissolved oxygen, needs to be understood to ensure quality is carried to the wafer. Inline trace impurity analytical technology for process critical materials is needed to better understand purity levels at the POU. Ultrapure water particle levels are easily achieved with existing design and filtration practice and verified with available offline particle metrology. Improved online monitoring is required to detect excursions realtime for particle sizes below 0.1 µm. Improved analytical technology is needed to characterize ultra-trace levels of bacteria (both viable and nonviable). Recycling and reclaiming initiatives must drive improvements in rapid online analytical technology, especially detection of organics, to ensure that POU-recycled UPW is equal or better than single-pass water. Demonstration of the

effectiveness and efficiency of particle filters in specialty gases is needed to increase the confidence that the filters are performing adequately without continuous monitoring. The requirements to measure particles at POU for specialty gases below 100 nm can be met by the development of an inline condensation nucleus counter (CNC) or novel techniques compatible with oxidizers, corrosives, and flammable and toxic gases. Specifications and standard test methods will need to be established for new materials.

Wafer environment control—As the list of ambient contaminants to be controlled broadens so must measurement capabilities. Availability of affordable, accurate, repeatable, real time sensors for nonparticulate contamination are becoming increasingly necessary. The use of inert environments to transport and store wafers is expected to increase with process sensitivities. Pre-gate and pre-contact clean and salicidation are cited as processes to first require this capability. In addition, using inert environments offers the opportunity to reduce the introduction of moisture into vacuum loadlock tools, thereby decreasing contamination and loadlock pumpdown times. While closed carrier purging systems exist and are evolving, tool environments that may need to become inert, such as wet sink endstations, present a challenge. As wafer isolation technologies evolve, design and material selection of carriers and enclosures will be critical for performance in isolating the wafers from the ambient and in not contributing contaminants themselves. In addition, the materials and designs must not promote cross-contamination between processes. Seal technology, low-outgassing, and nonabsorbing materials development are key to effective wafer isolation deployment.

International Technology Roadmap for Semiconductors 1999 Edition

Metrology

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METROLOGY

Advances in metrology are essential to the reduction of feature size and introduction of new materials and processes for future technology generations. Metrology accelerates yield improvement at every stage of manufacturing. It enables tool improvement, ramping in pilot lines and factory start-ups, and improvement of yield in mature factories. Metrology can reduce the cost of manufacturing and the time-to-market for new products through better characterization of process tools and processes. The metrology community must accelerate cooperative research, development, and prototyping in order to meet the ITRS timeline. The feature sizes at the end of the 1999 Roadmap will greatly challenge both microscopy and thickness measurements.

Measurement technology combined with computer integrated manufacturing (CIM) and data management systems provides information-based process control. Metrology will slowly migrate from offline to inline and *in situ* to achieve Roadmap goals. In addition, over the next ten years, microelectromechanical systems (MEMS) are expected to evolve into new types of metrology sensors and test structures. The combination of offline, inline, and *in situ* measurements will enable advanced process control and rapid yield learning.

Manufacturing process stability requires stable tools. The objective is for every tool to perform like every other such tool, with no unique signatures. An appropriate combination of well-engineered tools and appropriate metrology is necessary to maximize productivity while maintaining acceptable cost of ownership.

SCOPE

The metrology topics covered in the 1999 *Metrology* roadmap are microscopy; critical dimension (CD) and overlay; film thickness and profile; materials and contamination analysis; dopant profile; *in situ* sensors for process control; reference materials; correlation of physical and electrical measurements; and packaging. These topics are reported in the following sections: *Metrology for Processes Facing Statistical Limits*; *Microscopy*; *Lithography*; *Front End Processes*; *Interconnect*; *Materials and Contamination Characterization*; *Reference Materials*; *Metrology Integration*; and *Packaging Metrology*.

Metrology and standards research institutes, standards organizations, metrology tool suppliers, and the university community should continue to cooperate on standardization and improvement of methods and on production of reference materials. The measurement precision to tolerance (P/T) ratio for evaluation of automated measurement capability for use in statistical process control relates the measurement variation (precision) of the metrology tool to the specified limits of the process The determination of measurement tool variations is frequently carried out using reference materials that are not representative of the process of interest. Thus, the measurement tool precision information may not reflect measurement-tool induced variations on product wafers. It is possible that the sensitivity of the instrument could be insufficient to detect small but unacceptable process variations. There is a need for a metric that describes the resolution capability of metrology tools for use in statistical process control. Since the type of resolution (such as thickness requires spatial resolution, levels of metallics on the surface require resolution of atomic percent differences) depends on the process, topic-specific metrics may be required. Such a metric for distinguishing process variability from metrology tool variability also needs to receive more emphasis. The inverse of the measurement precision-to-process variability is sometimes called the signal-to-noise ratio or the discrimination ratio.

Wafer manufacturers, process tool suppliers, pilot lines, and factory start-ups all have different timing and measurement requirements. The need for a shorter ramp-up time for pilot lines means that characterization of tools and processes prior to pilot line startup must improve. However, as the process matures, the need for some types of metrology may decrease. As device dimensions shrink, the challenge for physical metrology will be to keep pace with inline electrical testing that provides critical electrical performance data.

INFRASTRUCTURE NEEDS

A healthy industry infrastructure is required if suppliers are to provide cost-effective metrology tools, sensors, controllers, and reference materials. New research and development will be required if opportunities such as MEMS are to make the transition from R&D to commercialized products. Many metrology suppliers are small companies that find the cost of providing new tools for leading-edge activities prohibitive. Initial sales of metrology tools are to tool and process developers. Sustained, high-volume sales of the same metrology equipment to chip manufacturers does not occur until several years later. The present infrastructure cannot support this delayed return on investment. Funding that meets the investment requirements of the supplier community is needed to take new technology from proof of concept to prototype systems and finally to volume sales.

DIFFICULT CHALLENGES

Metrology needs by 2005 will be affected by new materials and processes. Thus, it is difficult to identify all future metrology needs. Shrinking feature sizes, tighter control of device electrical parameters, such as threshold voltage and leakage current, and new interconnect materials will provide the main challenges for physical metrology methods. To achieve desired device scaling, metrology tools must be capable of measurement of properties on atomic distances. Table 81 presents the ten major challenges for metrology.

Table 81 Metrology Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥ 100 nm / BEFORE 2005	*SUMMARY OF ISSUES*
Factory level and company wide metrology integration for *in situ* and inline metrology tools; continued development of robust sensors and process controllers; and data management that allows integration of add-on sensors	Standards for process controllers and data management must be agreed upon. Conversion of massive quantities of raw data to information useful for enhancing the yield of a semiconductor manufacturing process. Better sensors must be developed for trench etch end point, ion species/energy/dosage (current), and wafer temperature during RTA.
Impurity detection (particles, oxygen, and metallics) at levels of interest for starting materials and reduced edge exclusion for metrology tools	Existing capabilities will not meet Roadmap specifications. Very small particles must be detected and properly sized. Detectivity of trace metals in bulk silicon or in the top silicon layer of SOI (silicon on insulator) must be enhanced.
Measurement of the frequency-dependent dielectric constant of low κ interconnect materials at 5xto 10x base frequency.	Equipment, procedures, and test structures need to be reduced to practice and applied to low κ interconnect materials that account for clock harmonics, skin effects, cross-talk, and anisotropy of materials.
Control of high-aspect ratio technologies such as Damascene challenges all metrology methods.	New process control needs are not yet established. For example, 3-dimensional (CD and depth) measurements will be required for trench structures in new, low κ dielectrics.
Measurement of complex material stacks	Reference materials and standard measurement methodology for new, high κ gate and capacitor dielectrics with interface layers, thin films such as interconnect barrier and low κ dielectric layers, and other process needs. Optical measurement of gate and capacitor dielectric averages over too large an area and needs to characterize interfacial layers. The same is true for measurement of barrier layers.

Table 81 Metrology Difficult Challenges (continued)

ADDITIONAL DIFFICULT CHALLENGES < 100 nm / BEYOND 2005	
Nondestructive, production worthy wafer and mask level microscopy for critical dimension measurement, overlay, defect detection, and analysis	Surface charging and contamination interfere with electron beam imaging. CD measurements must account for side wall shape. CD for Damascene process may require measurement of trench structures.
Standard electrical test methods for reliability of new materials, such as ultra-thin gate and capacitor dielectric materials, are not available.	The wearout mechanism for new, high κ gate and capacitor dielectric materials is unknown.
Statistical limits of sub-70 nm process control	Controlling processes where the natural stochastic variation limits metrology will be difficult. Examples are low-dose implant, thin gate dielectrics, and edge roughness of very small structures.
3D dopant profiling	The dimensions of the active area approach the spacing between dopant atoms, complicating both process simulation and metrology. Elemental measurement of the dopant concentration at the requested spatial resolution is not possible.
Production worthy, physical inline metrology for transistor processes that provides SPC* required to achieve consistent electrical properties	Presently, the combined physical metrology for gate dielectric, CD, and dopant dose and profile is not adequate for sub-70 nm design rules.

** SPC—statistical process control*

TECHNOLOGY REQUIREMENTS

Selected measurement requirements for metrology tools are listed in Tables 82–85. The microscopy resolution refers to the ability of a CD measurement tool to distinguish between lines that differ in width. The spatial resolution requirements for 2- and 3-dimensional (2D and 3D) dopant profiling are based on the requirements of Modeling & Simulation. Meeting 2D dopant profiling requirements will be difficult, and methods with slightly less spatial resolution may provide useful information. Measurement accuracy for all metrology requires appropriate reference materials.

Table 82a Metrology Technology Requirements—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
DRAM ½ Pitch	180	165	150	130	120	110	100	D½
MPU Gate Length	140	120	100	85	80	70	65	M Gate
Microscopy								
Inline, nondestructive microscopy resolution (nm) for P/T=0.1	1.4	1.2	1.0	0.85	0.8	0.7	0.65	M Gate
Maximum aspect ratio / diameter (nm) (DRAM contacts) [A]	6.3 200	6.7 175	7.1 160	7.5 140	8.0 130	8.5 120	9 110	D½
Materials and Contamination Characterization								
Real particle detection limit (nm) [B]	90	82	75	65	60	55	50	M Gate
Minimum particle size for compositional analysis (on dense lines) (nm)	48	40	33	28	27	23	22	M Gate
Specification limit of total surface contamination Ca, Co, Cu, Cr, Fe, K, Mo, Mn, Na, Ni (atoms/cm^2)	$\leq 9\times10^9$	$\leq 7\times10^9$	$\leq 6\times10^9$	$\leq 4.4\times10^9$	$\leq 3.4\times10^9$	$\leq 2.9\times10^9$	$\leq 2.5\times10^9$	M Gate
Surface detection limits for individual elements Ca, Co, Cu, Cr, Fe, K, Mo, Nm, Na, Ni (atoms/cm^2) with signal to noise of 3:1 for each element	$\leq 9\times10^8$	$\leq 7\times10^8$	$\leq 6\times10^8$	$\leq 4.4\times10^8$	$\leq 3.4\times10^8$	$\leq 2.9\times10^8$	$\leq 2.5\times10^8$	M Gate

Table 82b Metrology Technology Requirements—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
DRAM ½ Pitch	70	50	35	D½
MPU Gate Length	45	32	22	M Gate
Microscopy				
Inline, nondestructive microscopy resolution (nm) for P/T=0.1	0.45	0.32	0.22	M Gate
Maximum aspect ratio / diameter (nm) (DRAM contacts) [A]	10.5 80	12 60	13.5 45	D½
Materials and Contamination Characterization				
Real particle detection limit (nm) [B]	35	25	17	M Gate
Minimum particle size for compositional analysis (on patterned wafers) (nm)	15	10	7	M Gate
Specification limit of total surface contamination Ca, Co, Cu, Cr, Fe, K, Mo, Mn, Na, Ni (atoms/cm^2)	$\leq 2.1\times10^9$	$\leq 1.8\times10^9$	$\leq 1.7\times10^9$	M Gate
Surface detection limits for individual elements Ca, Co, Cu, Cr, Fe, K, Mo, Nm, Na, Ni (atoms/cm^2) with signal to noise of 3:1 for each element	$\leq 2.1\times10^8$	$\leq 1.8\times10^8$	$\leq 1.7\times10^8$	M Gate

[A] Metal and via aspect ratios are additive for dual-damascene process flow.
[B] This value depends on surface microroughness and layer composition.

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

MEASUREMENTS FOR PROCESSES FACING STATISTICAL LIMITS

As the dimensions of integrated circuit devices continue to shrink, the finite dimensions of the atoms within the structures will lead to statistical variations in critical dimensions. For instance, a silicon atom at the edge of a 50 nm gate represents about 0.6% of the gate length. The effects of statistical variations may be even more pronounced in gate dielectric structures composed of multi-layers of different components, each only several atoms thick. The engineering of such structures must take these statistical variations into account to obtain sufficiently uniform barrier height, tunneling current density, and dielectric constant properties. Continuing advances in metrological techniques will be required to characterize advanced multilayer dielectrics.

Advances in interconnect technology are introducing conductor materials such as copper that must be excluded from the semiconductor itself and low κ interconnect structures. Process and process modeling advances are required to deposit barrier layers of the order of only a few atomic layers that are pin hole-free. Metrology must be developed to ensure the integrity of barrier layers.

The inevitable variations in the positions of dopant atoms and intrinsic defects within semiconductor structures will cause variations in the transport properties of the transistors. Statistical variations in their local densities and positions within the depletion layers will generate significant variations in transistor properties. Innovations in device design are required to accommodate these statistical variations. Stochastic modeling strategies will be required to supplement deterministic (continuum) modeling techniques that have been used thus far. Significant advances in two- and three-dimensional dopant profiling metrology will be required.

These and other statistical variations in real materials and structures are independent of measurement uncertainties, and will add quadratically to the total uncertainty of the values of measured quantities. In addition, they must be taken into account in circuit and process design in ways that are not yet envisioned. It appears that the measurement uncertainties of a number of parameters specified for future device generations elsewhere in the Roadmap cannot be met for fundamental physical reasons having little to do with metrology *per se*.

MICROSCOPY

Microscopy is used in most of the core technology processes. Microscopes typically employ far-field light, electron beam, or scanned probe methods. Inline microscopy applications include CD and overlay measurement along with defect/particle detection, review and auto-classification. Because of the high value of wafers, the need for rapid, nondestructive, inline measurement is growing. In addition to feature size measurement, shape measurement should be available inline.

Scanning Electron Microscopy (SEM)—continues to provide at-line and inline imaging for characterization of cross-sectional samples, particle and defect analysis, inline defect imaging (defect review), and CD measurements. Improvements are needed for effective CD and defect review (and SEM detection in pilot lines) at or beyond the 100 nm generation. New inline SEM technology, such as the use of ultra-low voltage electron beams (<250 eV) may be required for overcoming image degradation due to charging, contamination, and radiation damage of the sample surface, while maintaining adequate resolution. Improving the resolution of an SEM by the reduction of spherical aberration leads to an unacceptably small depth of field; consequently non-image forming techniques such as holography are to be preferred.

There is a need to improve the modeling of the signal generation process by including the effects of sample charging and the role of the instrument electronics. A better understanding of the relationship between the physical object and the waveform analyzed by the instrument is expected to improve CD measurement. Sample damage, which arises from direct ionization damage of the sample and the deposition of charge in gate structures, sets a fundamental limit to the utility of all microscopies relying on charged particle beams.

Determination of 3D sidewall shape for sub-100 nm contact/vias, transistor gates, interconnect lines or damascene trenches will require continuing advances in existing microscopy and sample preparation

methods. Cross sectioning by FIB and liftout for imaging in a TEM or a STEM has been successfully demonstrated. Reflection electron holography has also been proposed as a method for observing 3D sidewall shape.

Scanning probe microscopy (SPM)—may be used to calibrate CD-SEM measurements. Stylus microscopes offer 3D measurements that are insensitive to the conductivity of the material scanned. Flexing of the stylus degrades measurements, however, when the probe is too slender. The stylus shape and aspect ratio must, therefore, be appropriate for the probe material used and the forces encountered. High stiffness probe materials, such as carbon nanotubes, alleviate this problem.

Far-field optical microscopy—is limited by the wavelength of light. DUV sources and near-field microscopy are being developed to overcome these limitations. Improved software allowing automatic classification of defects is needed. Optical microscopes will continue to have application in the inspection of large features, such as solder bump arrays for multi-chip modules.

For *defect detection*—each technology has limitations. A defect is defined as any physical, electrical, or parametric deviation capable of affecting yield. Existing SEMs and SPMs are considered too slow for the efficient detection of defects too small for optical microscopes. High speed scanning has been demonstrated with arrayed SPMs, but issues associated with stylus uniformity, characterization, and wear need to be addressed. The technique is most likely to be useful on surfaces with relatively gentle surface slopes and thus to the characterization of surface planarity. This technology should be pursued both by expanding the size of the array and in developing additional operational modes. Arrayed micro-column SEMs have been proposed as a method of improving SEM throughput, and operation of a single micro-SEM has been demonstrated. Research is needed into the limits of electrostatic and magnetic lens designs.

LITHOGRAPHY METROLOGY

Physical metrology is challenged by the advancement of lithography capabilities and is not meeting required improvements for precision and reproducibility. Whether optical lithography is extended or a next generation lithography (NGL) technology is introduced, new wafer and mask metrology needs will emerge. Mask and wafer CD metrology tool resolution, accuracy, tool-to-tool matching, and reproducibility all require significant advancement if they are to meet the accelerating timing of the industry needs. Additionally metrologists must learn how to effectively extract three-dimensional data from CD and overlay measurements to provide the maximum level of process control. The use of "feed forward" control concepts must be extended to lithography metrology taking data from resist measurements and controlling subsequent processing, such as etch, to improve product performance. Electrical measurements provide a monitoring of gate and interconnect linewidth, but only after the point where reworking the wafers is no longer possible. Future overlay metrology requirements, along with problems caused by low contrast levels, will drive the development of new optical or SEM methods along with scanning probe microscopy (SPM).

Methods for measurements of mask image placement will become more complex as many of the new technologies will require pattern-specific predistortion for mask writing that will force verification of the actual corrections. This will be most critical in the early development phases forcing early metrology tool development. Wafer level overlay will be equally challenged by the potential introduction of step and stitch lithography tools. Statistical methods such as dynamic averaging are under investigation. Innovations, such as scatterometry, will require application development before being accepted. Further innovations are required, including those captured in the Metrology roadmap section on microscopy. Metrology requirements for Lithography are listed in Table 83 below and potential solutions are shown in Figure 59.

Table 83a Lithography Metrology Requirements—Near Term

YEAR TECHNOLOGY NODE	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*
Wafer gate CD control*	13	10.8	9.0	8.1	7.2	6.3	5.9
Wafer dense line CD control*	18	16.5	15	13	12	11	10
Wafer contact CD control*	20	18.5	17	15	14.5	14	13
Wafer CD metrology tool precision* P/T=.2 for isolated lines**	2.6	2.2	1.8	1.6	1.4	1.3	1.2
Wafer CD metrology tool precision* P/T=.2 for dense lines**	3.6	3.3	3.0	2.6	2.4	2.2	2.0
Wafer CD metrology tool precision* P/T=.2 for contacts**	4.0	3.7	3.4	3.0	2.9	2.6	2.3
Maximum CD measurement bias (%)	10	10	10	10	10	10	10
Mask CD control isolated lines*	16	14	12	10	9	8	7
Mask CD control dense lines*	24	21	17	13	12	11	10
Mask contact area control Normalized to ρ of Area*	24	21	17	14	13	12	11
Mask CD metrology tool precision* P/T=.2 for isolated lines**	3.2	2.8	2.4	2	1.8	1.6	1.4
Mask CD metrology tool precision* P/T=.2 for dense lines**	4.8	4.2	3.4	2.6	2.4	2.2	2
Mask area metrology tool precision for contact normalized to ρ of area–ρ of target for P/T=.2	4.8	4.2	3.4	2.8	2.6	2.4	2.2
Wafer overlay control (nm)	65	58	52	45	42	38	35
Wafer overlay output metrology precision (nm, 3 sigma)* P/T=.1	6.5	5.8	5.2	4.5	4.2	3.8	3.5
Final mask image placement	39	35	31	27	25	23	21
Mask image placement Metrology precision P/T=.1	3.9	3.5	3.1	2.7	2.5	2.3	2.1
Mask phase (in degrees)	2	2	2	2	2	2	2
Phase metrology precision P/T=.2 (in degrees)	.4	.4	.4	.4	.4	.4	.4
Variation in attenuated mask film transmission % of deviation from nominal (%)	4	4	4	4	4	4	4
Transmission metrology precision % of nominal attenuated psm transmission P/T=.2 (%)	.8	.8	.8	.8	.8	.8	.8

* *All precision values are 3 sigma in nm and include metrology tool matching.*

** *Measurement tool performance needs to be independent of line shape, line materials, and density of lines.*

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 83b Lithography Metrology Requirements—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
Wafer gate CD control*	4.0	3.0	2.0
Wafer dense line CD control*	7.0	5.0	3.5
Wafer contact CD control*	8.0	5.5	4.0
Wafer CD metrology tool precision* P/T=.2 for isolated lines**	0.8	0.6	0.4
Wafer CD metrology tool precision* P/T=.2 for dense lines**	1.4	1.0	0.7
Wafer CD metrology tool precision* P/T=.2 for contacts**	1.6	1.1	0.8
Maximum CD measurement bias (%)	10	10	10
Mask CD control isolated lines*	7	5	3.3
Mask CD control dense lines*	11	8	5.6
Mask contact area control Normalized to ρ of area*	12	9	6.4
Mask CD metrology tool precision* P/T=.2 for isolated lines**	1.4	1.0	0.7
Mask CD metrology tool precision* P/T=.2 for dense lines**	2.2	1.6	1.1
Mask area metrology tool precision for contact normalized to ρ of area–ρ of target for P/T=.2	1.6	1.8	1.3
Wafer overlay control (nm)	25	20	15
Wafer overlay output metrology precision (nm, 3 sigma)* P/T=.1	2.5	2.0	1.5
Final mask image placement	15	12	9
Mask image placement metrology precision P/T=.1	1.5	1.2	0.9
Mask phase (in degrees)	1	NA	NA
Phase metrology precision P/T=.2 (in degrees)	0.2	NA	NA
Variation in attenuated mask film transmission % of deviation from nominal (%)	4	NA	NA
Transmission metrology precision % of nominal attenuated PSM transmission P/T=.2 (%)	0.8	NA	NA

* *All precision values are 3 sigma in nm and include metrology tool matching.*

** *Measurement tool performance needs to be independent of line shape, line materials, and density of lines.*

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

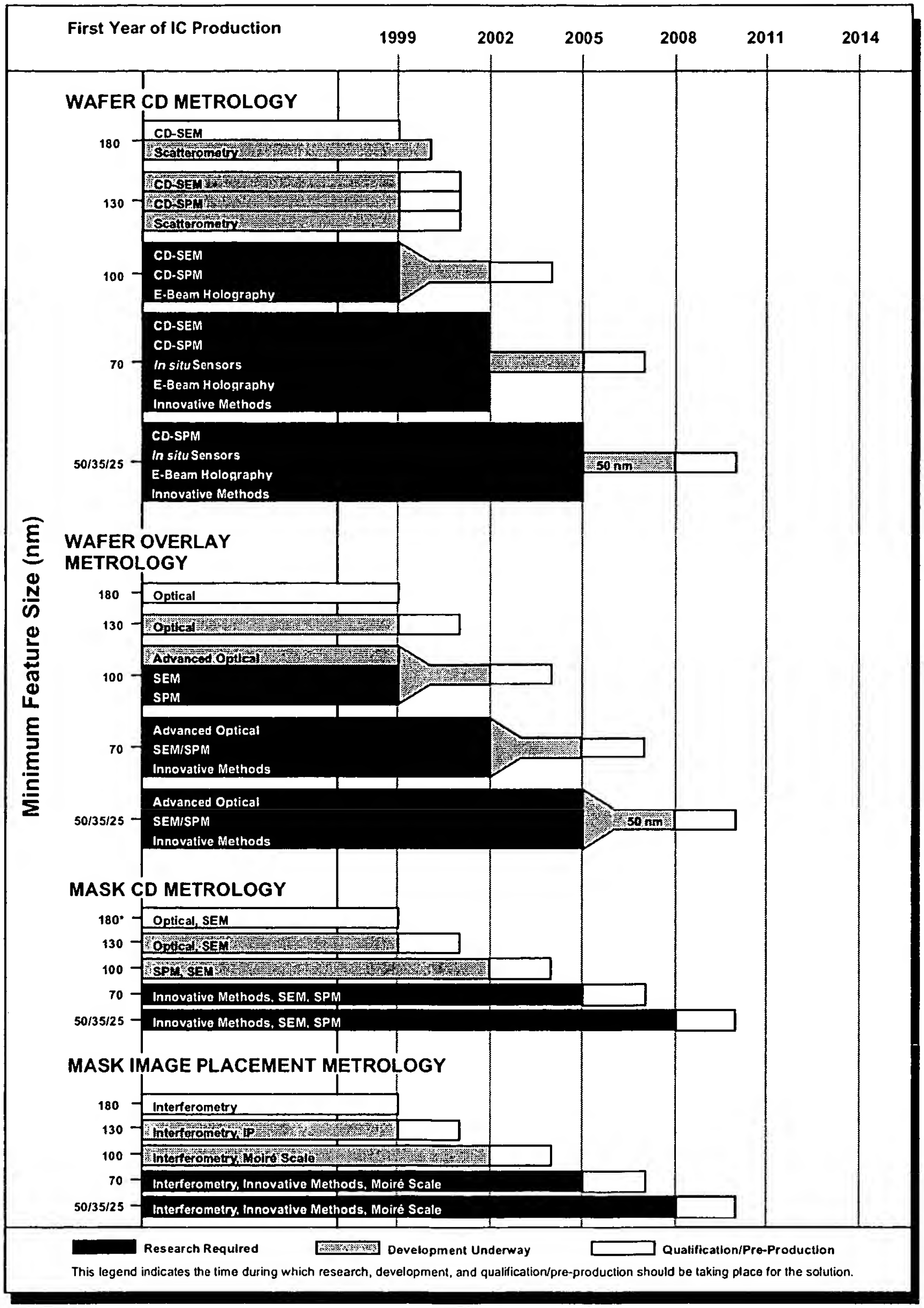

Figure 59 Lithography Metrology Potential Solutions

FRONT END PROCESSES METROLOGY

The accelerated introduction of new technology generations requires accelerated advancements of metrology for transistor development and fabrication. In this section the specific metrology needs for starting materials, surface preparation, thermal/thin films, doping technology, and front end plasma etch technologies are covered. Process integration issues such as the need to control leakage current and the reduction in threshold voltage and gate delay and their tolerances will interact with the reality of process control ranges for gate dielectric thickness, doping profiles, junctions, and doses to drive metrology needs. Modeling studies of manufacturing tolerances continue to be a critical tool for transistor metrology strategy. Metrology requirements for Front End Processes are shown in Table 84, and the Potential Solutions are shown in Figure 60.

Table 84a Front End Processes Metrology Technology Requirements—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
DRAM ½ Pitch	180	165	150	130	120	110	100	D½
MPU Gate Length	140	120	100	85	80	70	65	M Gate
Oxygen range (ASTM "79) in heavily doped substrates; measurement precision ± 0.5 ppma [A]	18–31	18–31	18–31	18–31	18–31	18–31	18–31	
Bulk control limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/cm^3)	1×10^{10}	$< 1 \times 10^{10}$	$< 1 \times 10^{10}$	$< 1 \times 10^{10}$	$< 1 \times 10^{10}$	$< 1 \times 10^{10}$	$< 1 \times 10^{10}$	
Bulk detection limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/cm^3)	1×10^{9}	$< 1 \times 10^{9}$	$< 1 \times 10^{9}$	$< 1 \times 10^{9}$	$< 1 \times 10^{9}$	$< 1 \times 10^{9}$	$< 1 \times 10^{9}$	
Logic dielectric equivalent thickness (nm) ± 3σ process range	1.9–2.5 ± 4%	1.9–2.5 ± 4%	1.5–1.9 ± 4%	1.5–1.9 ± 4%	1.5–1.9 ± 4%	1.2–1.5 ± 4%	1.0–1.5 ± 4%	M Gate
Logic dielectric measurement precision 3σ (nm) [B]	0.0075	0.0075	0.006	0.006	0.006	0.005	0.004	M Gate
DRAM capacitor structure dielectric material process control requirements (Dielectric constant) Equivalent oxide thickness (nm)	Cyl. MIS Ta_2O_5 (22) 3.0	Cyl. MIS Ta_2O_5 (22) 3.0	Cyl. MIS Ta_2O_5 (22) 3.0	Pedestal MIM Ta_2O_5 (50) 0.95	Pedestal MIM Ta_2O_5 (50) 0.95	Pedestal MIM Ta_2O_5 (50) 0.95	Pedestal MIM BST (250) 0.45	D½
DRAM capacitor dielectric physical thickness (nm) ± 3 σ process range	11.5 ±4%	11.5 ±4%	11.5 ±4%	12.2 ±4%	12.2 ±4%	12.2 ±4%	28.7 ±4%	D½
DRAM capacitor dielectric physical thickness measurement precision (nm 3σ) [C]	0.046	0.046	0.046	0.049	0.049	0.049	0.11	D½
2 and 3D dopant profile spatial resolution (nm)	3	3	3	2	2	2	1.5	
At-line dopant concentration precision (across concentration range) [D]	5%	5%	5%	4%	4%	4%	3%	

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 84b Front End Processes Metrology Technology Requirements—Long Term

YEAR *TECHNOLOGY NODE*	*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*	*Driver*
DRAM 1/2 Pitch	*70*	*50*	*35*	
MPU Gate Length	*45*	*32*	*22*	
Oxygen range (ASTM "79) in heavily doped substrates; measurement precision ± 0.5 ppma [A]	**18 – 31**	**18–31**	**18–31**	
Bulk control limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/cm^3)	**< 1 × 10^{10}**	**< 1 × 10^{10}**	**< 1 × 10^{10}**	
Bulk detection limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/cm^3)	**< 1 × 10^9**	**< 1 × 10^9**	**< 1 × 10^9**	
Logic dielectric equivalent thickness (nm) ± 3σ process range	**0.8–1.2** **± 4%**	**0.6–0.8** **± 4%**	**0.5–0.6** **± 4%**	*MPU*
Logic dielectric measurement precision 3σ (nm) [B]	**0.0032**	**0.0024**	**0.002**	*MPU*
DRAM capacitor structure dielectric material process control requirements (Dielectric constant) Equivalent oxide thickness (nm)	**Pedestal** **MIM** **epi-BST** **(700)** **0.15**	**Pedestal** **MIM** **???** **(1500)** **0.060**	**Pedestal** **MIM** **???** **(1500)** **0.043**	*D ½*
DRAM capacitor dielectric physical thickness (nm) ±3σ process range [C]	**27.2** **± 4%**	**23.0** **4%**	**16.4** **4%**	*D ½*
DRAM capacitor dielectric physical thickness measurement precision (nm 3σ)	**0.11**	**0.092**	**0.066**	*D ½*
2 and 3D dopant profile spatial resolution (nm)	**1**	**0.8–0.6**	**0.8–0.6**	
At-line dopant profile concentration precision (across concentration range) [D]	**2%**	**2%**	**2%**	

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Notes for Table 84 for Front End Processes Metrology Requirements

[A] IOC '88 value obtained by multiplying ASTM value by 0.65.

[B] Precision calculated from P/T=0.1=6xprecision/process range. The measurement requirements specify the equivalent thickness for a silicon dioxide dielectric film. It is expected that oxynitirides and stacked nitride/silicon dioxide layers will replace silicon dioxide for the 130 and 100 nm logic generations and that high dielectric constant materials such as Ta_2O_5 will be used at and after the 70 nm logic node and possibly at the 100 nm node. The physical thickness of the high dielectric constant layer can be calculated by multiplying the ratio of the dielectric constants ($\varepsilon_{high\ \kappa}/\varepsilon_{ox}$) by the effective oxide thickness. For example, a 6.4 nm thick Ta_2O_5 (κ= ~25) layer has a 1 nm equivalent oxide (κ=3.9) thickness. The listed precision is based on equivalent oxide thickness and must be multiplied by the ratio of the dielectric constant to obtain precision for the dielectric of interest. The total capacitance of the dielectric stack also includes that of the dielectric layer plus the interfacial layer, quantum state effects at the channel interface, and that associated with depletion of charge in the poly silicon gate electrode. Thus, the challenge to gate dielectric thickness measurement includes metrology for the interfacial layer.

[C] In the case of MIS structure, physical thickness, t_{diel}, is calculated using the equation of $t_{diel}=(t_{eq.ox}-1\ nm)_{diel}\,\varepsilon_{high\ \kappa}/3.9$ in which oxide film formed at the interface of poly-silicon and dielectric material in annealing is taken into account. In the case of MIM structure, t_{diel} is calculated using the equation of $t_{diel}=t_{eq.ox}\,\varepsilon_{high\ \kappa}/3.9$. Here $t_{eq.ox}$ is equivalent oxide thickness, and t_{diel} is dielectric constant of the dielectric material.

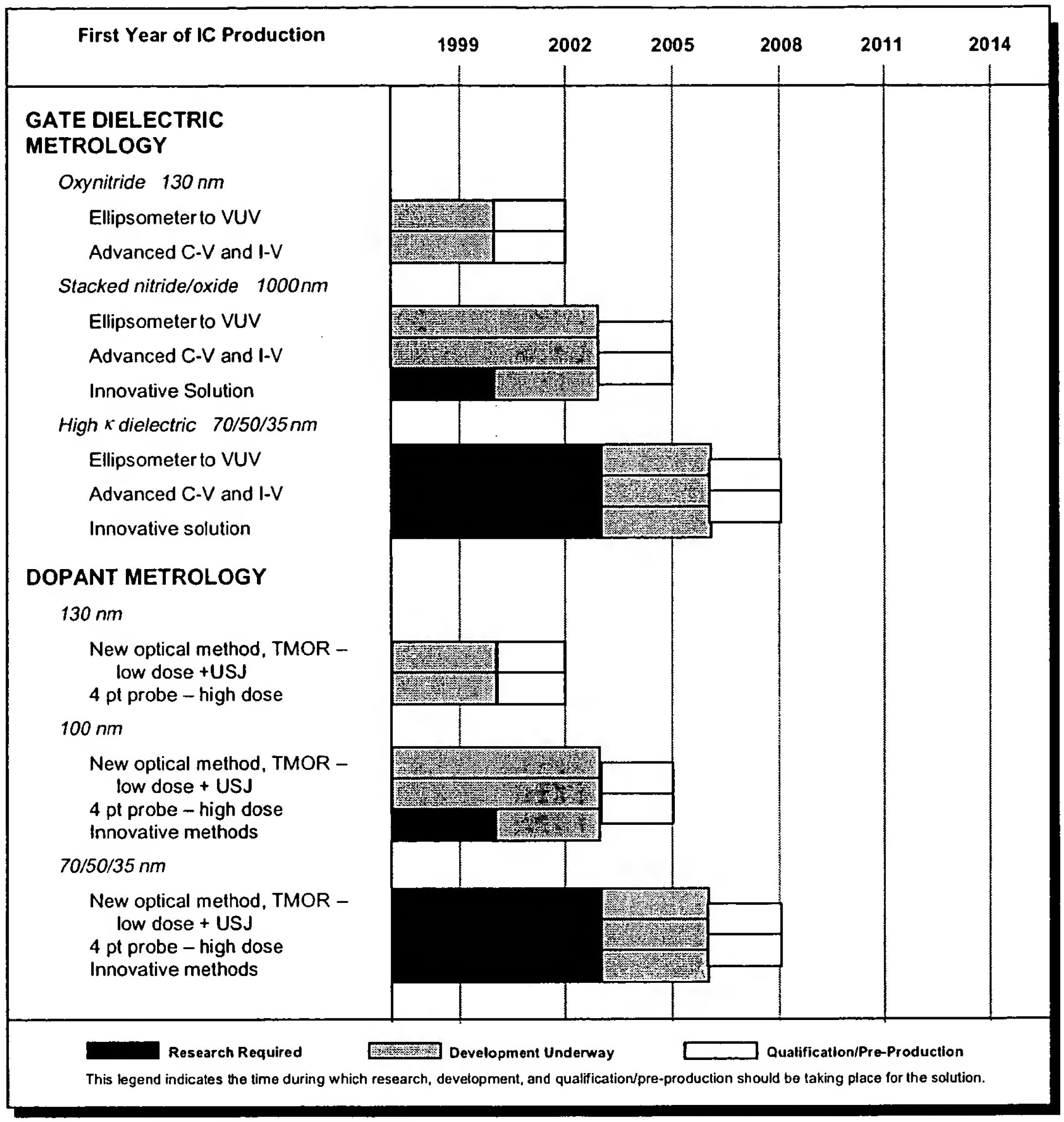
[D] High precision measurements with low systematic error are required.

Starting materials—Metrology continues to play an indispensable role in the cost-effective specification of polished, epitaxial and SOI silicon wafers to obtain optimal integrated circuit performance. Key metrology issues include (1) particle and surface defect detection, (2) reductions in edge exclusion, and (3) flatness. Gate oxide integrity (GOI) is becoming less of an issue as gate oxide thickness decreases. Improved tools are required to both size and distinguish different types of localized light scatterers, including particles and crystal originated pits. In addition, new methods may be required for detection and identification of LLSs less than 50–70 nm in size. Metrology for the measurement of wafer parameters within 2 mm of the wafer edge is a significant challenge. A key issue addresses the beam or critical probe size in relation to the wafer edge exclusion region; that is, what is the required degree of overlap to ensure a meaningful measurement. Lithography continues to be the gateway for the successful fabrication of ICs. Standardized metrology for measuring the site flatness under scanning stepper conditions is required for meaningful characterization of the wafer in order to ensure sufficient quality during subsequent patterning operations.

Surface preparation—*In situ* sensors for particles, chemical composition, and possibly for trace metallics are being introduced to some wet chemical cleaning tools. Particle detection is covered in the *Defect Reduction* chapter. Particle/defect and metallic/organic contamination analyses are covered in the Materials Characterization Section of the *Metrology* chapter.

Thermal/thin films—New high κ transistor and capacitor dielectrics, new gate electrode materials, and new process flows require materials and electrical characterization and inline metrology development. Near term metrology development will focus on extension of ellipsometry and electrical (capacitance–voltage and current–voltage) methods to sub 2 nm oxides and nitrogen containing oxides. Potential solutions include ellipsometry in the ultra-violet wavelength range. Methods capable of characterizing and providing inline metrology for interface layers are required. Continued development and standardization of electrical testing at high frequencies and new methods for dielectric reliability testing are required. There is considerable evidence that the dielectric properties of transistor and capacitor dielectric films after deposition are different from those subsequent to thermal processing. Although this complicates comparison of electrical and physical methods, correlation must improve.

Doping technology—Improved inline process measurements to control active dopant implants is required beyond 180 nm. Presently, 4-point probe measurement is used for high dose implant and thermally modulated optical reflectance is used for low-dose implant process control. Both methods need improvement, and a new method is needed that provides a direct *in situ* measurement of dose, dopant profile, and dose uniformity. Use of inline X-ray fluorescence for control of high dose B, P, and As implants has been reported. Offline secondary ion mass spectrometry has been shown to provide the needed precision for current technology generations including ultra-shallow junctions. The range of applicability and capability of new, non-destructive measurement methods such as carrier illumination (an optical technology) and impulsive stimulated thermal scattering (an acoustic wave technology) are under evaluation. Two- and preferably three-dimensional profiling is essential for achieving future technology generations. Activated dopant profiles and related TCAD modeling and defect profiles are necessary for developing new doping technology.



TMOR—thermally modulated optical reflectance
USJ—ultra shallow junctions

Figure 60 Front End Processes Metrology Potential Solutions

INTERCONNECT METROLOGY

The accelerated reduction in feature size along with copper, new dielectrics (such as low κ), and damascene structures will greatly challenge metrology for on-chip interconnect development and manufacture. Development of interconnect tools, processes, and pilot line fabrication all require detailed characterization of patterned and unpatterned films. Currently, many of the inline measurements for interconnect structures are made on monitor wafers (unpatterned), or rely on destructive techniques. Small feature sizes including ultra-thin barrier layers will continue to stretch current capabilities. Critical dimension measurements must be extended to very high aspect ratio structures made from dielectric materials. Interconnect metrology development will continue to be challenged by the need to provide physical measurements that correlate to electrical performance, yield, and reliability. More efficient and cost-effective manufacturing

metrology requires measurement on patterned wafers. Metrology requirements for Interconnect are shown in Table 85 and the potential solutions are shown in Figure 61 below.

Table 85a Interconnect Metrology Technology Requirements—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	20005 100 nm	DRIVER
DRAM 1/2 Pitch	180	165	150	130	120	110	100	
MPU Gate Length	140	120	100	85	80	70	65	
Planarity requirements: lithography field (mm × mm) for minimum interconnect CD (nm) Measurement precision (nm)	25 × 32 250 ± 25	250	250	25 × 36 200 ±20	200	200	25 × 40 175 ±17	MPU
Measurement of deposited barrier layer at thickness (nm) / process range (± 3σ) precision 1σ (nm) for P/T=0.1 Require profile characterization on patterned wafers [A]	17/10% <0.06	16/10% 0.05	14/10% <0.05	13/10% 0.04	12/10% 0.04	11/10% <0.04	10/10% 0.03	MPU
Measurement of reactive barrier layer thickness and uniformity for thickness (nm)								
Measure interlevel metal insulator effective dielectric constant (κ) and anisotropy on patterned structures at 5× to 10× local clock frequency (GHz) [B]	3.5–4 .0 1.25	3.5–4 .0	2.7–3 .0	2.7 – 3.0 2.1	2.2–2.7	2.2–2.6	1.6–2.2 3.5	MPU

Table 85b Interconnect Metrology Technology Requirements—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
Planarity requirements: lithography field (mm × mm)/ planarity for minimum interconnect CD (nm) / measurement precision	25 × 44 175 ±17	25 × 52 175 ±17	175 ±17	MPU
Measurement of deposited barrier layer at Thickness (nm) / process range (± 3σ) Precision 1σ (nm) for P/T=0.1 Require profile characterization on patterned wafers [A]	0	0		MPU
Measurement of reactive barrier layer thickness and uniformity for thickness (nm)	1	1	1	MPU
Measure interlevel metal insulator effective dielectric constant (κ) and anisotropy on patterned structures at 5× to 10× clock frequency (GHz) [B]	< 1.5 6	< 1.5 10	< 1.5 17	MPU

Notes for Table 85 for Interconnect Metrology Requirements

[A] Roadmap predicts barrier for 35 nm technology node will be formed by reactive processes in metal or dielectric or both instead of by deposition.

[B] Minimum effective dielectric constant is listed. Due to divergence of DRAM and logic requirements, minimum listed number is associated with logic requirements. The development of a measurement technique for low κ dielectric constant and anisotropy is nearly complete up to 40 GHz. Technology transfer to industry will take place from 1999 to 2000.

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

The wide set of new interconnect materials and processes require metrology method advancement and new measurement technology. Time-to-market considerations will require better and faster measurements during pilot line and early production to compensate for immature processing. A better approach would be to have metrology available for characterization in the development stage so that robust processes are transferred to production. Interconnect specific CD measurement procedures must be further developed. With the introduction of Damascene structures, metrology becomes more difficult because both depth and width measurements of high aspect ratio trenches/vias are needed. In addition, the presence of dielectric layer material may introduce charging problems. Rapid imaging of contact or via bottoms, or determining sidewall slopes are also beyond current microscopy capabilities.

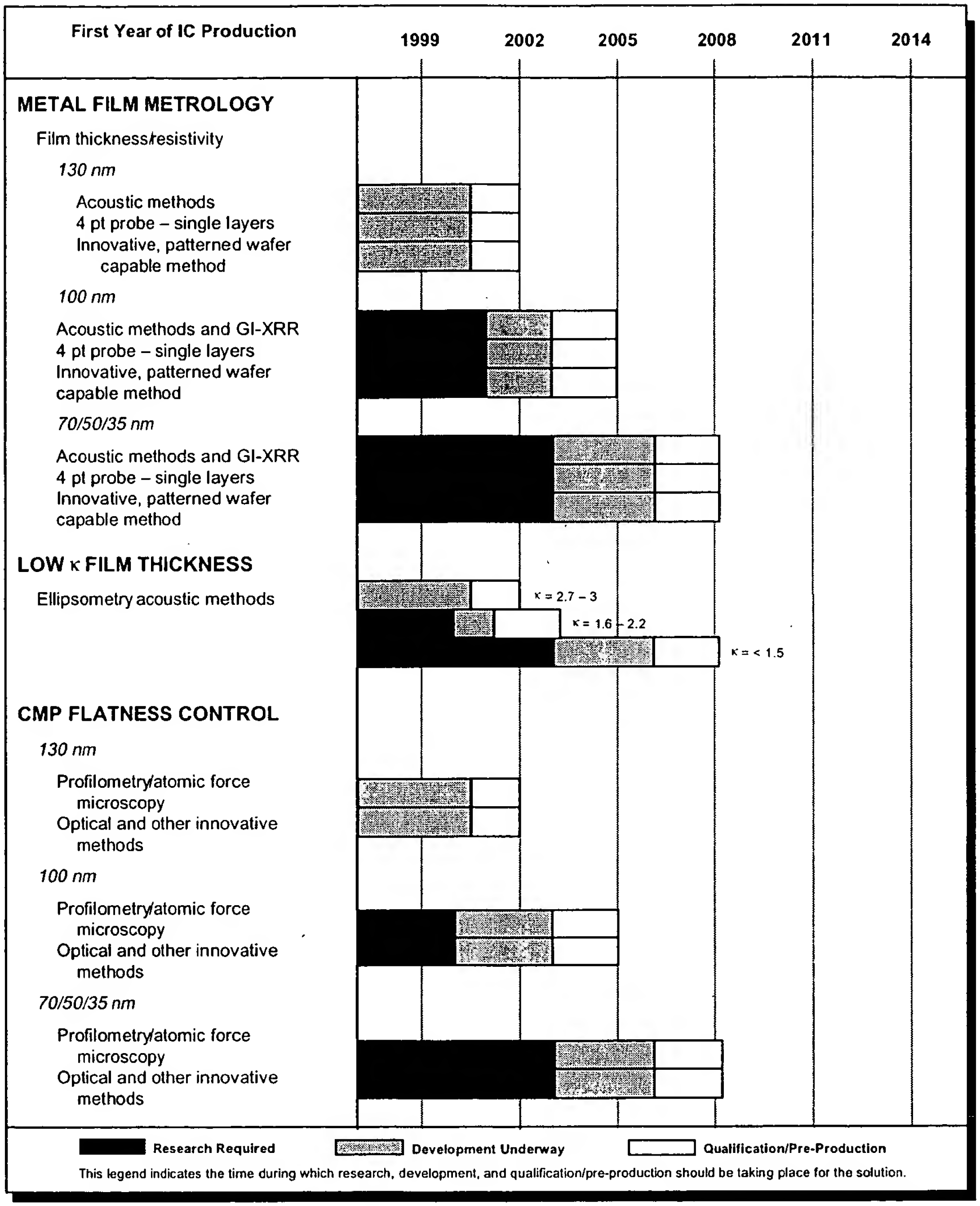
Interconnect technical requirements indicate that barrier layers for future technology will be <6 nm thick. If a process window of 20% total thickness variation is assumed, then measurement precision (6σ) must be ≤0.12 nm that is beyond current capabilities. High frequency measurement of *low* κ materials and test structures has been developed up to 40 GHz. Equipment, procedures, and test structures materials that account for clock harmonics, skin effects, cross-talk, and anisotropy of materials need to be reduced to practice and applied to *low κ* interconnect

Chemical mechanical polishing technology is outstripping flatness metrology capabilities for patterned wafers. Stylus profilers and scanned probe (atomic force) microscopes can provide local and global flatness information, but the throughput of these methods must be improved. Standards organizations are developing flatness tests that provide the information required for statistical process control that is useful for lithographic processing. Other areas of metrological concern with the new materials and architectures include in-film moisture content, film stoichiometry, mechanical strength/rigidity, local stress (versus wafer stress), and line resistivity (versus bulk resistivity). In addition, calibration techniques and standards need to be developed in parallel with metrology.

Interconnect structures, which involve many layers of widely varying thickness made from a variety of material types, pose the most severe challenge to rapid, spatially resolved (for product wafers) multilayer thickness measurements. Current film thickness methods such X-ray fluorescence, optical reflectivity, ellipsometry, profilometry, and microbalance do not meet this goal. New methods for measuring multiple film layers in production using laser stimulation of acoustic and thermal waves at this time require test structures in the scribe region between chips.

CRITICAL INTERCONNECT MEASUREMENT NEEDS SUMMARY

Design of interconnect structures requires measurement of the high frequency dielectric constant of low κ materials. High frequency testing of interconnect structures must characterize the effects of clock harmonics (5× to 10× base frequency), skin effects, and crosstalk. Other metrology needs include measuring resistivity (sheet resistance) at high frequency, adhesion, and mechanical strength. Also needed are imaging of high aspect ratio structures for process control, and endpoint for CMP, including damascene/copper processes.



GI-XRR—grazing incidence X-ray reflectivity

Figure 61 Interconnect Metrology Potential Solutions

MATERIALS AND CONTAMINATION CHARACTERIZATION

Materials characterization methods are both challenged by the rapid introduction of new materials and required to provide critical information on physical and electrical properties. Correlation of appropriate offline characterization methods with each other and with inline physical and electrical methods should be

accelerated. Use of characterization methods to provide more accurate information such as layer thickness or elemental concentration will continue. Characterization methods will continue to move toward whole wafer measurement capability and clean room compatibility.

Often, offline methods provide information that inline methods cannot. For example, transmission electron microscopy (TWM)and scanning TEM, especially those capable of annular dark field imaging, provide the highest spatial or cross-sectional characterization of ultra thin films and interfacial layers. ADF-STEM systems equipped with X-ray detection and electron energy loss instrumentation have provided new information about interface chemical bonding. Grazing incidence X-ray reflectivity provides measurement of thin film thickness and density. Grazing incidence X-ray diffraction provides information about the crystalline texture of thin films. Recent laser development has allowed spectroscopic optical second harmonic generation (SOSG) characterization of the optical properties of the interface between a dielectric and substrate not previously possible. One example of the power of SOSG is the observation of interfacial states between silicon and silicon dioxide not observed by spectroscopic ellipsometry in the same wavelength range. Offline characterization of physical properties such as void content and size in porous *low* κ insulators, film adhesion, and mechanical properties, for example, is required for evaluation of new materials.

Promising new technology such as high energy resolution X-ray detectors must be rapidly commercialized. Prototype microcalorimeter energy dispersive spectrometers (EDS) and superconducting tunnel junction techniques have X-ray energy resolution capable of separating overlapping peaks and providing chemical information. These advances over traditional EDS and some wavelength dispersive spectrometers can enable particle and defect analysis on SEMs located in the clean room.

The trend toward equipping appropriate characterization tools with wafer capable sample stages continues. Whole wafer Auger (thin film, particle and defect analysis) and several types of SIMS (thin film, dopant, organic and metallic surface contamination and particle and defect analysis) tools are commercially available. Roadmap needs include improved imaging and analysis resolution. Several other methods are used for surface contamination analysis including total reflection X-ray fluorescence and surface collection by vapor phase decomposition (VPD) followed by inductively coupled plasma mass spectrometry (ICP-MS). Improved automation and detection limits are required.

REFERENCE MATERIALS

Reference materials are physical objects with one or more well established properties used to calibrate metrology instruments. Reference materials are a critical part of metrology since they establish a "yard stick" for comparison of data taken by different methods, by similar tools at different locations (internally or externally), or between model and experiment. Reference materials can be obtained from a variety of sources and come in a variety of forms and grades. Depending on the source, they may be called certified reference materials (CRM), consensus reference materials, NIST Traceable Reference Materials (NTRM®), or Standard Reference Materials (SRM®).

NIST has maintained its position as one of the leading internationally acceptable national authorities of measurement science in the semiconductor industry. NIST has also recognized the difficulty of keeping pace with the IC industry through the traditional method of need identification, instrumentation and technique development, and the development of SRMs. Several approaches allow the industry to supplement NIST's ability to supply reference materials. Commercial suppliers can submit calibration artifacts to a rigorous measurement program at NIST for the purpose of developing an NTRM; reference material producers adhering to these requirements are allowed to use the NTRM trademark. A second approach, which has been growing in application, is the accreditation of commercial laboratories by NIST through the National Voluntary Laboratory Accreditation Program (NVLAP). A third approach is the development of consensus reference materials through interlaboratory testing under the supervision of recognized standards developing bodies, such as ASTM.

There are several technical requirements related to reference materials and certification, as follows:

- Reference materials must have properties that remain stable during use; both spatial and temporal variations in the certified material properties must be smaller than the desired calibration uncertainty.
- Reference materials may be difficult to manufacture with the desired attributes; frequently it is necessary to use specialized manufacturing techniques in short runs to obtain the samples to be measured and certified.
- Measurement and certification of reference materials must be carried out using standardized or well-documented test procedures. In some areas of metrology no current method of measurement is adequate for the purpose. When the basic measurement process has not been proven, reference materials cannot be produced.
- Uncertainties in the certified value of the reference material must be less than 1/4 of the variability of the manufacturing process to be evaluated or controlled by the instrument calibrated using the reference material.
- For applications where accurate measurements are required (such as dopant profiling to provide inputs for modeling), the reference material attribute must be determined with an accuracy better than 1/4 of the requirement; accuracy includes both bias and variability considerations.
- Additional training of process engineers in the field of measurement science is essential to avoid misuse of reference materials and misinterpretation of the results obtained with their use.

It is critically important to have suitable reference materials available when a measurement is first applied to a technology generation, especially during early materials and process tool development. Each type of reference material has its own set of difficult challenges, involving different combinations of the challenges described above.

METROLOGY INTEGRATION

As wafer size increases and required measurement resolution shrinks, both data volumes and data rates will increase dramatically. This raw data must be converted into useful information to facilitate process control and defect reduction. To accomplish this, metrology data must be integrated into factory and enterprise-level information systems so that it may be associated both with other data and with wafer tracking information.

The manner in which metrology integration occurs will be greatly influenced by the implementation of advances in technology. These include (1) introduction of advanced proximity correction and phase-shift mask technology; (2) the ramp of 193 nm, 157 nm, and next-generation lithography; (3) integration of copper and low κ interconnect processes; and (4) the shift from 200 mm to 300 mm wafers in high-volume production.

For example, CD and defect data on the reticle must be compared with CD and defect data on the wafer. This requires efficient communication between the mask supplier, pilot line, and high-volume factories. Also, bare-wafer nanotopography and defect data must be compared with yield losses on device wafers, requiring an information link between silicon suppliers and their customers. In addition, metrology in one factory must be linked to other factories producing the same device, most of which will use "copy exactly," "copy intelligently," or "wafer-state matching" strategies.

At the factory level, physical, electrical, and parametric defects found with inspection tools must be correlated with data from other inspection tools and blended seamlessly with physical parametric data from metrology tools.

One form of metrology integration is found in advanced process control (APC). APC applies model-based process control to reduce process variation, reduce send-ahead and tool monitor wafers, shorten learning cycles and response-times, enable better tool matching in high-volume production, improve overall equipment effectiveness, shorten development times, and ease process transfer from pilot line to factory.

PACKAGING METROLOGY

Assembly and Packaging will continue to play a significant and increasing role in the size, performance and cost of future electronic systems. This section summarizes the metrology challenges associated with assembly and packaging. This is not an exhaustive summary, but rather attempts to highlight the most critical areas of interest.

Current technology status and the needs for coordinated electrical modeling and simulation tools for chip, package and system—A set of chips is packaged individually or collectively in single or multi-chip packages. Modeling the electrical behavior of these chips and packages in the overall system environment pushes the limits of what can be done in a cost and time effective manner. Parameter extraction of three dimensional interconnect and power delivery structures and the detailed validation of these parameters and their effect on circuit performance requires further development including coupling between components, mixed signal simulation, power disturbances and EMI. Efficient simulation tools are needed for the overall system.

Accelerated failure test methods representative of the application—Temperature cycling, chemical exposure, and shock and vibration are techniques that are used to accelerate the onset of failures with a view to validate the failure mechanism, and to qualify and improve the lifetime and successful operation of the product. We need to continue to ensure through test, measurement and modeling, that these acceleration methods lead to the same kinds of failures that are found in the product in its daily usage.

Measurement and modeling of interfaces—The performance, reliability, and cost of assembly and packaging are driven by our understanding of interfaces, and our ability to measure and control them. For examples, the interfacial behavior of the die attach materials, mold compounds, encapsulations, adhesives, underfills, and thermal compounds are important issues. Our ability to accurately measure and predict interface performance will remain a key to future cost effective developments.

Refinement and validation of thermal and mechanical simulation models of packages and assemblies—We continue to push the cooling and mechanical limits of electronic products. Complete thermal and mechanical modeling, validated with measurements, is needed. This includes flow characteristics, interfacial properties, fracture mechanics, and the thermo-mechanical behavior of packages and assemblies. The validation also highlights the need for better systems and measurement techniques to locate and measure properties, defects and failures.

Material parameters—The measurement, collection and dissemination of the fundamental properties, for example, sizes, thicknesses, and temperatures of interest, of packaging materials requires constant improvement. They will also include thermal conductivity, electrical conductivity, dielectric constant and loss factor, stress/strain functions, specific heat, and micromechanical and dimensional stability over the temperature and stress ranges relevant to the application.

Material application control—The application of solders, solder alternatives, underfills, encapsulants, attachment materials, and others in the manufacture of packages and bumped chips continues to push the limits in many areas. They may include the quantity control, quality control, thickness, uniformity, voiding, thermal, and electrical and mechanical properties. Refinement in the online measurement of these parameters is needed to replace inspection, reduce process variation, control defects, and reduce waste.

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS 1999 EDITION

MODELING AND SIMULATION

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MODELING & SIMULATION

SCOPE

Modeling and Simulation can play a critical role in overcoming Difficult Challenges for future technology nodes; thus, the Difficult Challenges of the other technology working groups are the key drivers for the Modeling and Simulation area. The following topical areas are included in the scope of this chapter: 1) *Equipment/topography modeling*—hierarchy of models including the physical environment, conditions, and processes affecting the wafer; 2) *Lithography modeling*—modeling of the lithography equipment, and photoresist processing; 3) *Front End Process modeling*—the simulation of the physical effects of manufacturing steps used to build transistors up to metallization, but excluding patterning; 4) *Device modeling (numerical)*—hierarchy of physically based models for active devices and interconnect; 5) *Circuit element modeling*—compact models for active, passive, and parasitic circuit components as well as parameter extraction; 6) *Package modeling*—electrical, mechanical, and thermal modeling; and 7) *Numerical methods*—grid generators, matrix solvers, parallel algorithms, and surface-advancement techniques.

The "suppliers" of Modeling and Simulation capability include CAD vendors, universities, and researchers at government funded laboratories. While a substantial amount of modeling effort takes place inside the semiconductor companies, new modeling capability requires long-range research that is best accomplished in an academic or laboratory setting. For this reason, a healthy university research effort is a prerequisite for success in the modeling area. It is vital that adequate research funds be made available in a timely manner in order to address the industry's future critical needs.

DIFFICULT CHALLENGES

The difficult challenges in Table 86 are those areas within the scope of Modeling and Simulation that can make the greatest contribution toward solving the difficult challenges of the other technical working groups.

High frequency circuit modeling is a growing challenge as clock speeds continue to increase. Chief among the issues are accurate modeling of interconnect parasitics. Techniques are needed for efficient simulation of full-chip interconnect delay. Accurate models for 2D and 3D interconnect extraction from layout are a continuing need. The ability to deal with on-chip transmission lines and inductance effects is an increasing requirement. For high frequency modeling, comprehending the gate transmission line effect is important, as is the impact of substrate noise. Improvements in the transistor models in order to treat non-quasi-static effects and quantum mechanical gate effects are also an important challenge.

Table 86 Modeling and Simulation Difficult Challenges

DIFFICULT CHALLENGES ≥100 nm / THROUGH 2005	SUMMARY OF ISSUES
High frequency circuit modeling (>1GHz)	Efficient simulation of full-chip interconnect delay High frequency circuit models including non-quasi-static, gate RLC, substrate noise, QM effects Accurate 3D interconnect model; inductance effects
Modeling of ultra-shallow junctions	Diffusion parameters (such as from first principles calculations) for As, B, P, Sb, In, Ge Interface effects on point defects and dopants Activation models (In, As, B); metastable states Implant damage, amorphization, re-crystallization
Unified package/die-level models	Unified package/chip-level circuit models Integrated treatment of thermal, mechanical, electrical effects
Model thin film and etch variation across chip/wafer (Equipment/topography)	Reaction paths and rate constants; reduced models for complex chemistry Plasma models; linked equipment/feature models CMP (full wafer and chip level) Pattern dependent effects
Model alternative lithography technologies	Resolution enhancement; mask synthesis (OPC, PSM) Predictive resist models 248 versus 193 versus 157 evaluation and tradeoffs Next-generation lithography system models
Reliability models for circuit design and technology development	Circuit and device level transistor reliability: oxide TDDB, hot carrier, electromigration, NVM reliability, SER, ESD, latch-up
Model new interconnect materials and interfaces	Electromigration (physical), grain structure, diffusion barriers, metallurgy, low κ dielectric materials
DIFFICULT CHALLENGES <100 nm / BEYOND 2005	SUMMARY OF ISSUES
Gate stack models for ultra-thin dielectrics	Electrical and processing models for alternate gate dielectrics, and alternate gate materials (such as metal) Model epsilon, surface states, reliability, breakdown and tunneling from process conditions
Nano-scale device modeling	New device concepts (using quantum effect) beyond traditional MOS; single electron transistors, effect of single dopants, etc.
Atomistic process modeling	Accurate atomic scale models for process integration

The *modeling of ultra-shallow junctions* is a major concern, as low-resistance source/drain extensions are necessary for future high-performance devices. Thermal budgets have been reduced so much that profiles are dominated by damage, transient, and interface effects. Obtaining parameters for diffusion and reaction kinetics is a key challenge to allow greater understanding of the processes, especially for new dopants and materials. Modeling activation is key to achieving higher doping levels, and may lead to achievement of "metastable" dopant activation (higher than equilibrium activation). More detailed understanding of implant damage, amorphization and subsequent re-crystallization during anneal is important, as these phenomena can critically affect dopant profiles. Dopant and defect metrology are critical to the development and calibration of models for profile evolution. Accurate tools do not exist for dimensional (1D, 2D, or 3D) characterization of sub-100 nm technology.

A system for *unified package-chip modeling* is needed to analyze a number of new issues arising in the interactions of new, complex packaging approaches. Developments in chip size, packaging techniques, power dissipation, and switching speed require new simulation tools that treat thermal, mechanical, and electrical effects self-consistently. Seamless modeling of interconnects from chip to package to board level is needed.

The *modeling of thin film and etch variation* across the wafer and chip is an important first step towards better controlling those variations. Equipment and topography modeling is limited by lack of knowledge of the physical and chemical processes (such as chemical vapor deposition [CVD], plasma etch, chemical mechanical planarization [CMP]), so that obtaining greater information on reaction paths and rate constants is essential. The development of reduced chemistry models with only the primary mechanisms necessary for practical applications is an important challenge. Reactor and process design drive the linking of equipment modeling with topography modeling. The proliferation of CMP increases the need for CMP models. Modeling methods that address pattern dependencies directly from layout are needed.

Modeling of alternative lithography technologies becomes increasingly important in the coming generations as the number of wavelengths and the number of available resolution enhancement techniques increases. Creation of improved modeling approaches for OPC and PSM mask synthesis is an important challenge. Developing predictive resist models is a continuing challenge, but would greatly expand the application area of lithography modeling. As decisions are nearing on the selection of a next-generation lithography tool (beyond optical), the development of comprehensive modeling tools are needed to understand the tradeoffs between the different approaches.

Reliability models for circuit design and technology development will take on an increased importance as new reliability issues arise at small dimensions; reliability guard bands must be reduced for improved performance. More detailed modeling of SER and ESD phenomena will be of increasing importance.

Modeling new interconnect materials and interfaces is necessary due to the rapid introduction of new materials into the interconnect system, and the resulting reliability concerns. Modeling and simulation technology needs to provide 3D simulation tools that accurately describe the physical structure and properties of interconnect patterns. New materials and mechanisms (such as Cu diffusion through barrier layers into the dielectrics, mechanical stability of low κ dielectrics) and the reliability of interconnect systems (electromigration, stress) are of concern. Tools are needed to better model grain morphology and evolution during processing and during normal operation.

Gate stack models for ultra-thin dielectrics are needed in order to help optimize very thin conventional dielectrics, as well as to help in the search for alternative dielectric and gate electrode materials. This challenge encompasses the development of a new generation of process modeling tools to help engineer dielectrics on an atomic scale. Furthermore, more detailed quantum modeling of the electrical behavior of the gate stack is necessary as the thickness approaches a few atomic layers. Fundamental understanding of process impact on the effective dielectric constant epsilon, surface states, reliability and tunneling could play an important role in developing future high-performance MOS devices.

As traditional MOS scaling becomes less effective, *nano-scale device modeling* will be needed to help develop innovative MOS devices as well as to understand the limits of the MOS device. Modeling is also needed to explore new device structures that may operate on principles different than the MOS device. In this regime, non-equilibrium effects will heavily influence carrier transport. Towards the 50 nm node, full or hybrid quantum descriptions in 2D/3D will be needed. Research on such techniques needs to start very early because a long lead time is anticipated.

Atomistic process modeling will be needed at the far end of the Roadmap. Regardless of the particular technology direction, it is assumed that the ability to manipulate and control materials to atomic layer tolerances will be required.

TECHNOLOGY REQUIREMENTS AND POTENTIAL SOLUTIONS

Modeling and simulation encompasses a variety of applications with widely varying requirements. For example, in applications closely associated with design, speed and accuracy of phenomenological models are the primary requirement, while predictivity in uncalibrated regimes is secondary. Examples are circuit modeling and the lithography models built into OPC systems. In applications associated with technology

development, the requirement may be considered to be a mixture of physically based models and characterized empirical models. Traditional TCAD applications when used to optimize technology development (using highly characterized simulators) fit this description. Finally, there are modeling areas in which the basic physics are being explored. Examples are Monte Carlo device simulators, or first principles calculations of diffusion parameters for dopant diffusion in silicon. To give useful guidance for all these application areas, the Technology Requirements tables for Modeling and Simulation have been divided into tables for simulation "Capabilities" and tables for "Accuracy and Speed." Refer to Table 87a, b, and c.

The "Capabilities" requirements table is meant to describe the technology requirements for modeling and simulation that demand that new areas of modeling be developed. An example would be the capability to model EUV lithography steppers. In this case, the basic ability to simulate the performance of an EUV stepper needs to be developed. This type of requirement is often tied either to the introduction of new technologies, or to new regimes of physical phenomena at smaller dimension.

In contrast, the "Accuracy and Speed" requirements table more properly describes the level of simulator accuracy needed for process/circuit design or optimization. For TCAD applications, this level of accuracy is needed to achieve the overall TCAD cost reduction goals listed in the first row of the table. The cost reduction goal should be interpreted more generally as a cost and development time reduction, as it is understood that TCAD should speed the process development schedule. For ECAD and design applications, these are the accuracy levels needed for designers to effectively create new products. Note that accuracy requirements are specified only for the short-term technology requirements; for the long term, investigation of new technologies is the overall priority. It should be recognized that at a given point in time, several technology generations are being simulated in parallel, with differing accuracy requirements for each.

It should be noted that the accuracy requirements in Table 87b refer to accuracies obtained after calibration of the simulation tools to a particular technology node. It is generally understood that for TCAD simulation tools in particular, calibration is required for each technology node because new technologies, materials, dopant species, and process regimes are introduced in each node. The accuracy numbers were determined by questioning a sample of process development and design engineers.

Table 87a Modeling and Simulation Technology Requirements: Capabilities—Near Term

YEAR TECHNOLOGY NODE	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*
Equipment/Topography							
Equipment simulation	—	**Gate stack and interconnect uniformity models**			**Effect of processing conditions on material properties**		
Equipment/feature scale link	—	**Plasma etch: feature/equipment model**			**Within-chip feature variation**		
Lithography							
Lithography: evaluate wavelength	—	**Evaluate 248 nm versus 193 nm**			**Evaluate 193 nm versus 157 nm**		
Resist models	—	**193, 157 nm resist models**			**Detailed chemical resist developent model**		
Front End Process Modeling							
Gate Stack: evaluate materials	—	**Model alternate dielectrics**			**Model metal versus poly gate**		
Diffusion and activation coefficients	—	**Kinetics of diffusion and activation**			**Interface interactions with point defects and dopants**		
Stress/extended defects	—	**Front end stress model**			**Extended defects and disloactions**		
Device Modeling (Numerical)							
Gate stack models	—	**Gate current tunneling models**			**Full quantum gate stack models**		
Reliability models	—	**Transistor reliability models (gate oxide)**			**Interconnect reliability models (electromigration, stress)**		
Noise/variation	—	**Dopant fluctuation**			**Noise models**		
Circuit Element Modeling/ECAD							
New circuit element models	—	**SOI circuit model**			**Gate tunneling current**		
Interconnect models	—	**Full-chip RLC**			**On-chip Inductance effects**		
System-on-a-chip	—	**Unified analog/digital**			**DRAM/Flash/embedded memory models**		
Package Modeling							
Package models	—	**Complex interconnect geometries; multiple power and ground planes**			**Thermo-mechanical models**		
Unified package/chip models	—	**Unified package/chip circuit models**			**Unified RLC extraction for package/chip**		
Numerics							
Numerical algorithms	—	**Robust, reliable 3D grid generation**			**Highly efficient optimization algorithms**		

This table is meant to outline new capability requirements needed for future technology nodes; the column for the 180 nm node (1999) is blank only because the development of this technology is basically complete. Furthermore, if the development of capabilities specified for later nodes could be accelerated, they would in most cases be helpful for earlier technology nodes.

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

EQUIPMENT/TOPOGRAPHY MODELING

The key driver for accurate equipment/feature scale modeling and simulation software tools is the need to obtain knowledge and insight that will reduce development cycle times and costs. Enablers for equipment modeling are materials and process simulation tools, equipment to feature scale simulation capabilities (including equipment-feature integration), process control, and sensor design.

The equipment/topography modeling area can be subdivided into several unit process areas: CMP, plating, thermal and RTP, plasma processing, CVD, PVD, and etch. The requirements vary per application and per process being considered (such as thermal, deposition, etch). Thus, the metrics in Table 87b express accuracy requirements as a percent of specification limits or metrology capabilities. Models ranging from easy-to-use to complex, from fast executing to computationally intensive, and from high accuracy in a constrained process space to moderately predictive over wide range should be available to satisfy all uses. As the application moves from equipment understanding toward process integration, the need for linkage between equipment models and wafer/feature scale and atomistic models becomes stronger.

Although the models are becoming increasingly predictive, validation is still critical before results obtained from simulations will be considered. As a bare minimum, equipment and topography models must be able to predict trends correctly (correct sign and order of magnitude) to be useful.

Fundamental reaction mechanisms and rate constants (both gas/plasma and surface) are key to properly capturing the physics and chemistry of surface evolution during thin film etching or deposition. Both experimental and computational methods are needed to obtain these mechanisms and rate constants. A hierarchy of computational approaches from atomistic (molecular dynamics, Monte Carlo, quantum chemistry) to continuum must be employed (see *Materials* section in this chapter for more discussion). Providing integrated equipment and feature-scale simulation remains a great challenge as the fluxes from the reactor determine the boundary conditions for the feature scale and vice versa. Understanding derived from both the equipment and feature scale areas is also needed for modeling pattern dependent variation.

More work is needed on linking these equipment/feature scales simulation tools with the modeling of the reliability of the interconnect system, including the effects of electromigration, thermo-mechanical stress, and diffusion through barrier layers. Ultimately, this requires greater understanding of microstructure (grain formation and evolution) and thin film material properties that differ from those of the bulk.

An important future application of equipment modeling is the control of manufacturing equipment based on real time simulators including sensor design and simulation. Sensor design includes determination of what to measure, where to locate the sensor, as well as creation of "soft sensors," such as the use of a model to predict a quantity of interest from available measurements.

The potential solutions for equipment/topography modeling have been divided into five categories:

1. *Rates*—The understanding of semiconductor processes is improving, and the advance of computer capability is allowing one to solve large and difficult problems more effectively. However, chemical kinetics of bulk and surface reactions needs attention. These input parameters to the simulation codes are many times the weak link in being able to accurately predict results. Experimental determination or quantum chemistry methodologies for calculating these needed parameters would provide potential solutions.

   In addition, many times the complex chemistries can be reduced to a reduced model requiring only a few equations—thus allowing faster results and better insight into the driving mechanisms.

2. *Reactor modeling*—Plasma modeling and simulation is one of the more difficult unit process simulation areas. Accurate plasma models, the link of these gas phase models to the features on a wafer (such as good sheath models), and the ability to predict the equipment related variations across a wafer would lead to a significant improvement in process understanding.

3. *Feature scale models*—Present feature scale models are continuum models. They do not take into account grains, grain orientations, stoichometry, composition, and interfaces. However these materials considerations dictate the electronic and mechanical properties of the thin film layers. Predictive simulation solutions to these problems are only now becoming feasible.

4. *Chemical-Mechanical-Planarization (CMP) models*—CMP is a difficult chemical-mechanical problem. First order models and simulation tools exist. However with CMP being used on a variety of dielectric

and metallic materials, better predictive models are required. For example, models for feature-scale CMP modeling are needed to analyze dishing/erosion effects in the copper Damascene process.

5. *Interconnect morphology and reliability*—Materials models and simulation capability in this area would accelerate the development of new technology nodes since now over half of the total process is related to that above silicon.

LITHOGRAPHY MODELING

Lithography Modeling and Simulation—can be thought of as being applied on four fronts:

1. *Technology invention*—This includes EUV masks, imaging, resists as well as high beam current electron-beam system optics and resists.
2. *Technology design*—This includes masks, optical systems and wafer topography, and pattern transfer.
3. *Compensation of electronic design*—This includes automating the compensation process for OPC images, OPC resists and PPC.
4. *Manufacturing set point, control and yield*—This includes integrating the dozens of process parameters to find the optimal operation point, assigning causes to residuals, and physically based characterization for efficient modeling.

To enable these applications for future technologies, advances in capabilities are needed in several areas. The first is predictive, quantitative resist modeling. Resist modeling always has been and always will be the bottleneck in predictive lithography simulation. The second is flexible image modeling systems. With numerous resolution enhancement techniques being proposed that involve modifications of the imaging system, as well as the more detailed analysis of imaging non-idealities (such as aberration, mechanical vibrations, illuminator effects), imaging simulation tools that can treat a wide variety of effects are needed. Third, electromagnetic scattering analysis will need to become part of the mainstream analysis capability. Scattering from phase shift masks, and scattering from wafer topography underlying the resist are two examples of applications requiring rigorous electromagnetic capability. Finally, combined information and modeling systems are needed to analyze and optimize future lithography processes. With so many independent parameters, and an avalanche of data to understand, computer-based optimization systems are a requirement to fine tune future technologies that will operate near the limit of diffraction optics.

An important application for the next few technology nodes will be evaluation of the tradeoffs for the various lithography options (such as 193 nm versus 157 nm on specific critical layers). In order to fill this requirement, better imaging models, which include the non-idealities of the respective imaging systems, are needed. Furthermore, improved resist modeling and characterization capabilities need to be developed. More fundamental resist models are needed for many applications, including the understanding of line edge roughness.

With reduced wavelengths, k_1 factors, and the introduction of OPC and phase shift masks, mask making technology and costs are receiving increased attention. To aid this technology area, an integrated simulation system including e-beam, e-beam resist, and mask etch modeling is required.

The existence of numerous post-optical lithography options necessitate that comprehensive modeling capabilities be created to help choosing the best approach.

FRONT END PROCESS MODELING

Front end process modeling includes the simulation of the physical effects of manufacturing steps used to build transistors up to metallization, but excluding patterning activities. These areas are important for understanding and optimizing transistor fabrication. The needs for modeling are driven by the reduction of feature size in scaling transistors.

As technology scales, the requirements on implant energies are pushed to sub-keV energies, requiring understanding of the surface interactions and the nuclear stopping power. For wells, energies are being pushed to the MeV range requiring better understanding of electronic stopping mechanisms. Key to both efforts is damage production. The damage interacts with dopant diffusion and creates transient enhanced diffusion (TED), which can produce junction shifts on the order of several hundred nanometers. Significant effort needs to be expended to understand TED well enough so that the effects can be minimized. Despite a decade of work in this area, quantitative predictive models are still not widely available. Diffusion in gate materials needs to be characterized and understood so that gate stack technologies can be optimized. Interface interactions at the poly/oxide interface also must be understood.

Continuum diffusion and dopant activation models will remain the mainstay of process simulators, and will need refinement as new effects emerge. The effect of interfaces, especially non-SiO_2 interfaces, will become increasingly important. An important contribution of atomistic process models will be to provide coefficients for continuum models. Dopant binding and migration energies with defects need to be calculated. Examples include binding energy of a substitutional dopant to a mobile interstitial, migration energy of the dopant-interstitial pair, and binding energy between a mobile dopant atom or silicon interstitial and a point defect or dopant cluster. Forward and reverse rate coefficient calculations will be needed for several types of dopant-defect and dopant-interface interactions.

Analytic models will continue to be needed for ion implantation simulations in the near term. Monte Carlo implant models will be needed to support analytic model development. To accurately model dopant and damage interactions from source/drain and pre-amorphization implants, models for amorphization layer depth, dislocation loop evolution, and residual TED need to be developed. Extensive research and model development needs to start immediately to develop improved models for damage creation and annealing.

With rapidly shrinking device dimensions, mechanical stress effects are becoming important, and models for the effect of stress on reliability and dopant diffusion need to be developed. Thin film growth needs to be better understood, including the reliability impact of stress in corners and small 3D structures. Characterization of films with small dimensions and thickness is critically important but extremely difficult. In fact, all models need extensive characterization, which has been difficult and expensive. This drives metrology needs.

Advanced process models will be needed for modeling *metastable dopant activation* (> solid solubility). These should include the deactivation kinetics during subsequent backend processing.

Predictive models need to be developed for *advanced doping techniques*, like solid source, plasma implantation, GILD, and rapid vapor phase doping. No technique has emerged as a clear winner so far, and the modeling community needs to monitor the evolution of these techniques and develop models for the most promising ones.

Models for surface diffusion will be needed. These include interactions with SiO_2 and new gate dielectric materials. Process models for *alternative materials* (such as SiGe) also need to be developed.

There will be a continuing need for silicidation models in the near term. Gate dielectric process models, including models for non SiO_2 dielectrics, will be needed to accurately predict gate stack properties and dopant profiles in the channel and source/drain regions. For gate stack modeling, kinetics for oxidation with N_2O, NO and N are needed. In the short term, activation models for polysilicon gates will be needed. In the long term properties of metal gate electrodes will need to be modeled.

At the far end of the Roadmap, atomistic process models will be required. These will also serve to provide the easiest way for testing new continuum diffusion models, which might continue to be the mainstay of process simulators.

NUMERICAL DEVICE MODELING

Device modeling includes a suite of formulations and tools from drift-diffusion simulation via hydrodynamic and numerical Boltzmann to Monte Carlo. The drift-diffusion approach, although physically flawed at 250 nm and below, has been remarkably successful. The key challenges are to 1) further develop this hierarchy to include quantum modeling; 2) refine the physical models in these formulations; and 3) provide an easy means of moving through this hierarchy of formulations in a consistent fashion.

Transport phenomena have so far focused on silicon. For 100 nm devices and below, the gate dielectrics will be so thin that gate current will become a very important design factor. More detailed quantum modeling of the entire gate stack (channel, dielectric, electrode) is needed in order to understand the oxides that are only a few atomic layers thick, as well as to understand the impact of new gate electrode materials. Such modeling should include details of tunneling and transport in the dielectric, reliability effects, surface states, and detailed understanding of effective dielectric constants. Fundamental materials modeling should be instigated to aid in the search for alternative gate dielectric materials.

As MOS devices continue to scale, it is important to understand possible limits to scaling from a modeling perspective. For example, the effect of statistical dopant fluctuation or variations in poly gate line width need to be simulated. Modeling efforts need to track emerging trends to use new materials and alternative device structures for the 100 nm generation and beyond. Exploration of non-traditional devices through modeling is also necessary near the end of the Roadmap.

CIRCUIT ELEMENT MODELING—ECAD

Compact modeling and circuit simulation are key to chip design productivity. The challenges are the drastic increase of clock frequency and the exponential increase of the circuit complexity. Two opposing requirements need to be met, namely accuracy and CPU efficiency. The requirement for accuracy is derived from the clock frequency. With the rise/fall time of a gate loaded with an interconnect line at ~10% of the clock period, the accuracy for rise/fall time prediction should be ~10% (the simulation accuracy should be 1% of the clock period).

This can only be achieved by having accurate DC and high-frequency AC models for transistors, interconnect, passive, and parasitic elements. Model improvements for sub-100 nm need to address velocity overshoot, quantum effects, source barrier effects, and nonquasi-static behavior. Low-voltage technologies emphasize subthreshold and conductance behavior. Robust parameter extraction for these complex models will be a significant challenge. The development of industry-standard circuit models is necessary to support the current business environment, in which design and manufacture often take place in different organizations.

Interconnect delay forms an increasing fraction of critical path delay in current and future technologies. Improving the accuracy of extraction of interconnect parasitics from layout databases is an important requirement; accommodating complex geometries (such as 3D effects) and accurately modeling cross-talk are key issues. At higher clock frequencies, complex electrical effects will be significant, such as inductive coupling, ground bounce, transmission-line, and skin effects. Mismatch in interconnect is a limiting factor for very high speed (>1GHz) processors.

Models that treat reliability concerns, such as ESD, SER, and oxide reliability, will become increasingly important for circuit design. Analog, RF and system-on-a-chip applications will create new demands, for example noise concerns in RF circuits.

Both active and interconnect models need to be characterized for process variations. For example, the variation in interlevel dielectric (ILD) thickness using CMP is more than 20%. The CPU efficiency of the models and simulations drives the number of circuit elements that can be simulated. Since in critical path analysis as much as 10% of all circuit elements may play a role, the CPU efficiency should be enough to handle 10% of the total component count in an overnight simulation.

PACKAGE MODELING

Packaging needs to meet very demanding requirements in the areas of performance, power, junction temperature, and package geometries. Advanced modeling tools are needed that seamlessly cover electrical, thermal, and mechanical aspects, both on- and off-chip. These phenomena can no longer be described independently.

Reliability models for package design and development are needed. Built-in and thermally induced mechanical stresses need to be modeled throughout the 3D stack, coupling the chip and package level. The introduction of low κ dielectrics with low thermal conductivity amplifies the need for accurate thermal simulation, which needs to be solved consistently with electrical behavior given the higher power dissipation levels. Strongly non-uniform heat dissipation across the chip further complicates this analysis, and emphasizes the need for die-package coupling.

Power delivery for high frequency devices has become a major issue. Modeling inductance loops and analyzing return paths that extend over both the package and chip pose a complex problem, for which more powerful, integrated simulation systems are needed. Ideally, simulation systems should generate results working directly from the package and chip layout databases, creating accurate 3D representations of all interconnects.

As we move to higher frequencies, the modeling of electrical signal propagation needs to be improved substantially from approximate RLC modeling to full transmission line modeling. Circuit simulation tools need to couple board to package to chip. Electrical modeling must expand to include digital, analog, and RF devices on the same package or die. Noise coupling through power distribution networks and electromagnetic interference are areas of special concern for "system-on-a-chip" or "system-on-package" approaches.

NUMERICAL METHODS AND ALGORITHMS

Numerical methods and algorithms need improvement to support the growing complexity of physical phenomena in the application tools. For example, more accurate solutions of the Boltzmann transport equation requires dealing with an increasing number of coupled partial differential equations over the device grid, thus driving linear solver technology.

The switch from 2D to 3D, the increase in problem complexity, and the increase in steps for process simulation all require that the failure rate in automated grid generation must drop by at least two orders of magnitude. A grid failure can be defined in a local sense as an incorrectly constructed mesh element or in a more global sense as an excessive truncation error induced in a certain region. Adaptable geometry design utilities are required for equipment/reactor design separate from wafer gridding utilities. For 3D grids, a highly anisotropic grid generator tuned for semiconductor applications is needed (for both static and dynamic grids).

Particle-level Monte Carlo codes need an increase in raw CPU speed as well as variance reduction techniques to minimize noise within acceptable simulation times. The rapidly increasing demand for more MFLOPS may be successfully met by improving hardware, provided current trends continue. Workstation speed has improved by 1.8× on average each year since 1990. Parallel solution strategies are also needed in order to address computationally intensive 3D simulation needs.

Table 87b Modeling and Simulation Technology Requirements: Accuracy/Speed—Near Term

YEAR TECHNOLOGY NODE	1999 180 nm	2002 130 nm	2005 100 nm	Driver
OVERALL TECHNOLOGY COST REDUCTION TARGET (DUE TO TCAD)	20%	25%	35%	
Equipment/Topography Modeling				
Etch/dep. cross wafer uniformity (% accuracy of the control spec)	20%	10%	10%	M
2D/3D topography accuracy	36 nm (20%)	20 nm (15%)	10 nm (10%)	M
Lithography Modeling				
Resist profile prediction accuracy	27 nm (15%)	13 nm (10%)	10 nm (10%)	
OPC model accuracy	9 nm (5%)	6.5 nm (5%)	5 nm (5%)	
Front End Process Modeling				
Vertical and lateral junction depth simulation accuracy	18 nm (10%)	13 nm (10%)	10 nm (10%)	
Total source/drain series resistance (accuracy)	20%	20%	20%	
Long-channel V_t (accuracy)	5% (75–90mV)	4% (48–60mV)	3% (27–36mV)	
Device Modeling (Numerical)				
Accuracy of f_t at given f_t (% of maximum chip frequency)	10%	10%	10%	
Gate leakage current accuracy (%) (decreases due to increase of I_g/I_d)	100%	70%	40%	
I_{off} accuracy	100%	70%	40%	
V_t rolloff accuracy (mV)	25mV	20mV	20mV	
Circuit Element Modeling/ECAD				
I-V error—compact model accuracy	5%	5%	5%	
Sub-threshold current—compact	95%	50%	10%	
Intrinsic MOS C-V—compact model accuracy	<7%	<6%	<5%	
Parasitic C-V—compact model accuracy	5–10%	5–10%	5–10%	
G_m and r_0 at V_t+150mV versus L, V_{bs}, and T	5%	4%	3%	
Circuit delay accuracy (% of maximum chip frequency)	10%	5%	5%	
RLC delay accuracy (% of maximum chip frequency)	10%	5%	5%	
Package Modeling				
Package delay accuracy (% of off-chip clock frequency)	1%	1%	1%	
Stress model accuracy (% of yield stress)	10%	10%	10%	
Temperature distribution for chip and package (accuracy)	5°C	5°C	5°C	
Numerical Methods				
Speed-up of algorithms for 3D process/device	1×	2×	4×	
Linear solvers (kilo equations/minute)	150K	300K	600K	
Parallel speed-up	1×	2×	4×	
MFLOPS required	80	1000	4000	

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 87c Modeling and Simulation Technology Requirements: Capabilities—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
Equipment/Topography			
Equipment simulation	Ab initio simulation of materials properties	Computer engineered materials and process recipes	
Lithography			
Next generation lithography	EUV and E-beam system	Beyond roadmap lithography models	
Resist technology	EUV resists	Finite polymer-size effects	Non-conventional photo-resist models
Front End Process Modeling			
Advanced process models	Metastable activation (>solid solubility)	Alternative materials (such as SiGe)	Atomistic process model
Advanced doping models	Solid source	New technology needed	
Numerical Device Modeling			
Alternative device models	2D quantum models for MOS	Single electron transistor	Quantum effect devices
Circuit Element Modeling/ECAD			
Advanced circuit models	Quantum effets/non-quasi-static	Circuit models for alternative devices	New technology needed
Package Modeling			
Electrical/optical models	Full-wave analysis	Mixed electrical/optical analysis	New technology needed
Numerics			
Numerical algorithms	Exploit parallel computation	Efficient atomistic/ quantum methods	Multi-scale simulation (atomistic-continuum)

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

MATERIALS MODELING

While not a distinct application area in itself, materials modeling is an important new potential solution that can impact many other areas. Several factors are pointing towards the need and use of materials simulation tools for helping resolve challenges in future technology nodes:

- With devices continuing to shrink to nearly atomistic dimensions, materials simulation and modeling tools that go from the continuum to atomistic descriptions will become more and more important.
- Many alternate materials are being suggested as possible solutions for some of the critical semiconductor roadmap roadblocks. Materials simulation tools would allow many "what-ifs" without the need for many and complex experimental characterizations.
- Modeling and simulation tools in equipment, process, device, package, patterning, and interconnect are only as good as the input materials parameters. In many cases, these parameters are not known. Fundamental materials simulations and quantum chemistry calculations will aid in establishing this knowledge base.

The potential solutions Figure 62 indicates materials needs across all areas.

1. *Equipment/topography modeling*—fundamental materials modeling would provide chemical reaction rates, materials-plasma cross sections, surface and feature scale kinetics, physical vapor deposition material constants, and chemical-mechanical materials constants.

2. *Lithography modeling*—materials models are needed for improved resists and for advanced mask making.
3. *Front End Process modeling*—Predictive materials modeling would provide ion implantation codes with no adjustable parameters, of predicting very shallow and low concentration dopant profiles, and of modeling new gate dielectrics.
4. *Device modeling*—As device geometries shrink, materials modeling that goes from the continuum to atomistic predictions will facilitate the development of next generation gate stacks.
5. *Circuit element modeling/ECAD*—new memory cells such as flash and novel DRAM cells are based on complex materials-electronic transport mechanisms.
6. *Package modeling/materials modeling*—would support the prediction of the thermal and mechanical properties of packages, and of reliability issues such as adhesion, fatigue, and thermal stability.

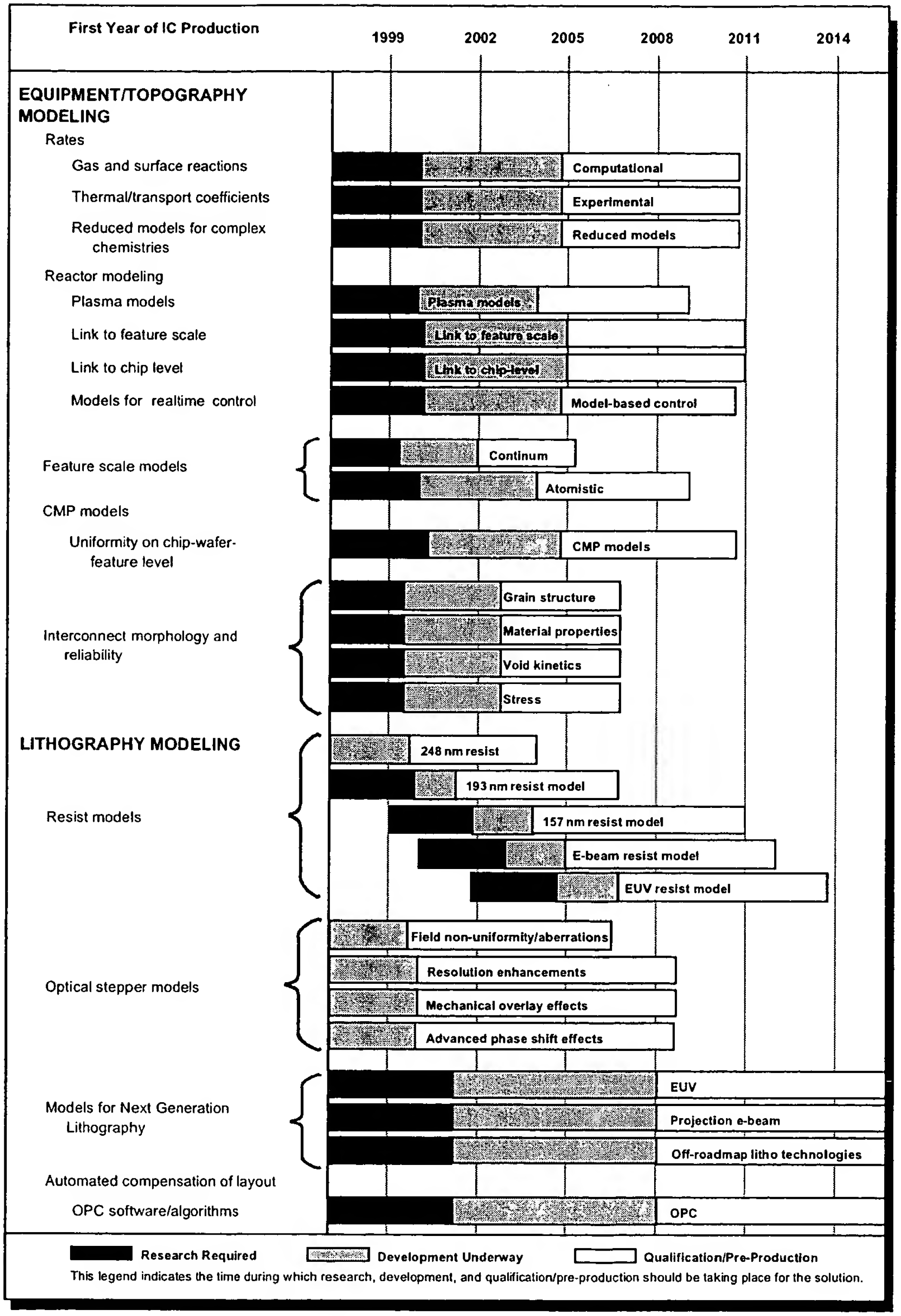

Figure 62 Modeling and Simulation Potential Solutions

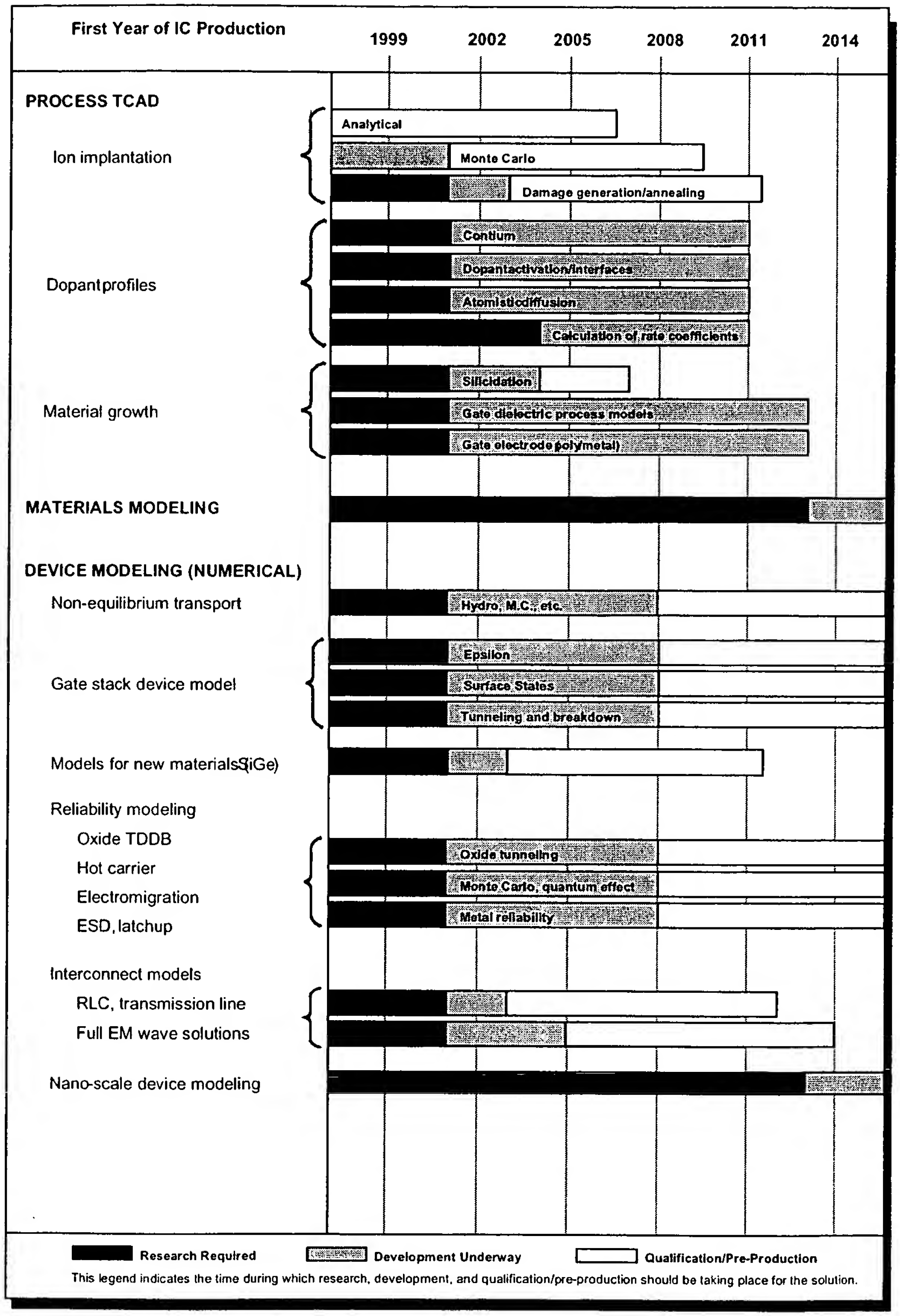

Figure 62 Modeling and Simulation Potential Solutions (continued)

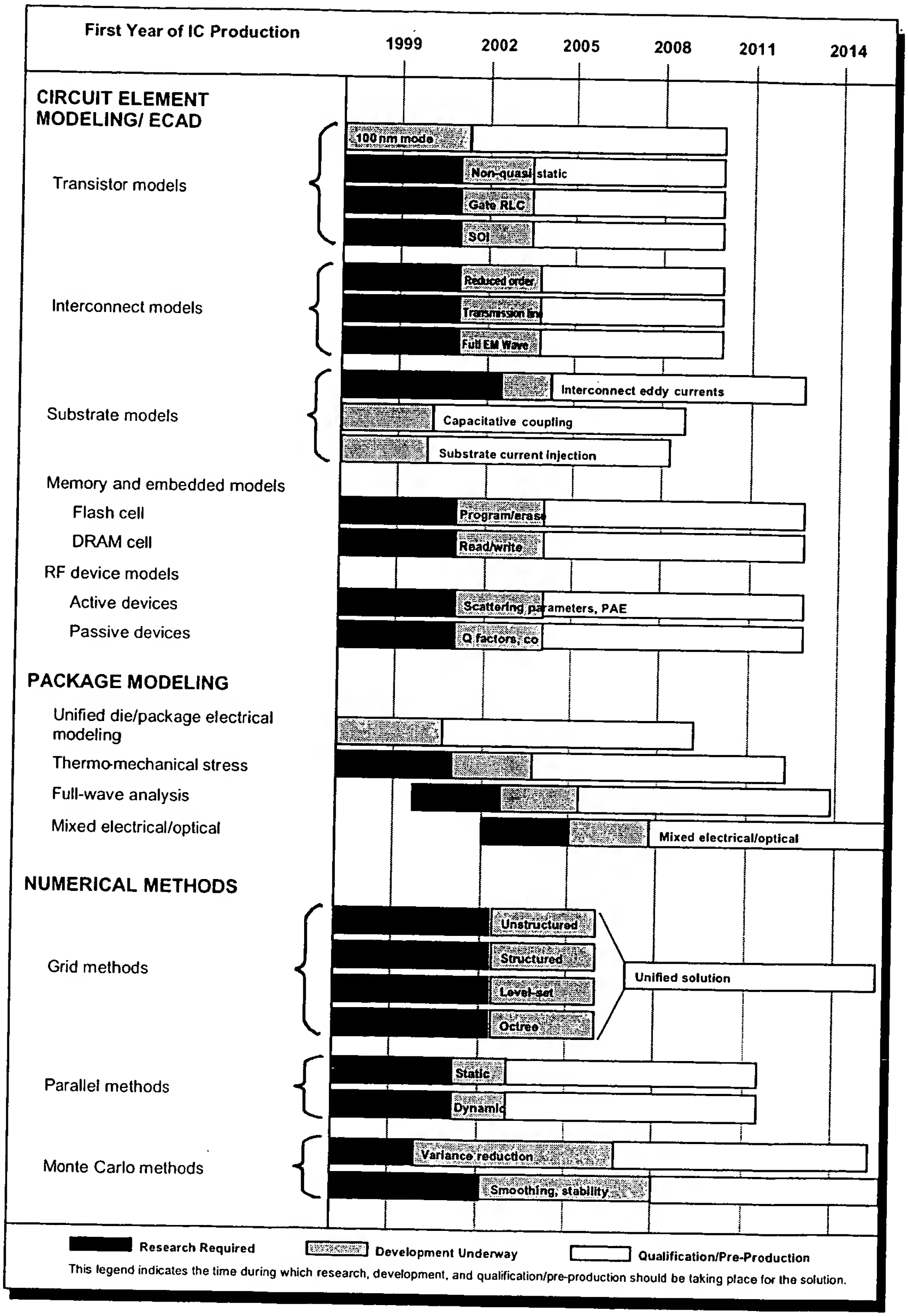

Figure 62 Modeling and Simulation Potential Solutions (continued)